National Semiconductor

LMX2512LQ0967

EVALUATION BOARD OPERATING INSTRUCTIONS

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LMX2512LQ0967FPEBI Rev 02.21.03

National Semiconductor

Table of Contents

1 General Description

The LMX2512 Evaluation Board simplifies evaluation of the LMX2512 Dual PLL with integrated RF VCO. The board allows for the evaluation of many RF and IF PLL performance parameters with various control settings including: phase noise, lock time and spurious. The CodeLoader software gives the user a simple means of programming the IC's control registers. The board has sufficient flexibility to allow the user to place an additional on-board supply regulator and TCXO.

The evaluation board circuitry consists of an LMX2512LQ0967 device, an IF VCO and a discrete IF loop filter. SMA flange mount connectors provide for the RF VCO (**RF_OUT**), IF VCO (**IF_OUT**) and RF lock detect (**LD**) outputs, the reference frequency (**OSC_IN**) input and the power (**VDD_5V**) connection. A MICROWIRE™ cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of serial port emulation, the CodeLoader software facilitates the LMX2512LQ0967 internal register programming for evaluation and measurement.

2 Setup

The fully assembled LMX2512 Evaluation Board is factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

2.1.1 Recommended Test Equipment

- Spectrum analyzer with operating frequency range > 2 GHz
- Modulation domain analyzer
- Low noise signal source adjusted to desired reference frequency
- DC power supply with adjustable voltage output

2.1.2 Connection and Setup

1. Connect the **RF_OUT** or **IF_OUT** output port to the input of the spectrum analyzer for phase noise and reference spur measurement or to the input of the modulation domain analyzer for lock time measurement. Connect the unused port to a suitable 50-ohm termination.

2. Connect an RF signal generator or TCXO to the **OSC_IN** port of the evaluation board. Set the RF frequency to the desired reference frequency, 19.68 MHz for the default case. Set the RF level to 1 dBm (~0.7 Vpp).

3. Plug the DB25 connector end of the cable assembly to the parallel port of the PC. Connect the other end of the cable to the on-board 10 Pin Header (**uWire**) with the strip on the cable at the end opposite the end with the **uWire** label. Refer to Appendix E for more details. Alternatively, refer to the CodeLoader Operating Instructions from National Semiconductor's Wireless Communications website: wireless.national.com.

4. Verify that jumper blocks **JP1** and **JP2** contain a full compliment of shunts. **JP1** connects the 5.0 V supply input (**VDD_5V**) to the on board regulator. For convenience, an additional regulator circuit and TCXO are included on the layout but not placed. **JP2** connects the 2.8 V regulated supply to various supply pins on the LMX2512 and the IF VCO.

5. Turn the DC power supply ON and adjust the voltage output to 5.0 V. Turn the DC power supply OFF.

6. Connect the DC power supply output to the **VDD_5V** port of the evaluation board. Turn the DC power supply ON.

7. Run the CodeLoader software for LMX2512 register programming. Ensure proper port setup and that the reference frequency matches the CodeLoader programming in the Bits/Pins and RF and IF PLL tabs. Refer to Appendix E for more details.

3 Measurement Considerations

3.1 Phase Noise Measurement

Measure the phase noise characteristics of the PLL with spectrum analyzer or a VCO/PLL analyzer. The phase noise plots in these instructions are from a VCO analyzer and give an overall picture of the phase noise of the LMX2512LQ0967. The VCO analyzer provides plots of the phase noise over a span of offset frequencies giving the designer a more complete indication of a device's overall phase noise performance.

For phase noise measurements at fixed offset frequencies, use an analyzer with a noise floor below the level of measurement interest. Since they are more readily available, below is an explanation of this test technique using a spectrum analyzer.

Tune the spectrum analyzer to the desired center frequency with the span adjusted to include the appropriate offset frequency. Using the delta marker, the difference between the carrier and the noise level at the desired offset frequency is measured. The video averaging feature of the spectrum analyzer should used to better determine the noise level.

The phase noise is a 1 Hz normalized bandwidth measurement expressed in dBc/Hz. Most modern spectrum analyzers have a feature that automatically normalizes the phase noise measurements to a 1 Hz bandwidth. This feature gives greater measurement accuracy. For spectrum analyzers without this feature, the normalized phase noise is equal to the noise level relative to the carrier minus 10 * $\log_{10}$ [Resolution Bandwidth].

For accurate close-in phase noise measurements, the offset frequency selected should be inside the loop bandwidth on the flat portion of the curve.

With either measurement method, VCO analyzer or spectrum analyzer, care should be taken to ensure the noise floor of the instrument does not limit the phase noise measurement.

3.2 Loop Filter Bandwidth Measurement

The loop bandwidth is the bandwidth of the closed loop PLL system. It is by definition, the frequency that makes the forward loop gain equal to zero. The spectrum analyzer span is set to view the characteristic rising, peaking, and falling of the phase noise. Measurement of the loop bandwidth is rather complex. It is simpler to measure the 0 dB bandwidth. Although, not the same, the 0 dB bandwidth is a sufficient estimate of the loop filter bandwidth. The 0 dB bandwidth is defined as the frequency where the phase noise falls back to the level of the close-in value after rising to its peak value. The value measured is typically greater than the true loop filter bandwidth. For this evaluation, the 0 dB bandwidth is measured.

3.3 Reference Spur Measurement Using a Spectrum Analyzer

The reference spurs can be seen on a spectrum analyzer and are measured in dBc. The spectrum analyzer is set to the desired center frequency with a span which allows the reference sidebands to be viewed. The spurious level is the difference between the level of the VCO output frequency tone and the level of the spur at an offset equal to the carrier frequency +/- the comparison frequency.

For a more accurate account of a device's spurious performance, the reference spurs across the VCO's frequency band should be determined. The worst-case spur is typically defined as the PLL's spur performance.

3.4 Lock Time Measurement Using a Modulation Domain Analyzer

The modulation domain analyzer measures the switching speed, or lock time, using a frequency versus time plot.

Set the center frequency of the modulation domain analyzer to the final (settling) frequency. Use a wide span allows viewing of the entire positive or negative switching waveform. Use a narrower span to evaluate the settling waveform within +/- 1 kHz. A trigger condition, typically a latch enable pulse, specifies the event that will cause the modulation domain analyzer to capture and display the measurement results. The lock time is the time difference between the point the frequency starts to change (T_1), and the point the VCO frequency settles to within +/- 1 kHz of the final value (T_2), (i.e. lock time = $T_2 - T_1$).

Use the BurstMode tab of the CodeLoader software to program the device to toggle between a desired minimum and maximum frequency. It is necessary to include a sufficient delay, such as 100000, after each programming command. For more detail, refer to the BurstMode Tab section in the *CodeLoader Operating Instructions* from National Semiconductor's Wireless Communications website: *wireless.national.com*.

4 Evaluation Board and CodeLoader Configuration

4.1 CodeLoader Control Settings

Table 4.1.1 summarizes the settings of the programming registers used in creating the plots in the following section. To aid in setting up the correct configuration, the Mode pull down menu contains a default state for CodeLoader. The default mode will set the bits to a known working state. Use this mode to reset the configuration of the registers. The LMX2502/12 datasheet provides additional details about the controls.

Note on SPI_DEF control:

With SPI_DEF set to 1, the initial startup of the LMX2512LQ0967 requires only the Default words (R0 – R3). After startup, only word R0 is required to change the RF frequency. Setting SPI_DEF to 0 allows words R4 through R6 to be loaded into the registers.

The LMX2512LQ0967 operates using one of three default IF frequencies depending on the application and frequency plan. With the SPI_DEF bit set to 1, the IF N and R counter values from the IF PLL tab are ignored, and the appropriate default values are used based on the selected reference (OSC_FREQ) and IF frequency (IF_FREQ) from the Bits/Pins tab. If a non-default IF frequency is desired, the SPI_DEF bit must be set to 0 and the desired IF frequency can be entered using the IF PLL tab.

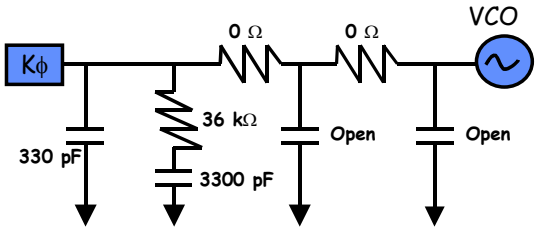
Note on Reference Frequency Controls:

The Bits/Pins, RF PLL and IF PLL tabs contain reference oscillator controls. For SPI_DEF = 1, the IF PLL uses the OSC_FREQ and IF_FREQ controls on the Bits/Pins tab to determine the counter values. For SPI_DEF = 0, the IF PLL uses reference frequency control on the IF PLL tab to determine the N counter values (IF_A, IF_B) based on the IF VCO frequency entered. The RF PLL uses reference frequency control on the RF PLL tab to determine the N counter values (RF_A, RF_B, RF_FN) based on the RF VCO frequency entered. These reference frequency controls are independent, and to obtain predictable device behavior, set them to the same reference frequency.

Table 4.1.1 CodeLoader Default Control Settings

Control Register Name	Setting
Bits/Pins Tab	
RF PLL Controls	
RF_EN	High (Checked)
OB_CRL	11 (Maximum)
SPUR_RDT	10 Cont-Recommended
VCO_CUR	11 (Max-Recommended)
IF PLL Controls	
IF_EN	High (Checked)
SPI_DEF	High (Checked)
IF_FREQ	440.76 MHz
IF_CUR	300 uA
Misc Controls	
OSC_FREQ	19.68 MHz
RF_LD	Hard Zero
Bandwidth Controls	
BW_EN	High (Checked)
BW_DUR	00 (Min-Recommended)
BW_CONT	00 (Max-Recommended)
Program Pins	
CE	High (Checked)
TRIGGER	Low (Not Checked)
RF PLL Tab	
Reference Oscillator	19.68 MHz
Fractional Compensation	253
Fractional Denominator	1968
VCO	966.85 MHz

4.2 IF PLL Loop Filter Parameters



Settings For Operation	
Charge Pump Gain (Kϕ)	300 μA
Comparison Frequency (F_{comp})	120 kHz
Output Frequency (F_{out})	(435 – 465) MHz
VCO Supply	2.8 V
Other Information	
VCO Used	Varil LVCO-4279U
VCO Gain	20 MHz/V

Figure 4.2.1 IF loop filter parameters

5 Typical Performance Measurements

The LMX2512 Evaluation Board typical performance criteria is shown below:

5.1 Evaluation Conditions

Table 5.1.1 Test Conditions

Operating Voltage	2.8 V from regulator output
Reference Frequency	19.68 MHz
RF VCO Tuning Range	(954 – 980) MHz
RF Comparison Frequency	19.68 MHz
IF VCO Tuning Range	(435 – 465) MHz
IF Comparison Frequency	120 kHz

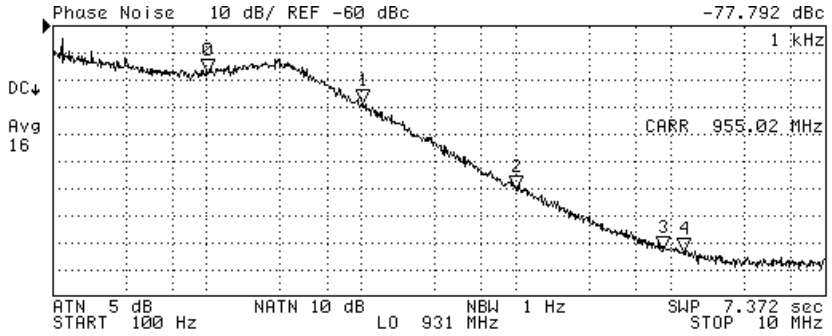
5.2 Typical Performance Criteria

Table 5.2.1 Typical Performance Criteria

RF PLL Phase Noise	< -112 dBc/Hz at 100 kHz Offset
RF PLL Reference Spur	< -75 dBc at 19.68 MHz Offset
RF PLL Lock Time	< 800 μs (Within +/- 1 kHz Settling Frequency)
IF PLL Phase Noise	< -80 dBc/Hz at 1 kHz Offset
IF PLL Reference Spur	< -80 dBc at 120 kHz Offset

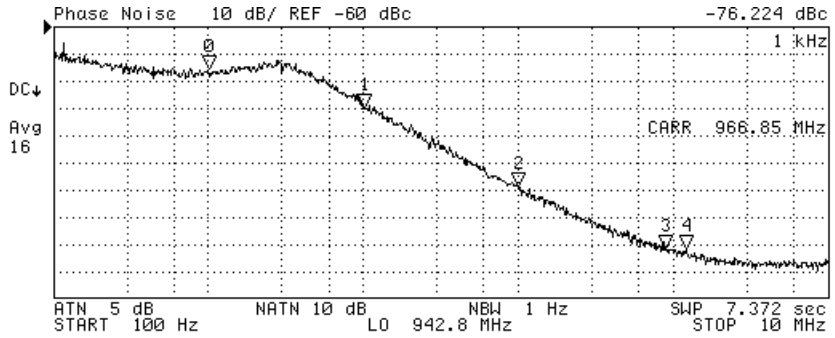
Remark: Computer monitors and other lab equipment can cause noise spikes. If noise spikes are present on the signal, try turning off the monitor or other equipment to verify that they are not the cause. In addition, noise may be getting onto the signal through the cable that connects to the parallel port of the computer.

5.3 RF PLL Typical Performance Measurements



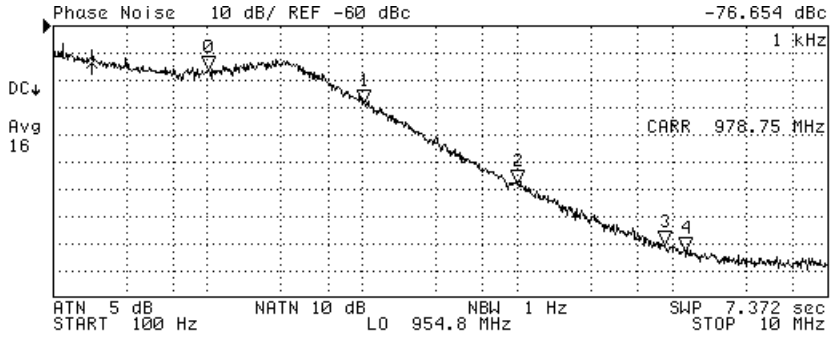
N	SWP PARAM	VAL
0	1 kHz	-77.792 dBc
1	10 kHz	-88.874 dBc
2	100 kHz	-121.21 dBc
3	900 kHz	-143.54 dBc
4	1.25 MHz	-144.3 dBc

Figure 5.3.1 RF VCO phase noise and loop bandwidth (low channel – 955.02 MHz)



N	SWP PARAM	VAL
0	1 kHz	-76.224 dBc
1	10 kHz	-89.971 dBc
2	100 kHz	-119.06 dBc
3	900 kHz	-142.18 dBc
4	1.25 MHz	-142.51 dBc

Figure 5.3.2 RF VCO phase noise and loop bandwidth (mid channel – 966.85 MHz)



N	SWP PARAM	VAL
0	1 kHz	-76.654 dBc
1	10 kHz	-89.074 dBc
2	100 kHz	-118.51 dBc
3	900 kHz	-141.22 dBc
4	1.25 MHz	-143.56 dBc

Figure 5.3.3 RF VCO phase noise and loop bandwidth (high channel – 978.75 MHz)

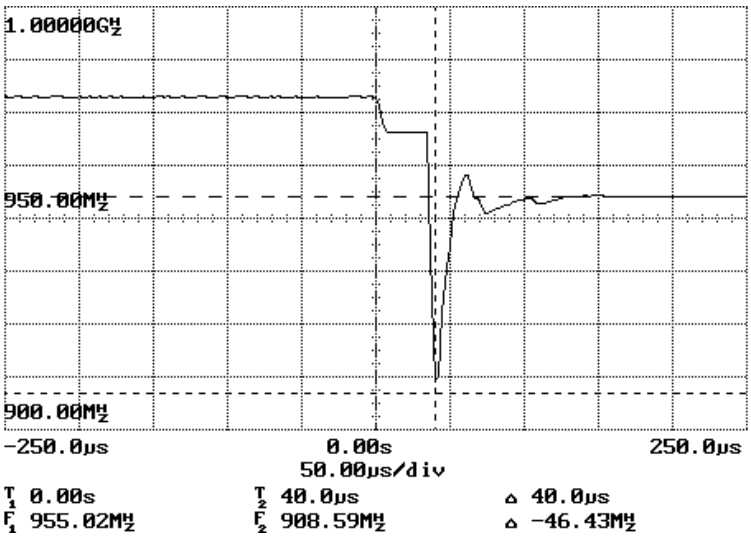


Figure 5.3.4 RF PLL negative frequency switching waveform

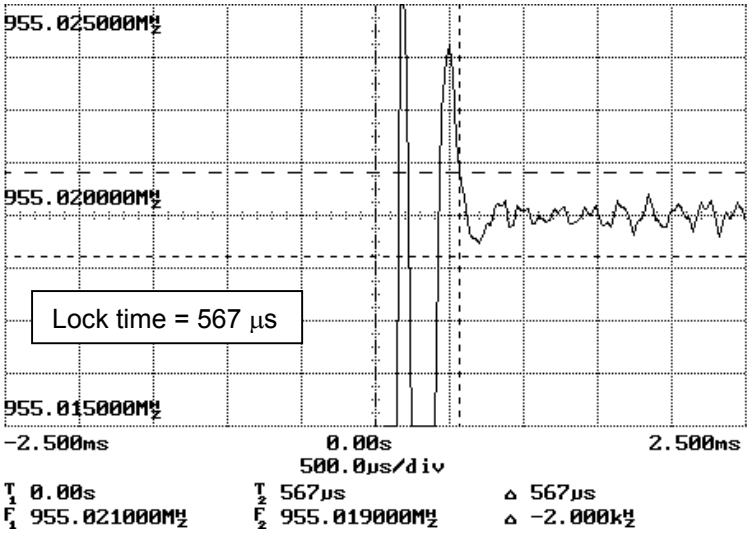


Figure 5.3.5 Lock time from 978.75 MHz to 955.02 MHz

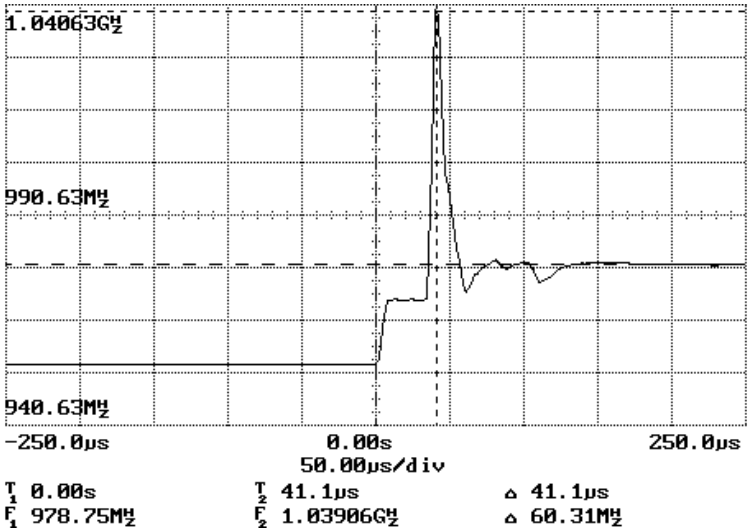


Figure 5.3.6 RF PLL positive frequency switching waveform

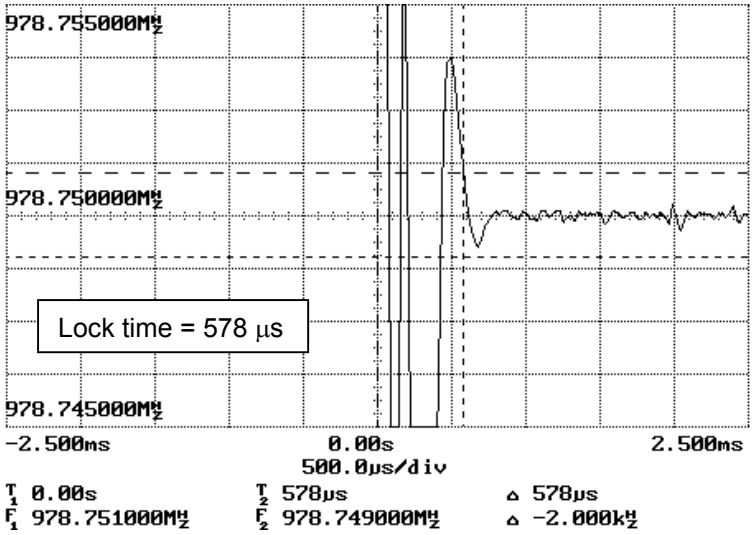
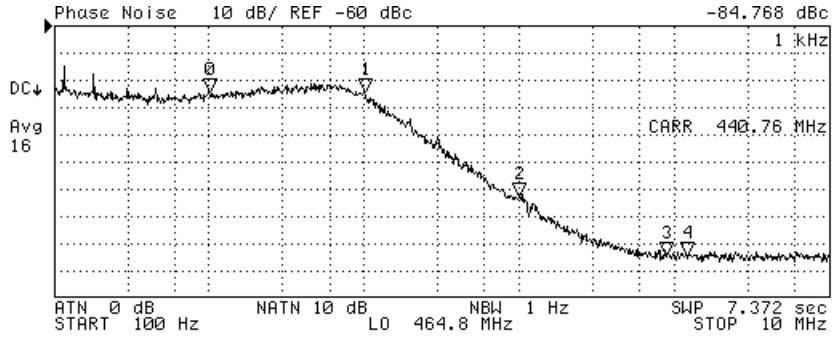


Figure 5.3.7 Lock time from 955.02 MHz to 978.75 MHz

5.4 IF PLL Typical Performance Measurements



N	SWP PARAM	VAL
0	1 kHz	-84.768 dBc
1	10 kHz	-84.975 dBc
2	100 kHz	-123.11 dBc
3	900 kHz	-144.98 dBc
4	1.25 MHz	-145.43 dBc

Figure 5.4.1 IF VCO phase noise and loop bandwidth

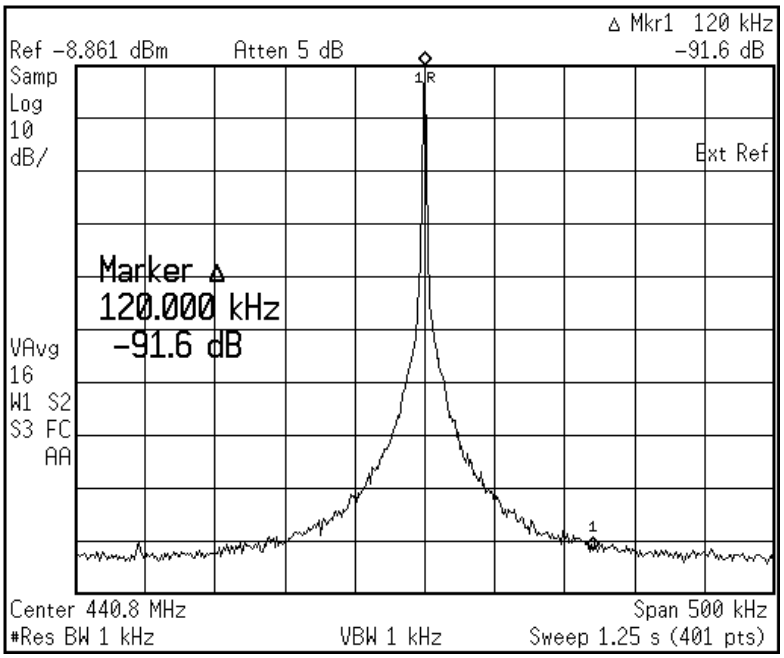


Figure 5.4.2 IF PLL reference spurs at 120kHz offset (spur level <-91.6 dBc)

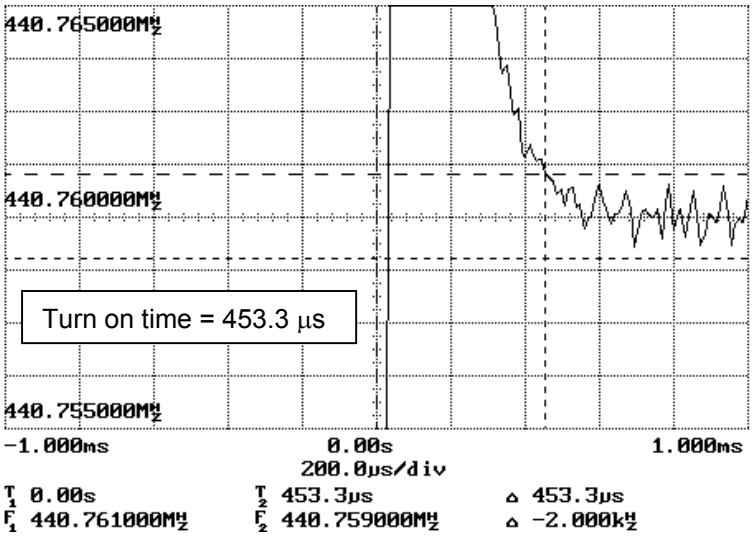


Figure 5.4.3 IF PLL turn on time (with CE control pin)

APPENDIX A:

Evaluation Board – Schematic

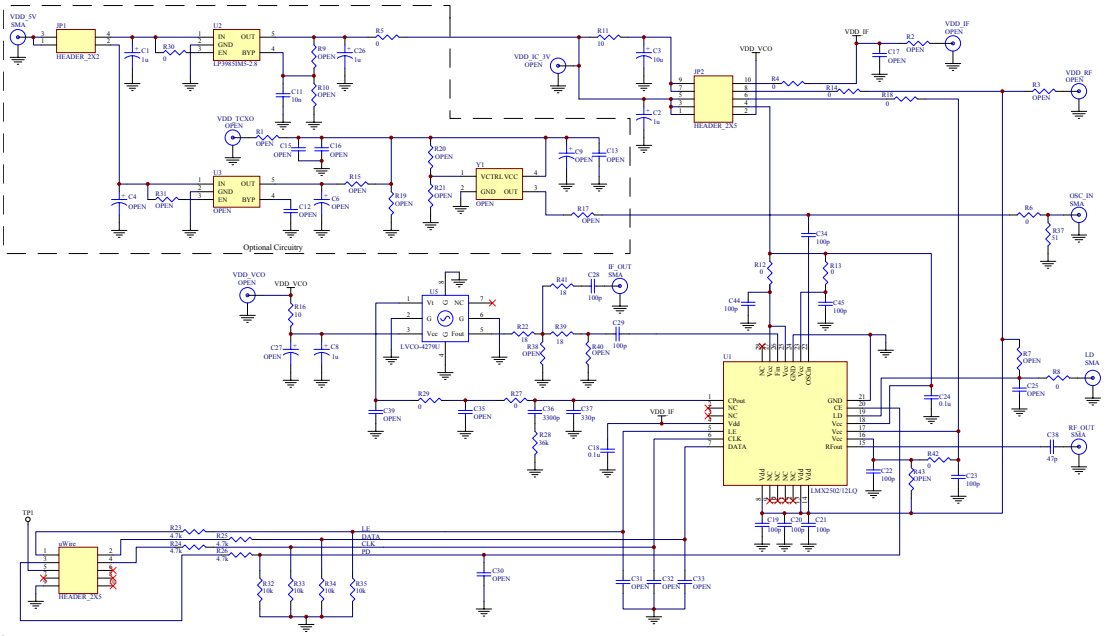


Figure A.1 Schematic

Note: The default configuration has all jumpers placed on the board.

APPENDIX B:

Evaluation Board – Build Diagram

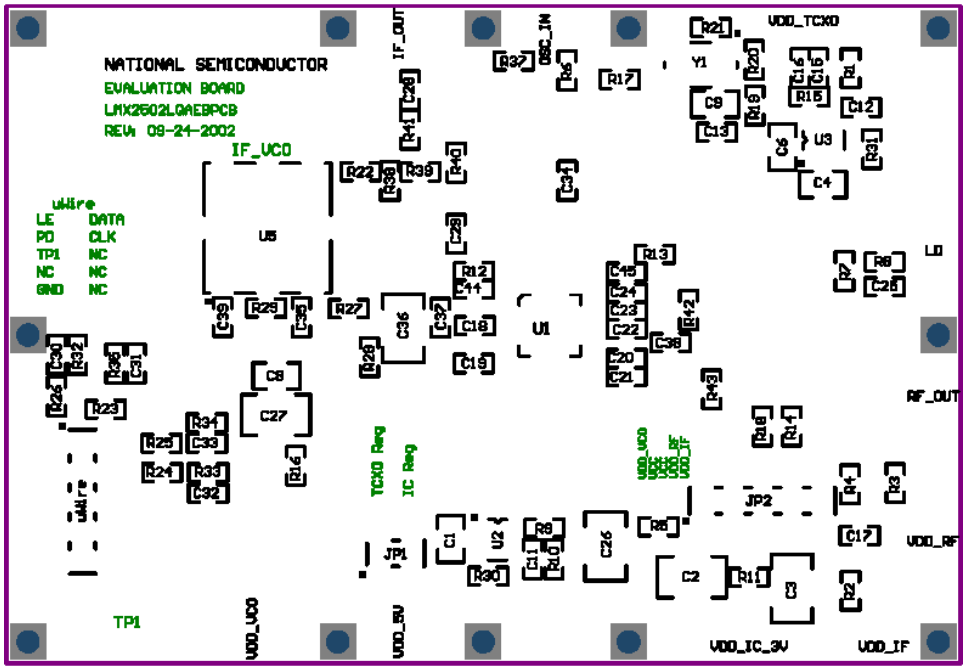


Figure B.1 Top layer (top view)

APPENDIX C:
Evaluation Board – Bill of Materials

Table C.1 Bill of Materials

Item #	QTY	Part Number	Description	Reference Designators	Preferred Vendor
0	38	N/A	Open, No component	C4, C6, C9, C12, C13, C15, C16, C17, C25, C27, C30, C31, C32, C33, C35, C39, R1, R2, R3, R7, R9, R10, R15, R17, R19, R20, R21, R31, R38, R40, R43, U3, VDD_IC_3V, VDD_IF, VDD_RF, VDD_TCXO, VDD_VCO, Y1	N/A
1	1	C0603C470J5GAC	CAP, 47 pF, Ceramic, 5%, NPO, 0603	C38	Kemet
2	10	C0603C101J5GAC	CAP, 100 pF, Ceramic, 5%, NPO, 0603	C19, C20, C21, C22, C23, C28, C29, C34, C44, C45	Kemet
3	1	C0603C331J5GAC	CAP, 330 pF, Ceramic, 5%, NPO, 0603	C37	Kemet
4	1	C0805C332J3GAC	CAP, 3300 pF, Ceramic, 5%, COG, 0805	C36	Kemet
5	1	C0603C103K4RAC	CAP, 10nF, Ceramic, 10%, X7R, 0603	C11	Kemet
6	2	C0603C104K4RAC	CAP, 0.1 uF, Ceramic, 10%, X7R, 0603	C18, C24	Kemet
7	4	C0805C105K4RAC	CAP, 1 uF, Ceramic, 10%, X7R, 0805	C1, C2, C8, C26	Kemet
8	1	TCKOJ106AT	CAP, 10 uF, Tantalum, 10%	C3	Cal-Chip
9	12	CRCW0603000JRT1	RES, 0 ohm, 0603	R4, R5, R6, R8, R12, R13, R14, R18, R27, R29, R30, R42	Vishay
10	2	CRCW0603100JRT1	RES, 10 ohm, 0603	R11, R16	Vishay
11	3	CRCW0603180JRT1	RES, 18 ohm, 0603	R22, R39, R41	Vishay
12	1	CRCW0603510JRT1	RES, 51 ohm, 0603	R37	Vishay
13	4	CRCW0603472JRT1	RES, 4.7k ohm, 0603	R23, R24, R25, R26	Vishay
14	4	CRCW0603103JRT1	RES, 10k ohm, 0603	R32, R33, R34, R35	Vishay
15	1	CRCW0603363JRT1	RES, 36k ohm, 0603	R28	Vishay

16	1	HTSM3203-4G2	HEADER, 4 Pin	JP1	Comm Con Connectors
17	2	HTSM3203-10G2	HEADER, 10 Pin	JP2, uWire	Comm Con Connectors
18	1	LMX2512LQ0967	PLL/VCO IC	U1	National Semiconductor
19	1	LP3985IM5-2.8	2.8V REGULATOR	U2	National Semiconductor
20	1	LVCO-4279U	VCO	U5	Varil
21	5	5762SF	CONNECTOR, SMA, 50 ohm	IF_OUT, LD, OSC_IN, RF_OUT, VDD_5V	CDI
22	7	CCIJ255G	SHUNT, Single, .100" Center, Closed Top		Comm Con Connectors
23	1	225325GTSP	FRAME, 2.25" x 3.25"		Lux Manufacturing
24	12	OF12SHCA	SCREW, 0-80x1/8		Orlander Inc
25	10	2C18PPMZZ	SCREW, 2-56x3/16, Philips, pan head		Orlander Inc

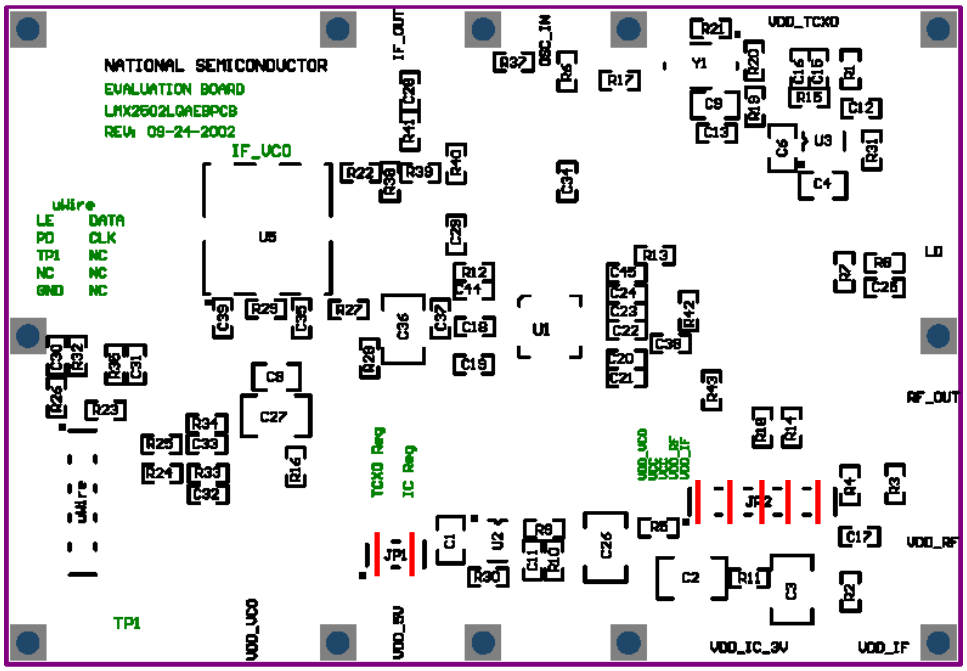


Figure C.1 Shunt placement (top view)

Note: Shunts placed on JP1 and JP2 as indicated by RED lines.

APPENDIX D:
Evaluation Board – Board Layout

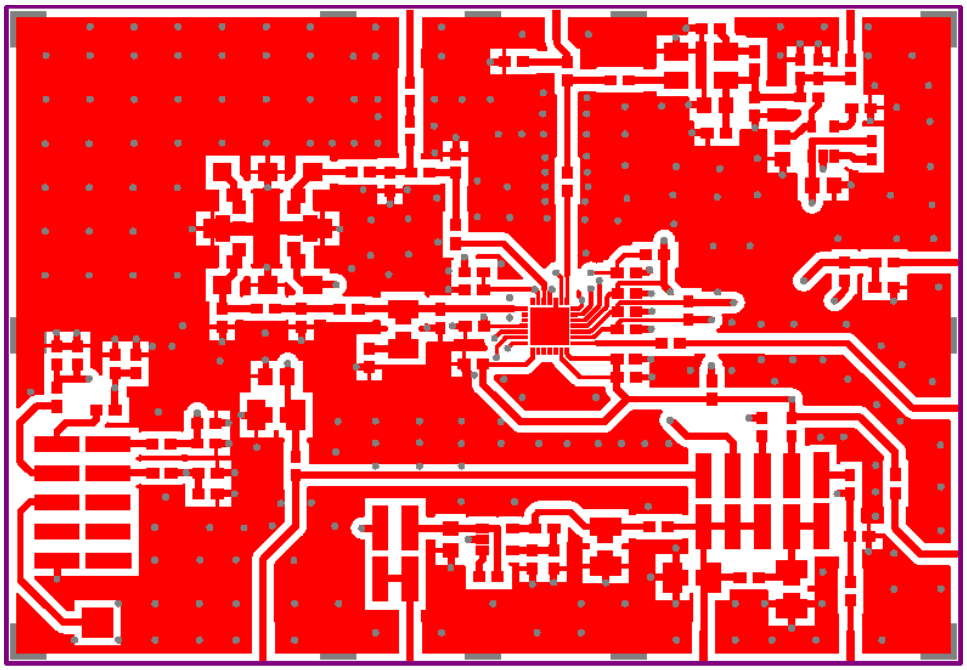


Figure D.1 Top layer

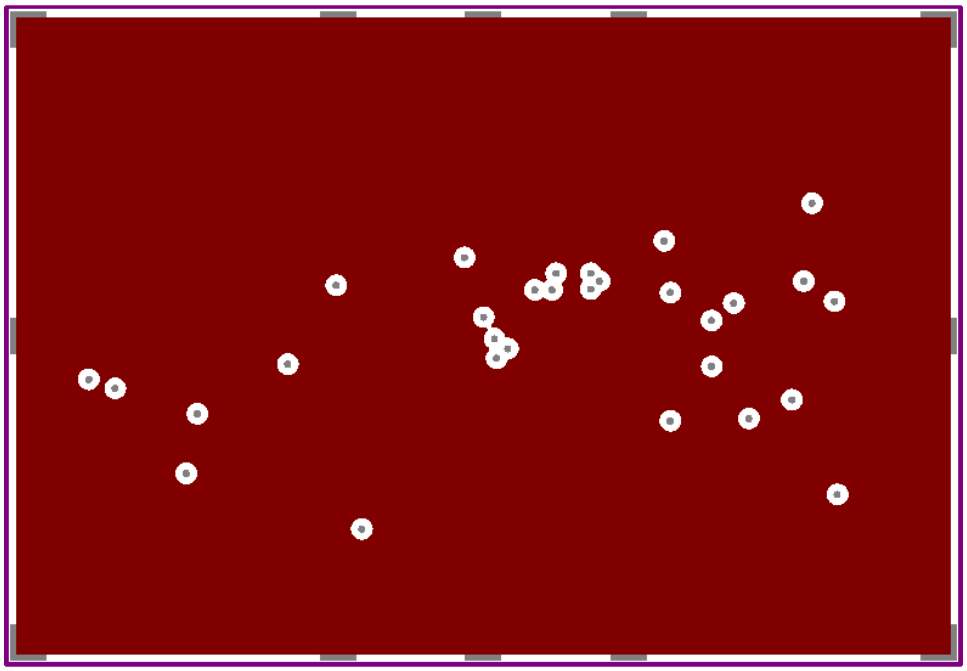


Figure D.2 Mid layer 1

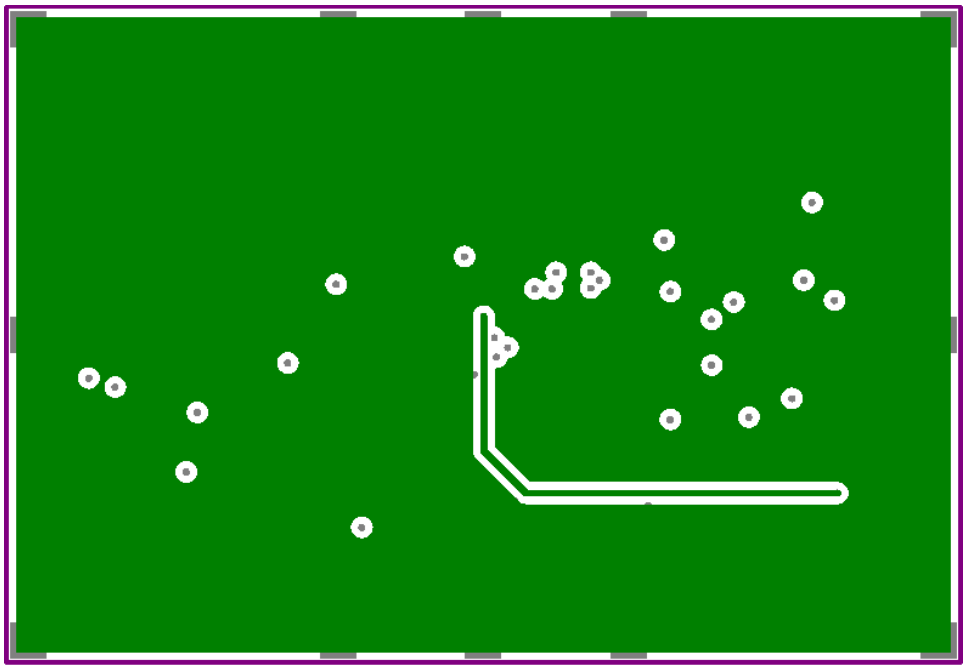


Figure D.3 Mid layer 2

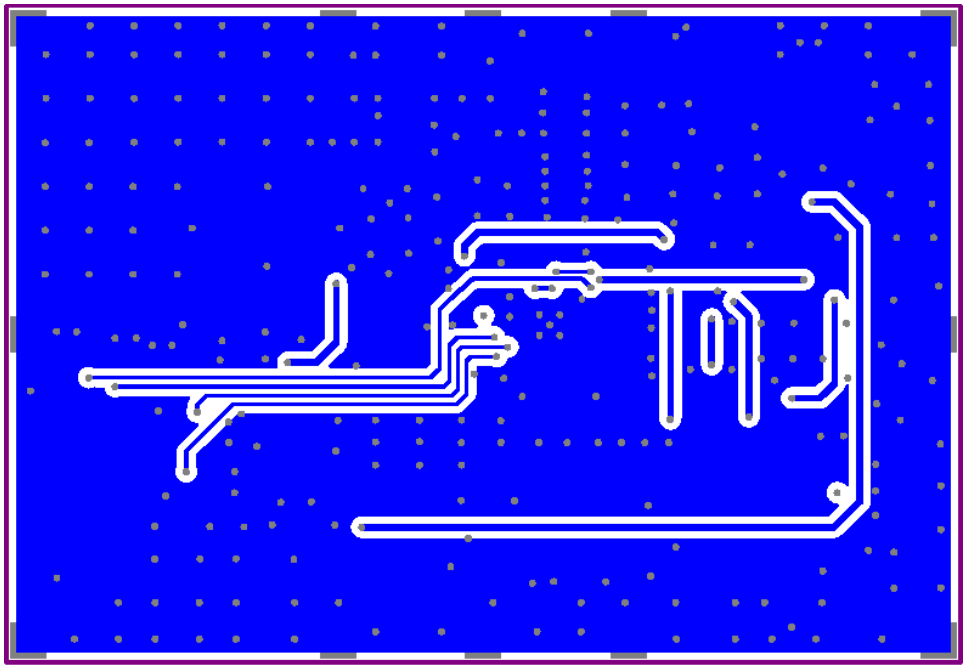


Figure D.4 Bottom Layer

APPENDIX E:

CodeLoader Software Setup

The port setup is necessary to tell the CodeLoader program which signals to send to which locations on the computer parallel port. The proper pin configuration for this part is shown below. The Port Address may change depending on the PC.

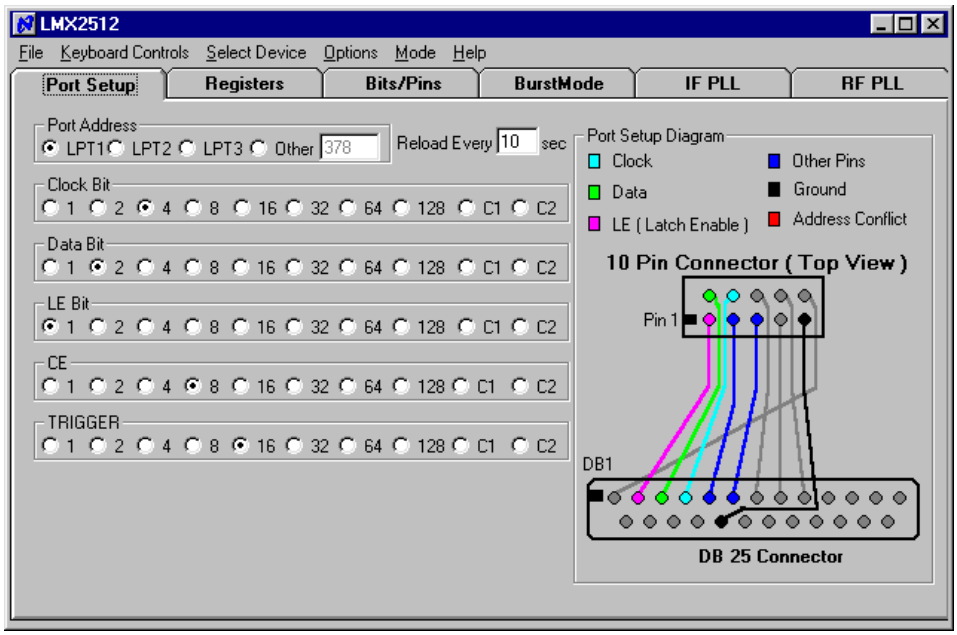


Figure E.1 Proper Port Setup

Table E.1 Port Setup and Corresponding PC Parallel Port and 10-Pin Header Configuration

Port Setup Name	Port Setup Column	DB25 Connector Pin	10-Pin Header Pin
1	1	DB2	1
2	2	DB3	2
4	3	DB4	4
8	4	DB5	3
16	5	DB6	5
32	6	DB7	6
64	7	DB8	7
128	8	DB9	8
C1	9	DB1	10
C2	10	DB25	Not Used
N/A	N/A	18 (Ground)	9

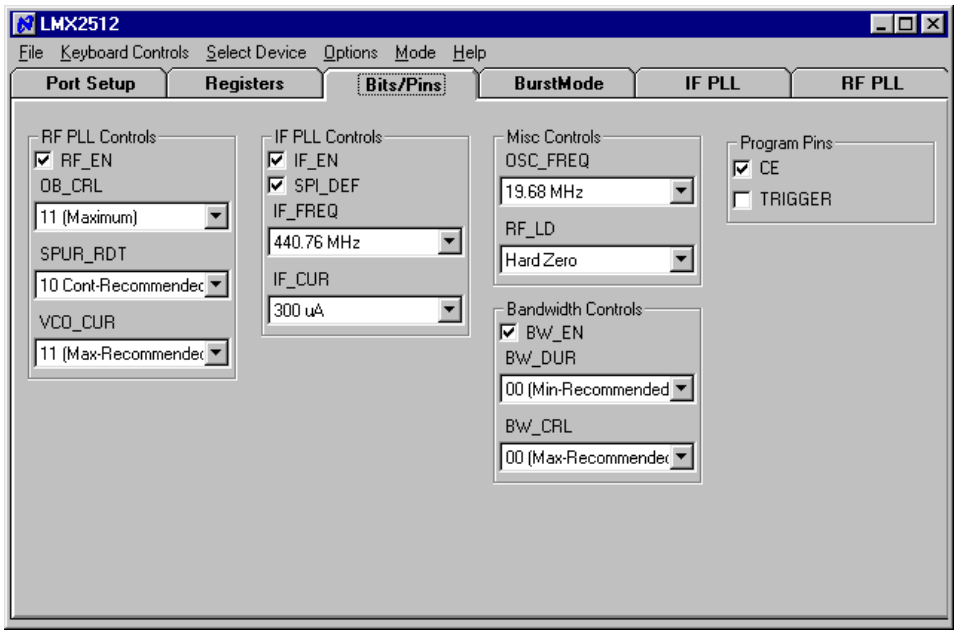


Figure E.3 Default Bits/Pins Setup

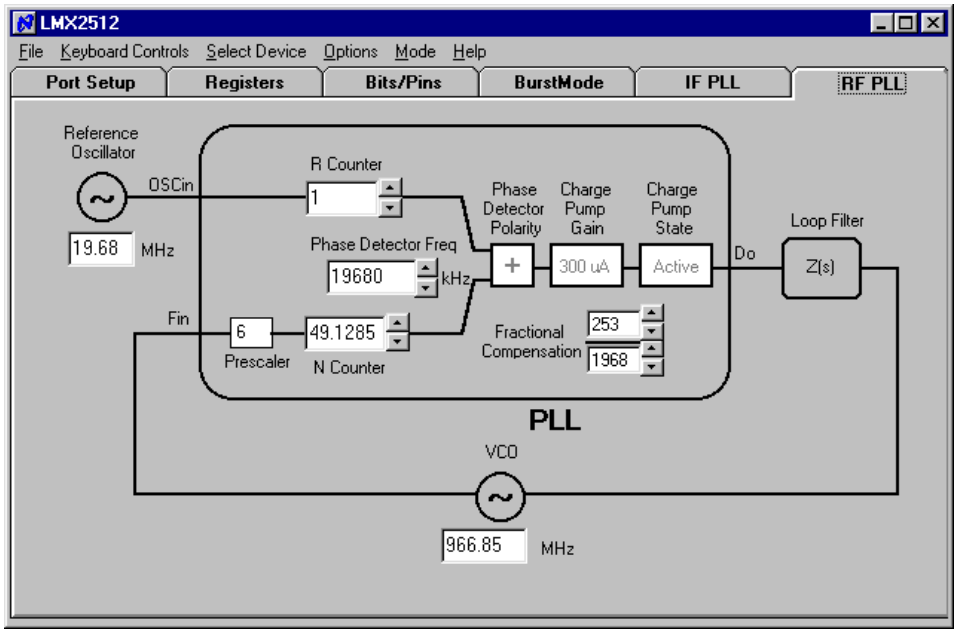


Figure E.4 Default RF PLL Setup

Special Note:

Version 2.1.3 of CodeLoader contains a known problem, to be corrected in the next version of CodeLoader, associated with programming the RF PLL frequency.

To program the RF PLL to frequencies with fractional values greater than 0.5, the fractional numerator must be entered manually. When the desired frequency is entered in the frequency box, the program will round the fractional compensation up to the next integer N counter value. The following example illustrates the problem.

Correct Values:
Desired Frequency: 974.32 MHz
Reference Frequency: 19.68 MHz
N Counter: 49.5081
Fractional Comp.: 1000

For the frequency 975 MHz, the displayed values are:

Desired Frequency: 984 MHz
N Counter: 50
Fractional Comp.: 0

To overcome this problem, the N counter and fractional compensation need to be set manually. In this example, set the N counter to 49 and the fractional compensation to 1000.