LMX2433SLE
EVALUATION BOARD OPERATING INSTRUCTIONS

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LMX2433SLEFPEBI Rev 02.08.06

Table of Contents

1.0 General Description

The LMX2433SLE Evaluation Board simplifies evaluation of the LMX2433SLE 3.6 GHz/1.7 GHz PLLatinum™ dual frequency synthesizer. The board enables all performance measurements with no additional support circuitry.

The evaluation board consists of a LMX2433SLE device, RF and IF VCO modules, and RF and IF loop filters built by discrete components. The SMA flange mount connectors are provided for external reference input, RF and IF VCO outputs, and the power and grounding connection. A cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of MICROWIRE™ serial port emulation, the CodeLoader software included can be run on a PC to facilitate the LMX2433SLE internal register programming for the evaluation and measurement.

1.1 Quick Start

The LMX2433SLE Evaluation Board is fully assembled and factory tested. Follow the instructions below to set up the hardware platform for the measurement of interest.

1.1.1 Recommended Test Equipment

- Spectrum analyzer with operating frequency range > 3.5 GHz
- DC power supply with adjustable voltage outputs
- 10 MHz signal source/generator. A high quality TCXO is the preferred signal source. Alternatively, the 10 MHz (0 dBm) reference output from the rear panel of the spectrum analyzer may be used.

1.1.2 Connection And Setup

1. Connect the RF_OUT/IF_OUT output port to the input of the spectrum analyzer for phase noise and reference spur measurement or to the input of the modulation domain analyzer for lock time measurement.

2. Connect a 10 MHz reference oscillator to the REF_IN input port. A high quality reference source such as a TCXO is preferred to achieve an accurate and low noise measurement. Depending on the reference source used, the 51Ω terminating resistor, designated R10, can be removed when appropriate. Alternatively, connect a signal generator to the REF_IN input port and set the output frequency to 10 MHz. Keep the 51Ω resistor if the signal generator is used. Another option is to use the 10 MHz reference output from the rear panel of the spectrum analyzer.

3. Plug the DB25 connector end of the cable assembly to the parallel port of the PC. Connect the other end of the cable to the on-board 10 Pin Header, JP2. Refer to Appendix E for more details. Alternatively, refer to the CodeLoader 2 Operating Instructions from National Semiconductor's Wireless Communications website: http://wireless.national.com/.

4. Verify that three jumper blocks are in place so that the RF and IF sides as well as their corresponding VCOs have power to them. Refer to the schematic in Appendix A for proper placement of the jumper blocks.

5. Turn the DC power supply ON and adjust the voltage output to 5.0V. Turn the DC power supply OFF.

6. Connect the DC power supply output to the V_{cc} port of the evaluation board. Turn the DC power supply ON.

7. Run the CodeLoader software for LMX2433SLE register programming. Ensure proper port setup, and that the frequency of the reference source on the CodeLoader matches that actually used for the board. Refer to Appendix E for more details.

2.0 Measurement Considerations

2.1 Phase Noise Measurement Using A Spectrum Analyzer

The phase noise characteristics of the PLL can be measured on a spectrum analyzer or a phase noise test set. The spectrum analyzer test technique is described here. Phase noise is measured in units of dBc/Hz. In this evaluation, the phase noise is measured at 1 kHz offset from the output signal. For accurate close-in phase noise measurements, the offset frequency selected should be inside the loop bandwidth on the flat portion of the curve. For integrated phase noise measurements a phase noise analyzer is recommended.

The CodeLoader software is used to set the desired frequency and to program the LMX2433SLE device. Refer to Appendix E for more details. For phase noise measurements at fixed offset frequencies, use an analyzer with a noise floor below the level of measurement interest. Since they are more readily available, below is an explanation of this test technique using a spectrum analyzer.

Tune the spectrum analyzer to the desired center frequency with the span adjusted to include the appropriate offset frequency. Using the delta marker, the difference between the carrier and the noise level at the desired offset frequency is measured. The video averaging feature of the spectrum analyzer should used to better determine the noise level.

The phase noise is a 1 Hz normalized bandwidth measurement expressed in dBc/Hz. Most modern spectrum analyzers have a feature that automatically normalizes the phase noise measurements to a 1 Hz bandwidth. This feature gives greater measurement accuracy. For spectrum analyzers without this feature, the normalized phase noise is equal to the noise level relative to the carrier minus 10 * log10 [Resolution Bandwidth]. This formula does not take into account any errors from the spectrum analyzer.

2.2 Loop Filter Bandwidth Measurement Using A Spectrum Analyzer

The loop bandwidth is the bandwidth of the closed loop PLL system. It is, by definition, the frequency that makes the forward loop gain equal to zero. The spectrum analyzer span is set to view the characteristic rising, peaking, and falling of the phase noise. To measure the loop bandwidth is rather complex. It is simpler to measure the 0 dB bandwidth. Although, not exactly the same, the 0 dB bandwidth is a sufficient estimate of the loop filter bandwidth. The 0 dB bandwidth is defined as the frequency where the phase noise falls back to the level of the close-in value after rising to its peak value. The value measured is typically greater than the true loop filter bandwidth. For this evaluation, the 0 dB bandwidth is measured.

2.3 Reference Spur Measurement Using A Spectrum Analyzer

The reference sidebands can be seen on a spectrum analyzer and are measured in dBc. The CodeLoader software is used to set the desired frequency and to program the LMX2433SLE device. Refer to Appendix E for more details. The spectrum analyzer is set to the desired center frequency and the span is set to allow the reference sidebands to be viewed. For the LMX2433SLE device, the span can be set to 7 MHz during the RF or IF VCO measurements because their loop filter designs are based on a 2.5 MHz reference frequency. The spurious output is the difference between the level of the VCO output frequency tone and the level of the spur at an offset equal to the carrier frequency +/- the reference frequency. For a more accurate account of the device's spurious performance, the reference spurs across the VCO's frequency band should be determined. The worst-case spur is typically defined as the PLL's spur performance.

2.4 Lock Time Measurement Using A Modulation Domain Analyzer

The modulation domain analyzer measures the switching speed, or lock time, using a frequency versus time plot. The modulation domain analyzer was used for the IF lock time measurement.

Set the center frequency of the modulation domain analyzer to the final (settling) frequency. Use a wide span allows viewing of the entire positive or negative switching waveform. Use a narrower span to evaluate the settling waveform within +/- 1 kHz. A trigger condition, typically a latch enable pulse, specifies the event that will cause the modulation domain analyzer to capture and display the measurement results. The lock time is the time difference between the point the frequency starts to change (T1), and the point the VCO frequency settles to within +/-1 kHz of the final value (T2), (i.e. lock time = T2 – T1).

Use the BurstMode tab of the CodeLoader software to program the device to toggle between a desired minimum and maximum frequency. It is necessary to include a sufficient delay, such as 100000, after each programming command. For more detail, refer to the BurstMode Tab section in the CodeLoader 2 Operating Instructions from National Semiconductor's Wireless Communications website: http://wireless.national.com/.

2.5 Lock Time Measurement Using A Spectrum Analyzer

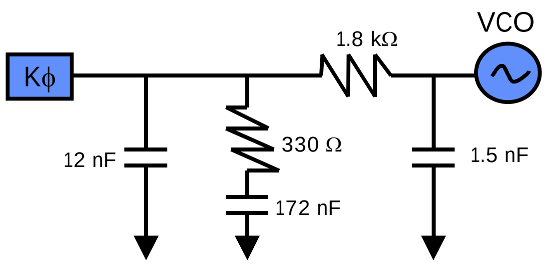
The principle behind this is to use the spectrum analyzer as an FM demodulator to detect the frequency change over time when the PLL is switching between two frequencies. This method is called the Zero-Span mode. The idea is to convert the FM of the signal to amplitude variations and then measure these variations over time. The center frequency of the spectrum analyzer is first set to the final (settling) frequency. The frequency span and resolution bandwidth are both set to 10 kHz, and the video bandwidth is set to 100 kHz. The scale is set to 2 dB per division and the step size is set to 1 kHz per division. A filter response is displayed. The spectrum analyzer is tuned off the center frequency so that the slope of the tunable filter is used as an FM to AM converter. The linear section (slope) of the filter is at 5 kHz from the center frequency. The slope is approximately 1 dB/ 1 kHz. The frequency span is finally set to 0 Hz. A sweep time of 30 msec is used.

A x1 probe is used to connect the MICROWIRE to the external trigger on the rear panel of the spectrum analyzer. Using the CodeLoader software, port address 'C1' is selected for the TRIGGER programming pin. The TRIGGER is then set to HIGH. Using the Burst Mode menu of the software, a macro is created to program the LMX2433SLE device to switch between the maximum and minimum frequency alternately over time. It is necessary to include a sufficient delay, such as 10000000, after each programming command. Refer to the Burst Mode Tab section in the CodeLoader 2 Operating Instructions from National Semiconductor's Wireless Communications website: http://wireless.national.com/. The lock time is the time difference between the point the frequency starts to change (T1), and the point the PLL frequency settles within +/- 1 kHz range (T2), i.e. lock time = T2 – T1. The single sweep feature of the spectrum analyzer can be used to capture the trace. (+/- 1 kHz tolerance corresponds to +/- 1 dB from the settling frequency).

Due to a maximum frequency range specification of 2.5GHz, the modulation domain analyzer cannot be used for the RF lock time measurement. Do to component tolerances, the maximum of some Vail 690-3300T VCOs used will not reach 3270 MHz with a tuning voltage of 2.0V. The 2.0V is 0.5V below the Vcc (3.0V) supply, which is the minimum delta specification in the datasheet. Figure 4.1.6 and 4.1.7 shows lock times to and from 3270 MHz. On instances where VCO does not reach 3270 MHz, use 3250 MHz for the maximum frequency. Other than the frequency the waveform should be the same as shown in Figure 4.1.6.

3.0 Evaluation Board Configuration

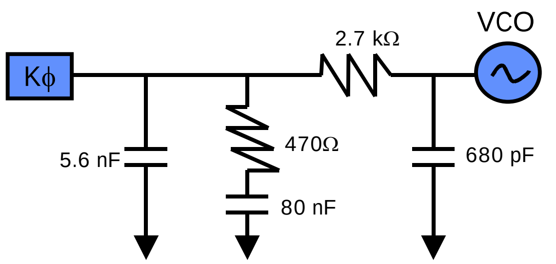
3.1 RF PLL Loop Filter Parameters



Settings For Operation	
Charge Pump Gain ($K\phi$)	4 mA (HIGH Gain)
Comparison Frequency (f_{compRF})	2500 kHz
Output Frequency (f_{FinRF})	3120 - 3250 MHz
VCO Supply	5.0V
Other Information	
VCO Used	VARI-L VCO690-3300T
VCO Gain	90 MHz/V
VCO Input Capacitance	22 pF

Figure (3.1)

3.2 IF PLL Loop Filter Parameters



Settings For Operation	
Charge Pump Gain ($K\phi$)	4 mA (HIGH Gain)
Comparison Frequency (f_{compIF})	2500 kHz
Output Frequency (f_{FinIF})	1530 – 1600 MHz
VCO Supply	5.0V
Other Information	
VCO Used	VARI-L VCO190-1650T
VCO Gain	32 MHz/V
VCO Input Capacitance	39 pF

Figure (3.2)

4.0 Typical Performance Measurements

The LMX2433SLE Evaluation Board has been tested to meet the typical performance criteria as shown below:

Evaluation Conditions:

V_{cc} Operating Voltage	2.50V
TCXO Frequency	10 MHz
RF VCO Tuning Range	3120 - 3250 MHz
RF Comparison Frequency	2500 kHz
IF VCO Tuning Range	1530 - 1600 MHz
IF Comparison Frequency	2500 kHz

Typical Performance Criteria:

RF PLL Phase Noise	< -83 dBc/Hz At 1 kHz Offset
RF PLL Reference Spur	< -80 dBc At 2500 kHz Offset
RF PLL Lock Time	< 1.1 ms (Within +/- 1kHz Settling Frequency)
IF PLL Phase Noise	< -88 dBc/Hz At 1 kHz Offset
IF PLL Reference Spur	< -73 dBc At 2500 kHz Offset
IF PLL Lock Time	< 550 μs (Within +/- 1kHz Settling Frequency)

Remark

Computer monitors and other lab equipment have been shown to cause noise spikes. If noise spikes are observed on the signal, try turning off the monitor or other equipment to verify that they are not the cause. In addition, noise may be getting onto the signal through the cable that connects to the parallel port of the computer.

4.1 RF PLL Typical Performance Measurements

RF PLL Phase Noise at 3.200 GHz at 1.0 kHz Offset = -85.0 dBc/Hz

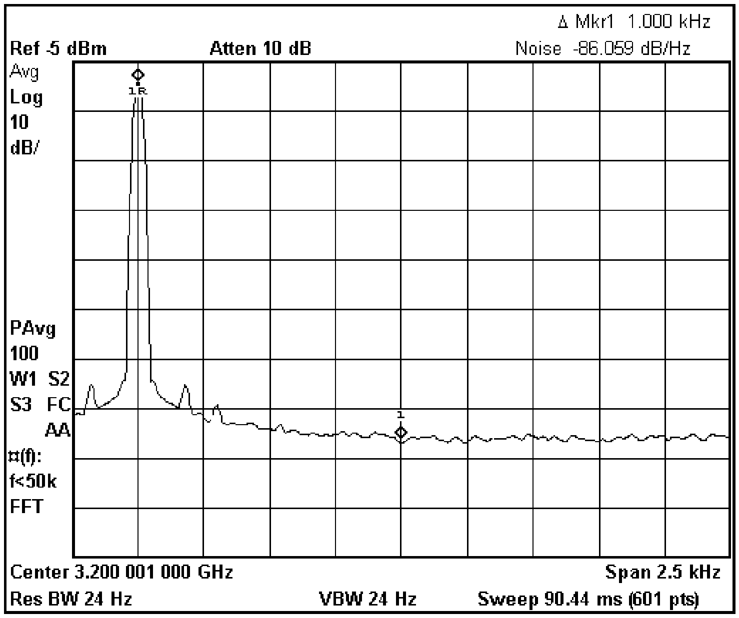


Figure (4.1.1)

RF PLL Loop Filter Bandwidth (≈15.0 kHz)

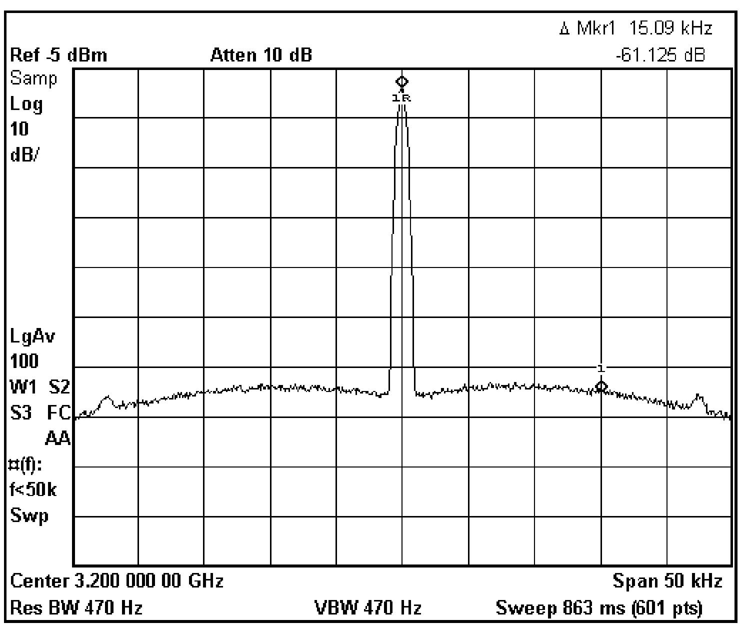


Figure (4.1.2)

RF PLL Reference Spurs at 3.120 GHz at 2.5 MHz Offset < -84.6 dBc

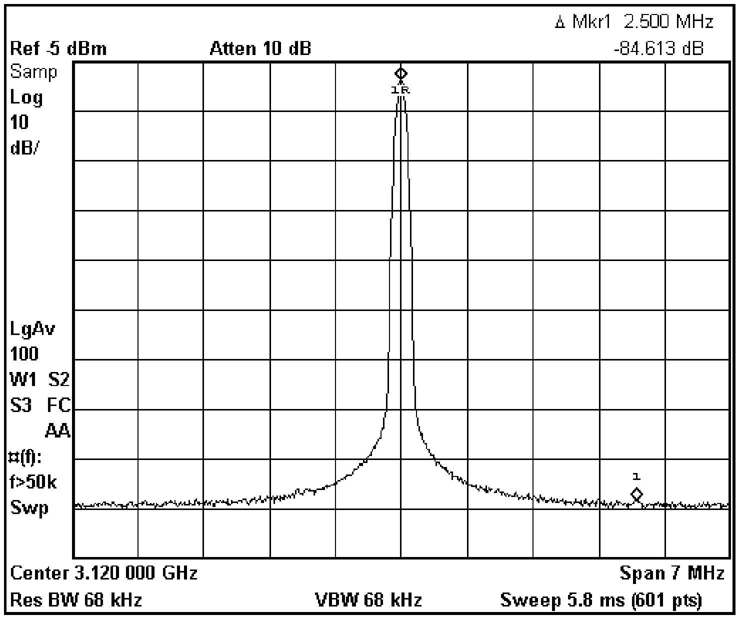


Figure (4.1.3)

RF PLL Reference Spurs at 3.200 GHz at 2.5 MHz Offset < -84.8 dBc

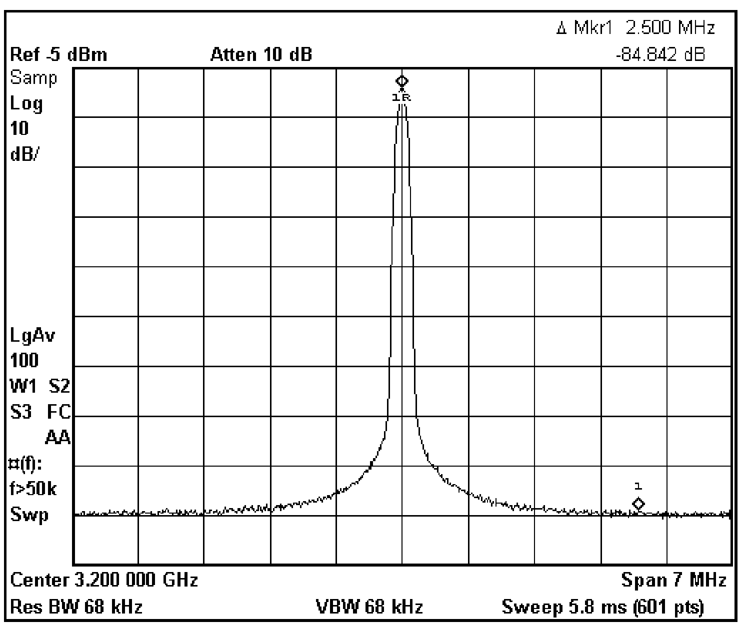


Figure (4.1.4)

RF PLL Reference Spurs at 3.250 GHz at 2.5 MHz Offset < -83.3 dBc

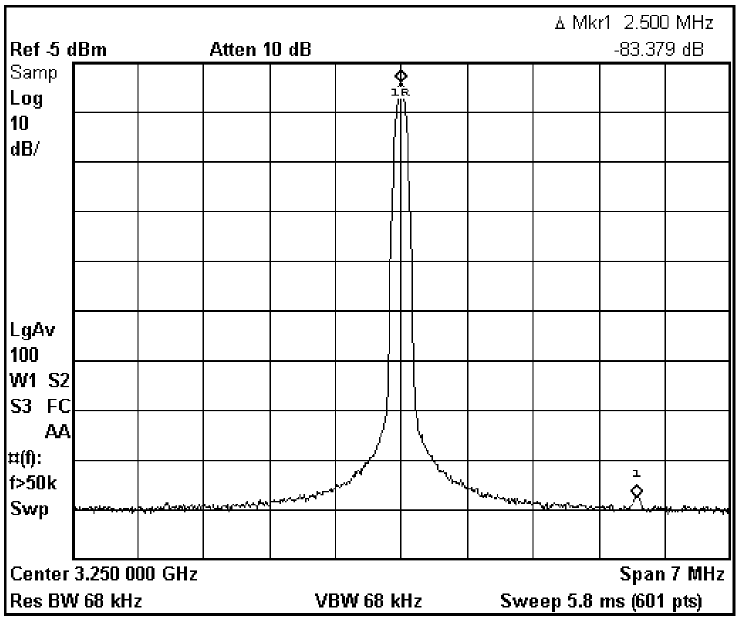


Figure (4.1.5)

RF PLL Positive Frequency Switching Waveform

3.120 GHz to 3.270 GHz Lock Time (+/- 1kHz < 870.0 µs)

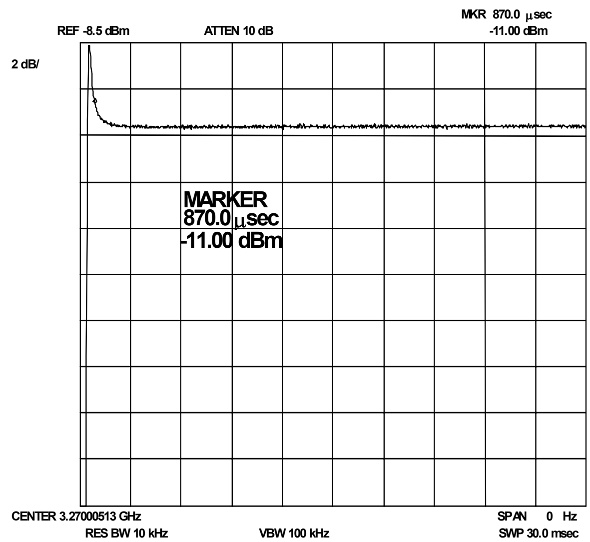


Figure (4.1.6)

RF PLL Negative Frequency Switching Waveform

3.270 GHz to 3.120 GHz Lock Time (+/-1 kHz < 1.050 ms)

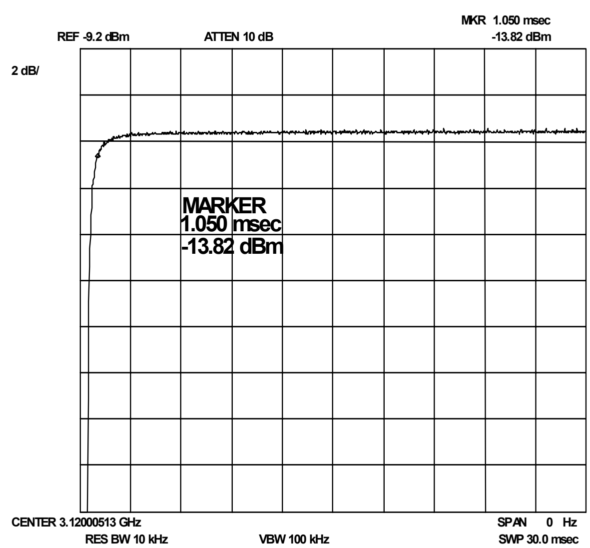


Figure (4.1.7)

4.2 IF PLL Typical Performance Measurements

IF PLL Phase Noise at 1.565 GHz at 1.0 kHz Offset = -90.4 dBc/Hz

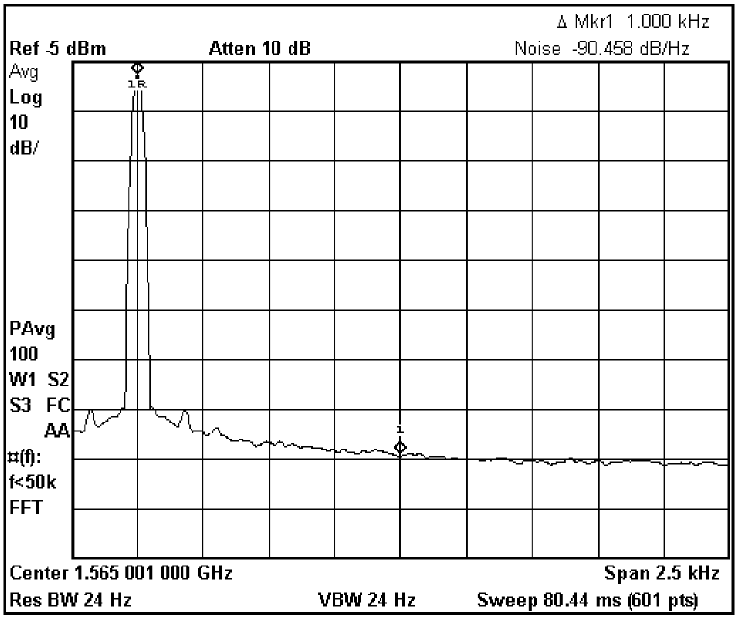


Figure (4.2.1)

IF PLL Loop Filter Bandwidth (≈26.00 kHz)

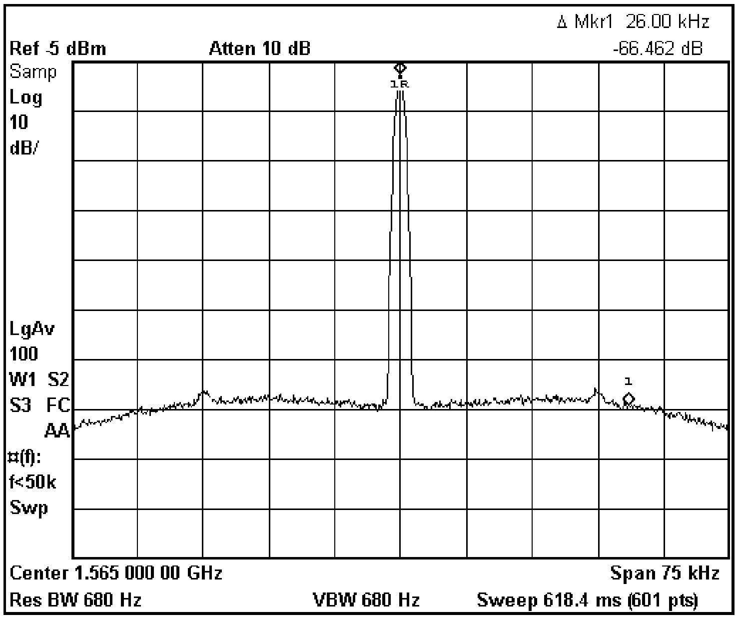


Figure (4.2.2)

IF PLL Reference Spurs at 1.530 GHz at 2.5 MHz Offset < -79.2 dBc

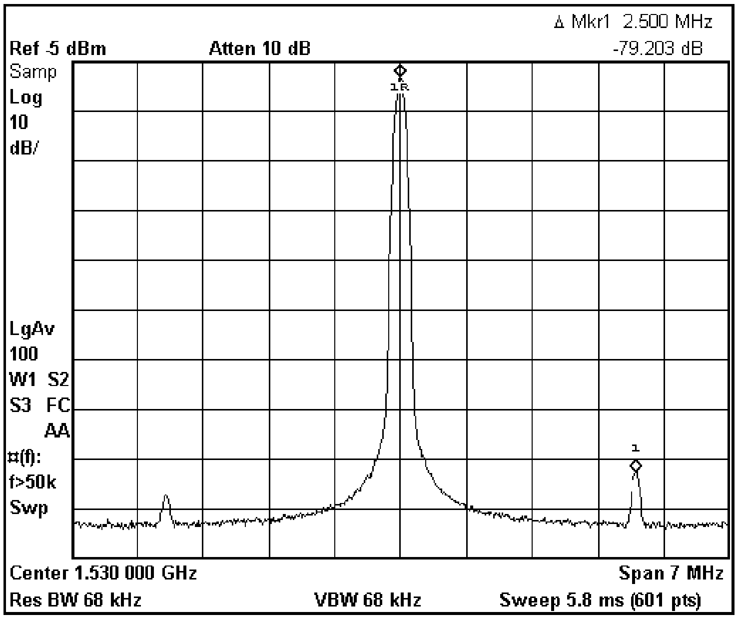


Figure (4.2.3)

IF PLL Reference Spurs at 1.565 GHz at 2.5 MHz Offset < 90.5 dBc

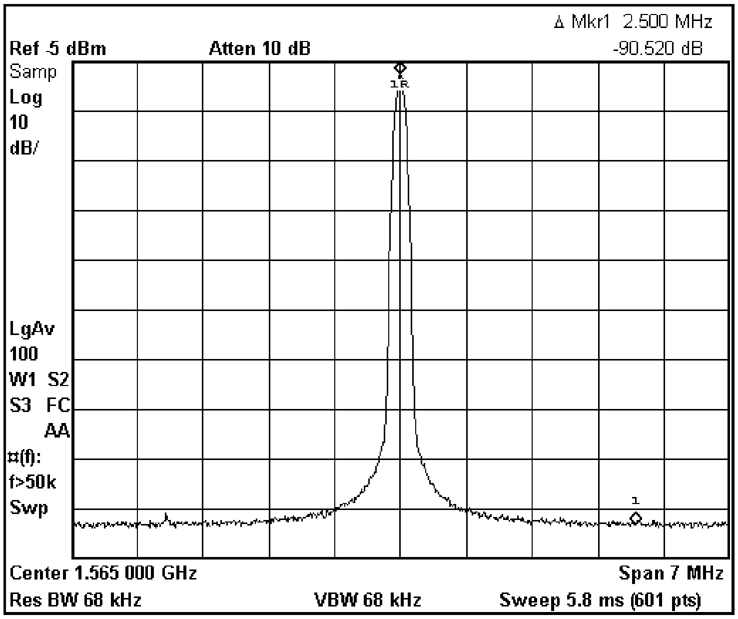


Figure (4.2.4)

IF PLL Reference Spurs at 1.600 GHz at 2.5 MHz Offset < -90.7 dBc

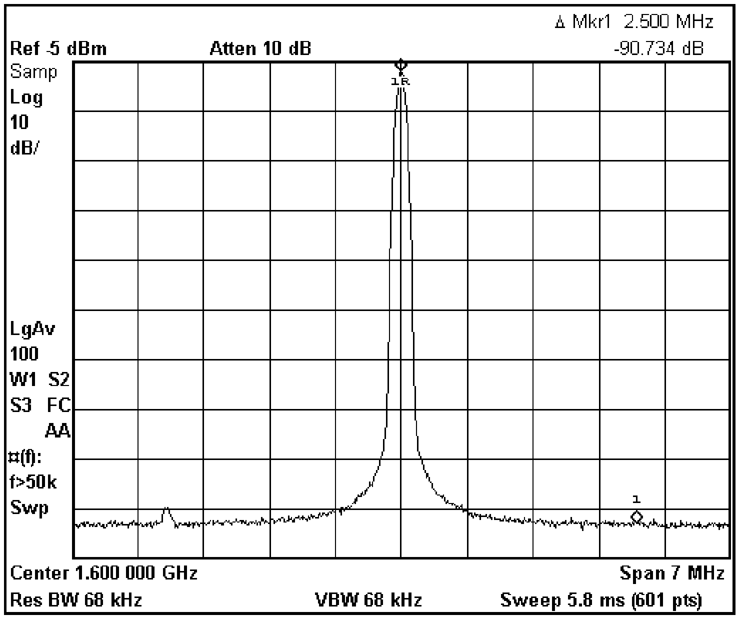


Figure (4.2.5)

IF PLL Positive Lock Time Waveform Using HP53310A Modulation Domain Analyzer

1.530 GHz to 1.600 GHz Lock Time (+/- 1kHz - 463 μs)

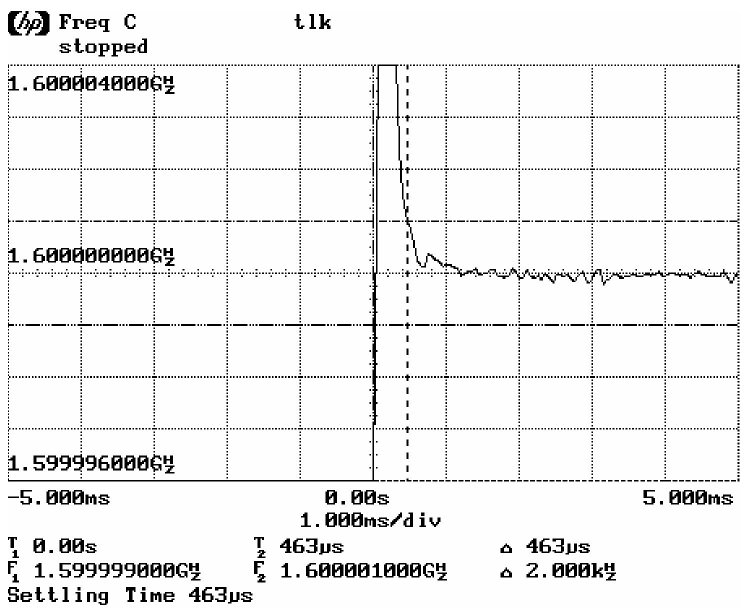


Figure (4.2.6)

IF PLL Negative Lock Time Waveform Using HP53310A Modulation Domain Analyzer

1.600 GHz to 1.530 GHz Lock Time (+/- 1kHz - 513 μs)

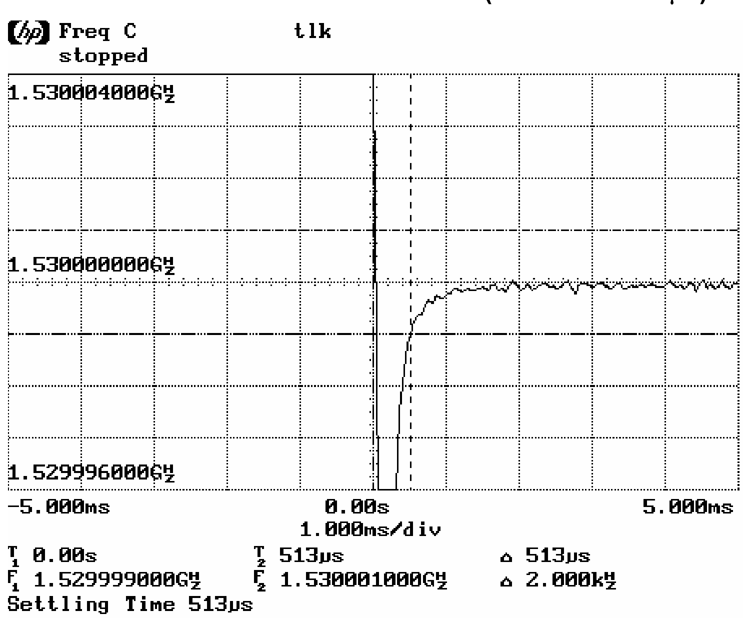


Figure (4.2.7)

APPENDIX A:

LMX2433SLE Evaluation Board Schematic

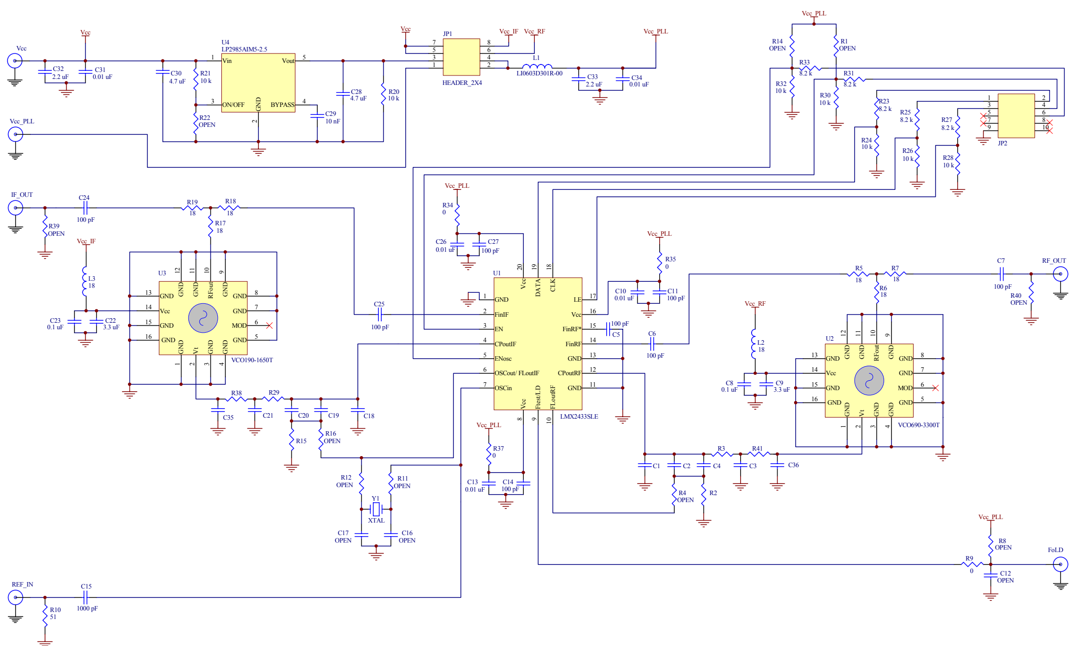


Figure (A.1)

Note:

1. All jumpers are placed for the default configuration of the board (JP2 requires 3 jumpers: 3-4, 5-6, 7-8)

APPENDIX B:

LMX2433SLE Evaluation Board – Board Layout

Top Layer

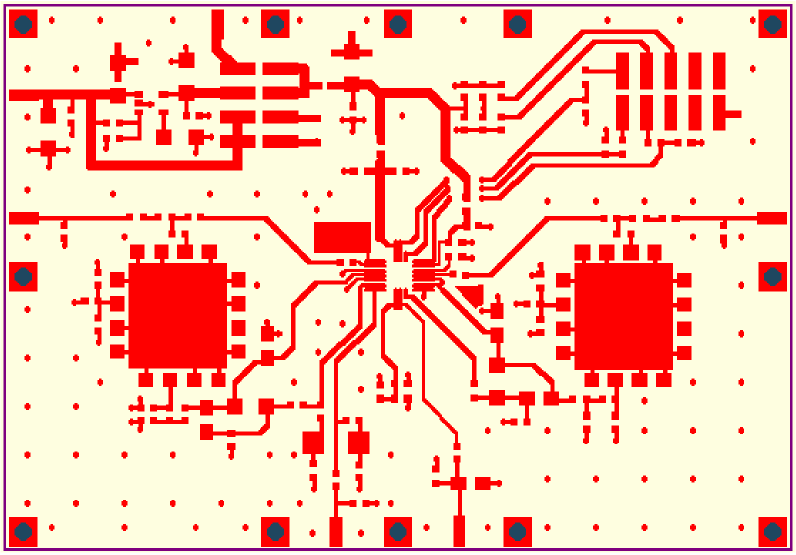


Figure (B.1)

MidLayer1

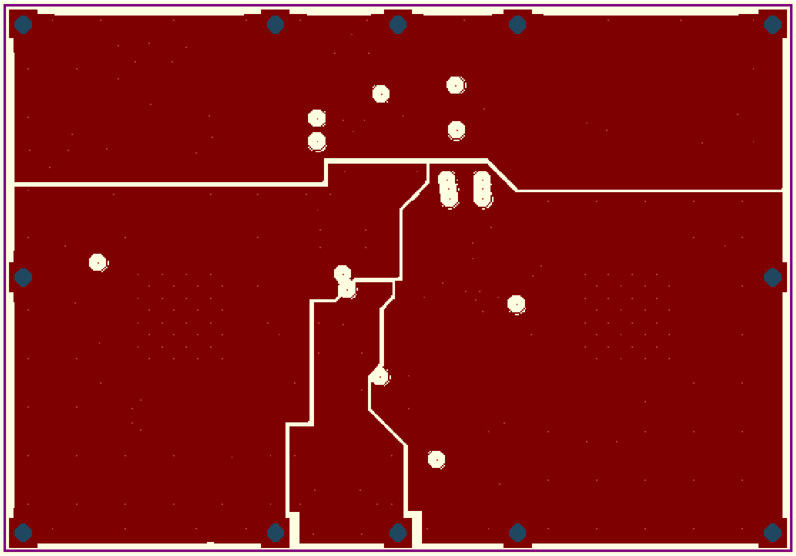


Figure (B.2)

MidLayer2

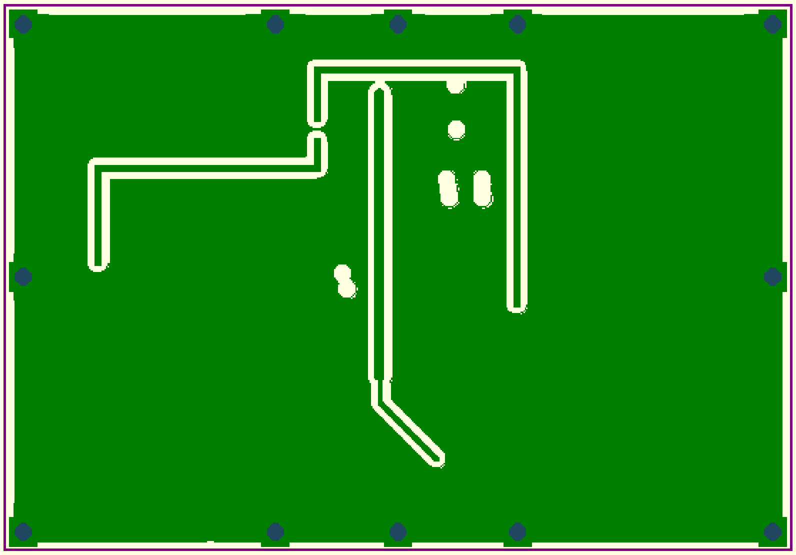


Figure (B.3)

Bottom Layer

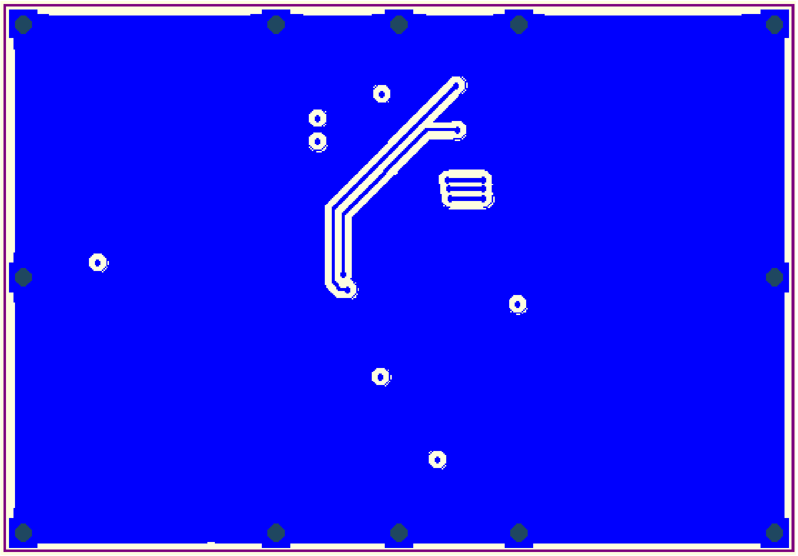


Figure (B.4)

APPENDIX C:

LMX2433SLE Evaluation Board – Bill Of Materials

ITEM #	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS	PREFERRED VENDOR
1	18	N/A	OPEN, NO COMPONENT	R1, R4, R8, R11, R12, R14, R16, R22, R39, R40, C12, C16, C17, C35, C36, Y1, Vcc_PLL, FoLD	N/A
2	8	C0603C101J5GAC	CAP, 100 pF, CERAMIC, 5%, NP0, 0603	C5, C6, C7, C11, C14, C24, C25, C27	KEMET
3	1	C0603C681J3GAC	CAP, 680 pF, CERAMIC, 5%, NP0, 0603	C21	KEMET
4	1	C0603C102J3GAC	CAP, 1000 pF, CERAMIC, 5%, NP0, 0603	C15	KEMET
5	1	C0603C152J5RAC	CAP, 1500 pF, CERAMIC, 5%, X7R, 0603	C3	KEMET
6	1	C0805C562J5RAC	CAP, 5600 pF, CERAMIC, 5%, X7R, 0805	C18	KEMET
7	5	C0603C103J5RAC	CAP, 0.01 μF, CERAMIC, 5%, X7R, 0603	C10, C13, C26, C31, C34	KEMET
8	1	C1206C103J3GAC	CAP, 0.01 μF, CERAMIC, 5%, NP0, 1206	C29	KEMET
9	1	C0805C123J5RAC	CAP, 0.012 μF, CERAMIC, 5%, X7R, 0805	C1	KEMET
10	1	C0805C223J5RAC	CAP, 0.022 μF, CERAMIC, 5%, X7R, 0805	C2	KEMET
11	1	C0805C333J5RAC	CAP, 0.033 μF, CERAMIC, 5%, X7R, 0805	C19	KEMET
12	1	C1206C473J5RAC	CAP, 0.047 μF, CERAMIC, 5%, X7R, 1206	C20	KEMET
13	2	C0603C104J3RAC	CAP, 0.1 μF, CERAMIC, 5%, X7R, 0603	C8, C23	KEMET
14	1	ECP-U1C154MA5	CAP, 0.15 μF, FILM, 20%, 1206	C4	PANASONIC
15	2	C1206C225J8RAC	CAP, 2.2 μF, CERAMIC, 5%, X7R, 1206	C32, C33	KEMET
16	2	GMC21Y5V335Z16NE	CAP, 3.3 μF, CERAMIC, 20%, Y5V, 0805	C9, C22	CAL CHIP
17	2	C1206C475K4PAC	CAP, 4.7 μF, CERAMIC, 10%, X5R, 1206	C28, C30	KEMET
18	6	CRCW0603000ZRT1	RES, 0Ω, 0603	R9, R34, R35, R37, R38, R41	VISHAY
19	8	CRCW0603180JRT1	RES, 18Ω, 5%, 0603	R5, R6, R7, R17, R18, R19, L2, L3	VISHAY
20	1	CRCW0603510JRT1	RES, 51Ω, 5%, 0603	R10	VISHAY
21	1	CRCW0603331JRT1	RES, 330Ω, 5%, 0603	R2	VISHAY
22	1	CRCW0603471JRT1	RES, 470Ω, 5%, 0603	R15	VISHAY
23	1	CRCW0603182JRT1	RES, 1.8 kΩ, 5%, 0603	R3	VISHAY
24	1	CRCW0603272JRT1	RES, 2.7 kΩ, 5%, 0603	R29	VISHAY
25	5	RMC 1/16 8.2K 1% R	RES, 8.2 kΩ, 1%, 0603	R23, R25, R27, R31, R33	SEI
26	7	RMC 1/16 10.0K 1% R	RES, 10 kΩ, 1%, 0603	R20, R21, R24, R26, R28, R30, R32	SEI
27	1	LI0603D301R-00	FERRITE BEAD, 300Ω, 0603	L1	STEWARD
28	4	5762SF	CONNECTOR, SMA, 50 Ω	Vcc, RF_OUT, IF_OUT, REF_IN	CDI
29	3	CCIJ255G	SHUNT, 0.100" CENTER, CLOSED TOP		COMM CON CONNECTORS
30	1	HTSM3203-8G2	HEADER, 8 PIN	JP1	COMM CON CONNECTORS
31	1	HTSM3203-10G2	HEADER, 10 PIN	JP2	COMM CON CONNECTORS
32	1	LMX2433SLE	IC, PLL	U1	NATIONAL SEMICONDUCTOR
33	1	LMX2434SLEEBPCB	PCB		NATIONAL SEMICONDUCTOR
34	1	LP2985AIM5-2.5	REGULATOR, SOT2-3	U4	NATIONAL SEMICONDUCTOR
35	1	VCO190-1650T	VCO	U3	VARI-L
36	1	VCO690-3300T	VCO	U2	VARI-L
37	1	LMXOGTSP	FRAME, 2.25" x 3.25"		LUX MANUFACTURING
38	8	OF12SHCA	SCREW, 0-80x1/8		ORLANDER INC
39	12	2C18PPMZZ	SCREW, 2-56x3/16, PHILIPS, PAN-HEAD		ORLANDER INC

APPENDIX D:

LMX2433SLE Evaluation Board – Build Diagram

Top Layer (Top View)

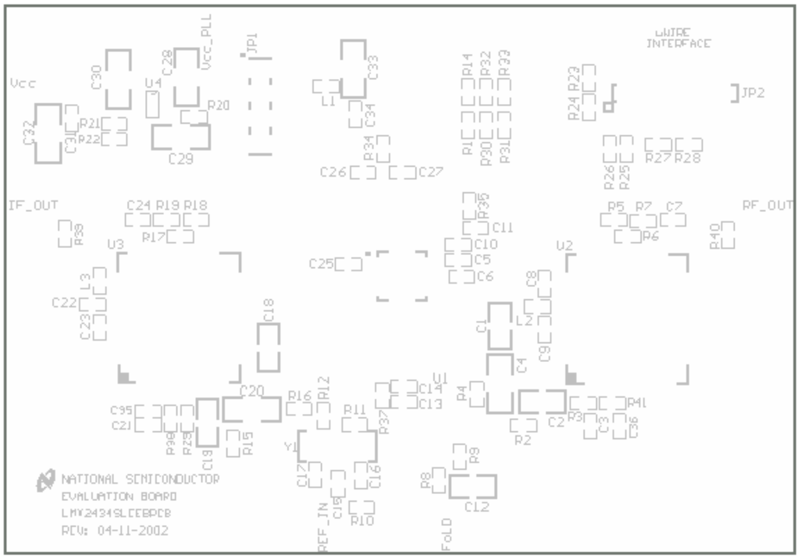


Figure (D.1)

Bottom Layer – No Components

APPENDIX E:

LMX2433SLE How To Setup The CodeLoader Software

The port setup is necessary to tell the CodeLoader program which signals to send to which locations on the computer parallel port. The proper setup for this part is shown below. The *Bits/Pins* page controls special functions in the PLL. For the LMX2433SLE, these special functions include the Timeout Counter bits, Power Control bits, and the operation of the EN, ENosc, and Ftest/LD pins.

Proper Port Setup

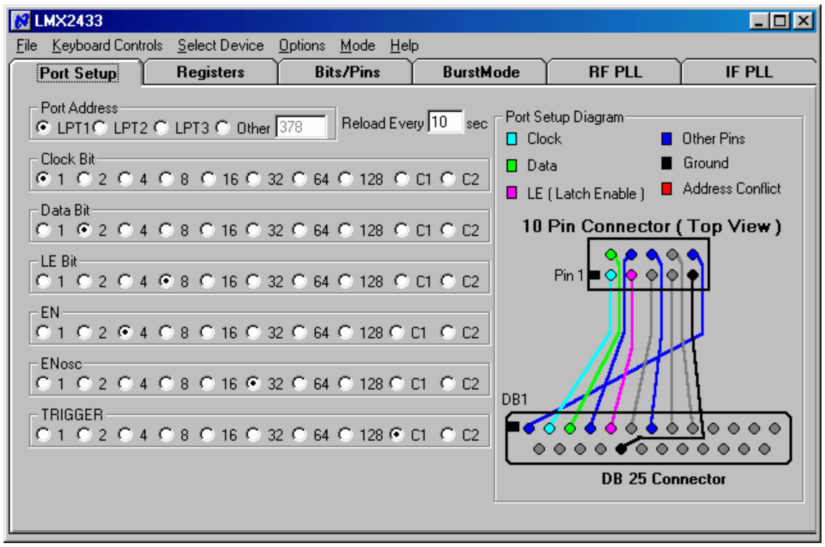


Figure (E.1)

Port Setup And Corresponding PC Parallel Port And 10-Pin Header Configuration

Port Setup Name	Port Setup Column	DB25 Connector Pin	10-Pin Header Pin
1	1	DB2	1
2	2	DB3	2
4	3	DB4	4
8	4	DB5	3
16	5	DB6	5
32	6	DB7	6
64	7	DB8	7
128	8	DB9	8
C1	9	DB1	10
C2	10	DB25	Not Used
N/A	N/A	18 (Ground)	9

Figure (E.2)

Pin 1 Position For PC Parallel Port And 10-Pin Header

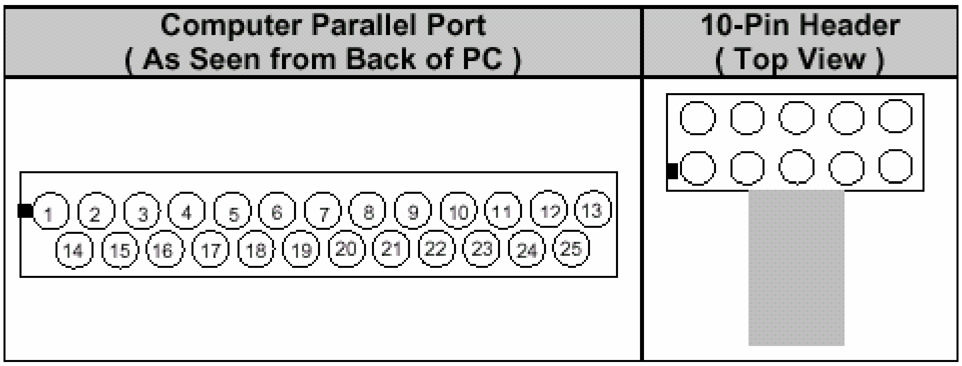


Figure (E.3)

Default *Bits/Pins* Setup

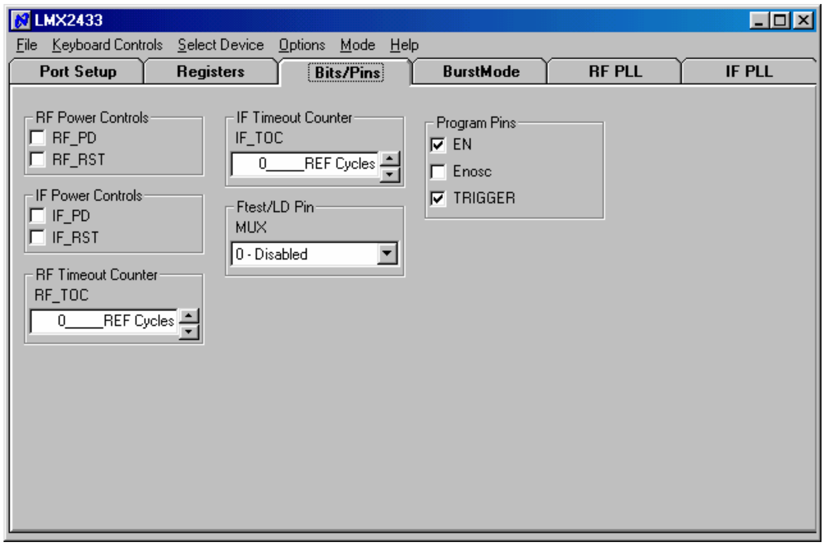


Figure (E.4)

RF PLL Default Setup

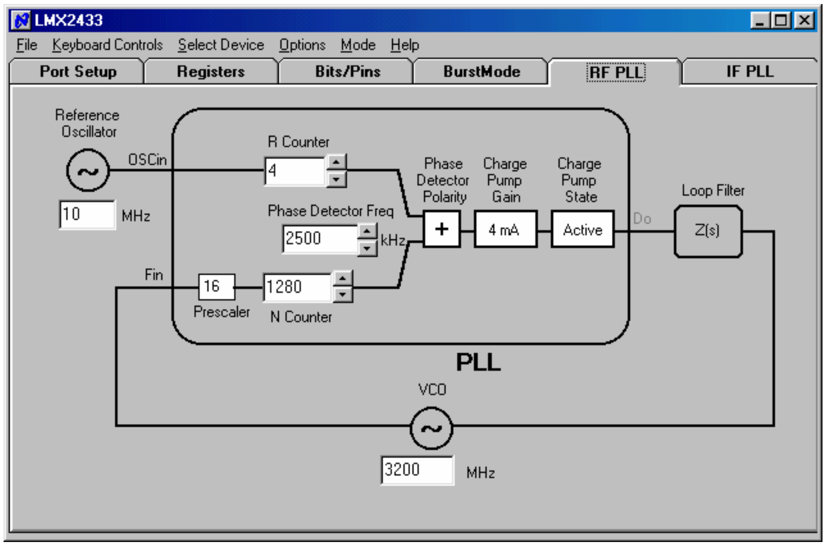


Figure (E.5)

IF PLL Default Setup

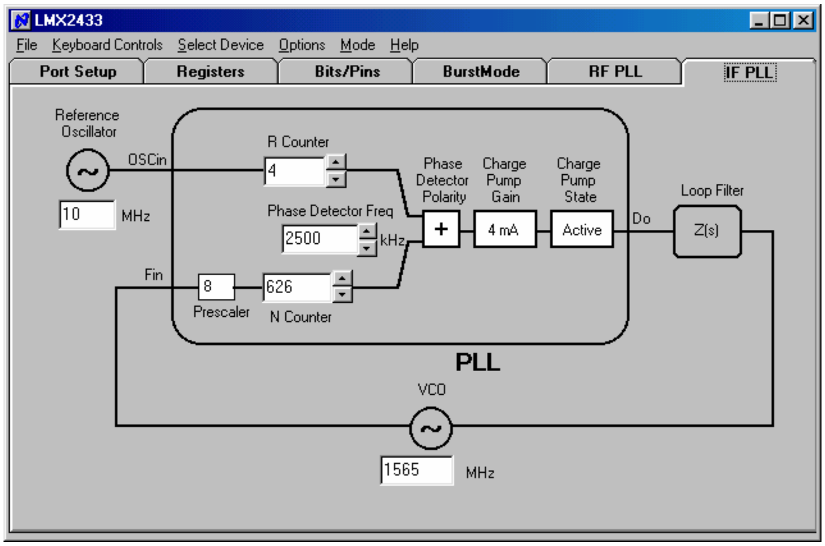


Figure (E.6)