LVDS Flow Through Evaluation Boards

LVDS47/48EVK Revision 1.0

January 2000

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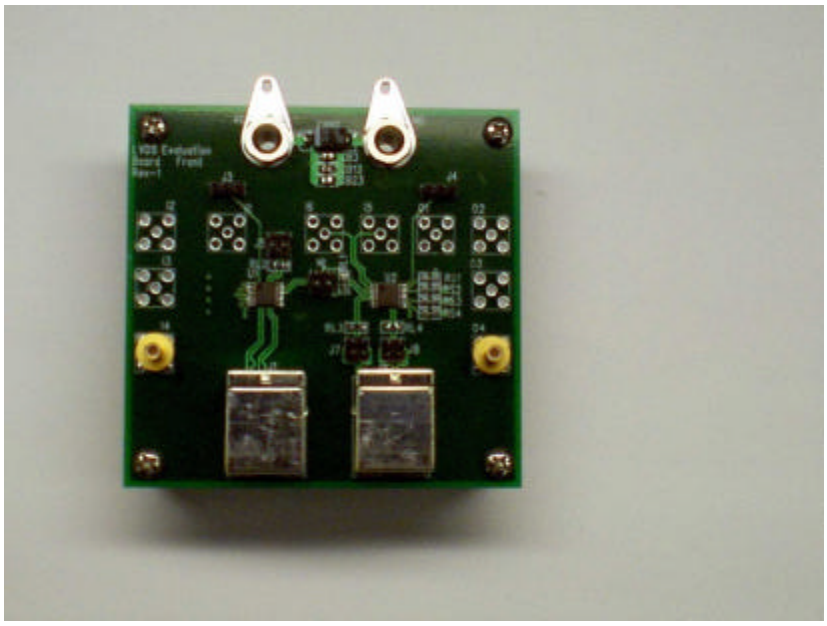
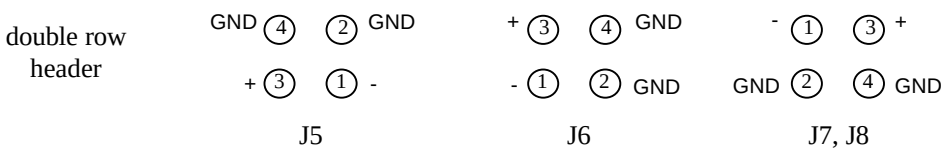


The Flow Through LVDS Evaluation Board

The Flow Through LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over a PCB trace, RJ45 connector and CAT5 UTP cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the standard LVDS I/O characteristics of most of National's LVDS devices. We can also use the DS90LV047A/048A to represent the LVDS I/O characteristics of 3V Channel Link and 3V FPD-Link devices.

6.1.1 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of RJ45 cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation kit is LVDS47/48EVK. In this application note, the following differential signal nomenclature has been used: "Jx-3" represents the true signal and "Jx-1" represents the inverting signal. On the PCB, the true signal is represented by a '+' and the inverting signal is on the adjacent header pin as shown below.



The two adjacent ground pins are there to view the true or inverting signal single-endedly. Input signals are represented with an "I" while receiver outputs are represented with an "O."

6.1.2 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately. The five test cases are shown in *Figure 1*.

LVDS Channel # 1A: LVDS Line Driver

This test channel provides test points for an isolated driver with a standard 100 Ohm differential termination load. Probe access for the driver outputs is provided at test points on J5-1 and J5-3. The driver input signal (I1) is terminated with a 50 Ohm termination resistor (RT1) on the bottom side of the PCB.

LVDS Channel # 1B: LVDS Receiver

This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either two separate 50 Ohm terminations (RT5 and RT6) (each line to ground) or a 100 Ohm resistor connected across the inputs (differential). The first option allows for a standard signal generator interface. Input signals are connected at test points I5 (R_{IN-}) and I6 (R_{IN+}). A PCB option for a series 453 Ohm resistor (RS1) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is with two separate 50 Ohm terminations (RT5 and RT6) and without the series 453 Ohm resistor (RS1) for use of high impedance probes. The receiver output signal may be probed at test point O1.

LVDS Channel # 2: PCB Interconnect

This test channel connects Driver #2 to Receiver #2 via a pure PCB interconnect. A test point interface of the LVDS signaling is provided at test point J6-1 and J6-3. The driver input signal (I2) is terminated with a 50 Ohm termination resistor (RT2) on the bottom side of the PCB. The receiver output signal may be probed at test point O2. A PCB option for a series 453 Ohm resistor (RS2) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is without the series 453 Ohm resistor for use of high impedance probes. A direct probe connection is possible with a TEK P6247 differential probe high impedance probe (>1GHz bandwidth) on the LVDS signals at test points J6-1 and J6-3. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel # 3: Cable Interconnect

This test channel connects Driver #3 to Receiver #3 via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I3) is terminated with a 50 Ohm termination resistor (RT3) on the bottom side of the PCB. LVDS signals are probed via test points on J7. The receiver output signal may be probed at test point O3. A PCB option for a series 453 Ohm resistor (RS3) is also provided in case 50 Ohm probes are employed on the receiver output signal (see options section). The default setting is without the series 453 Ohm resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1GHz bandwidth) on the LVDS signals at test point J7-1 and J7-3.

LVDS Channel # 4: Cable Interconnect

This test channel connects Driver #4 to Receiver #4 also via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I4) is terminated with a 50 Ohm termination resistor (RT4) on the bottom side of the PCB. LVDS signals are probed via test points on J8. The receiver output signal may be probed at test point O4. A PCB option for a series 453 Ohm resistor (RS4) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is without the series 453 Ohm resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1 GHz bandwidth) on the LVDS signals at test point J8-1 and J8-3. This channel duplicates channel #3 so that it may be used for a clock function or for cable crosstalk measurements.

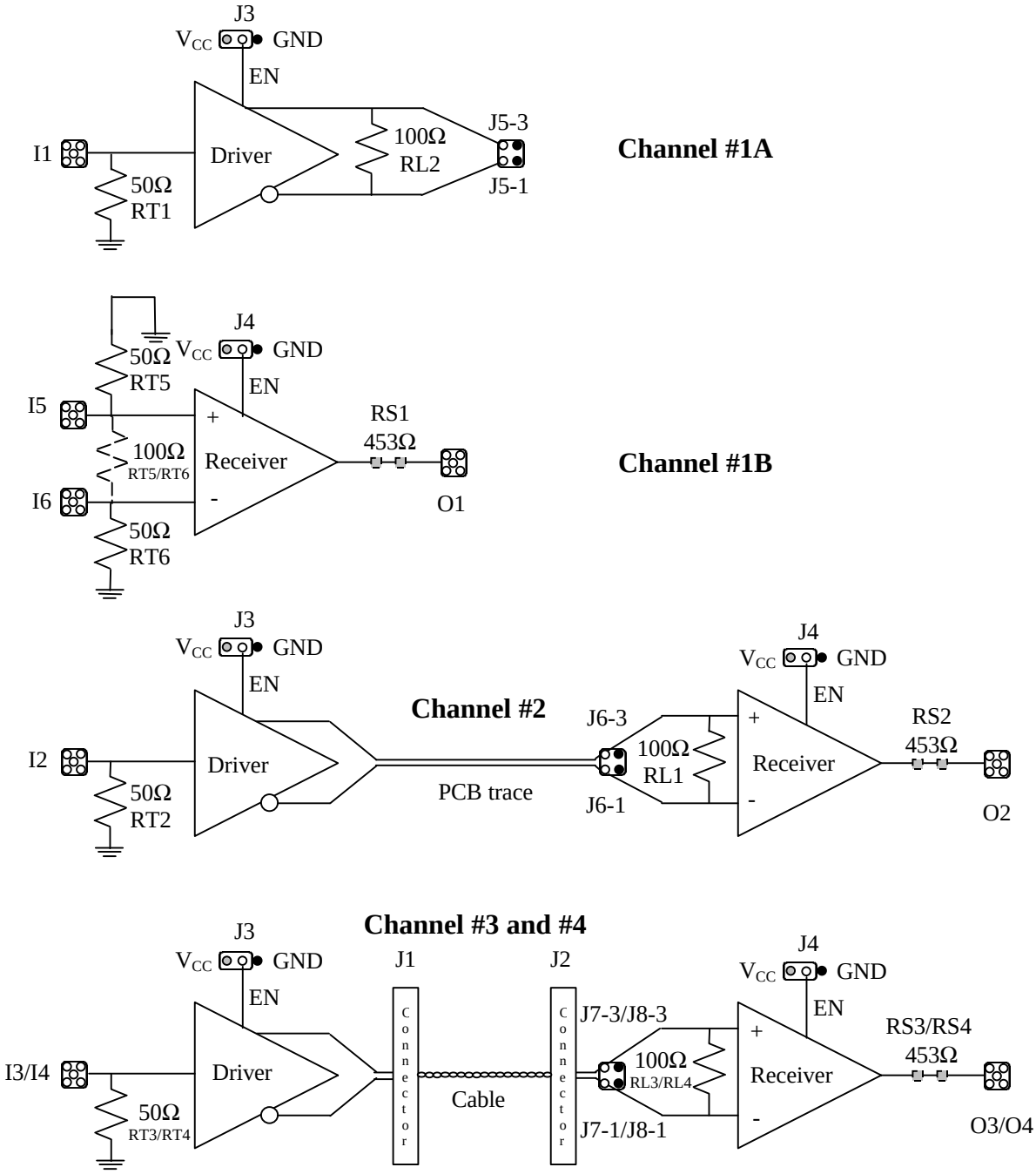


Figure 1: PCB Block Diagram

6.1.3 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a CAT 5 four twisted pair (8-pin) RJ45 cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the Ethernet standard and the cable is widely available. The connector is 8 position, with 0.10 centers and the pairs are pinned out up and down. For example pair 1 is on pins 1 and 5, not pins 1 and 2 (see *Figure 2*).

IMPORTANT NOTE: The 2 unused pairs are connected to ground. Other cables may also be used if they are built up.

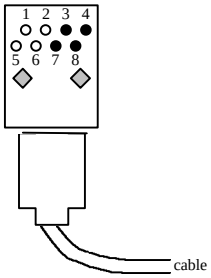


Figure 2: RJ45 Connector

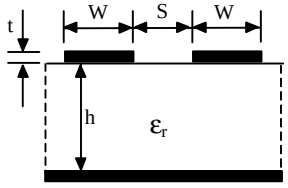
6.1.4 PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal.

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, refer to PCB layout between U1 and J1). Employing differential traces will ensure a low emission design and maximum common mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common mode. Also by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable's differential characteristic impedance). Equations for calculating differential impedance are contained in National application note AN-905 for both microstrip and stripline differential PCB traces.

For the microstrip line, the differential impedance, Z_{diff}, is:

$$Z_{diff} \cong 2Z_O (1 - 0.48e^{-0.96s/h}) \text{ Ohms}$$



For the new evaluation board h = 24 mils, s = 11mils and Z_O = 70 Ohms. Calculating the differential impedance, Z_{diff}, is:

$$Z_{diff} \cong 2Z_O (1 - 0.48e^{-0.96(11/24)}) \text{ Ohms}$$

$$2 (70) (0.69086) \text{ Ohms}$$

$$96.72 \text{ Ohms}$$

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor minimizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13 mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match, the higher the signal fidelity and the less common mode reflections will occur (lower emissions too). A typical value is 100 Ohms ±1%.

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

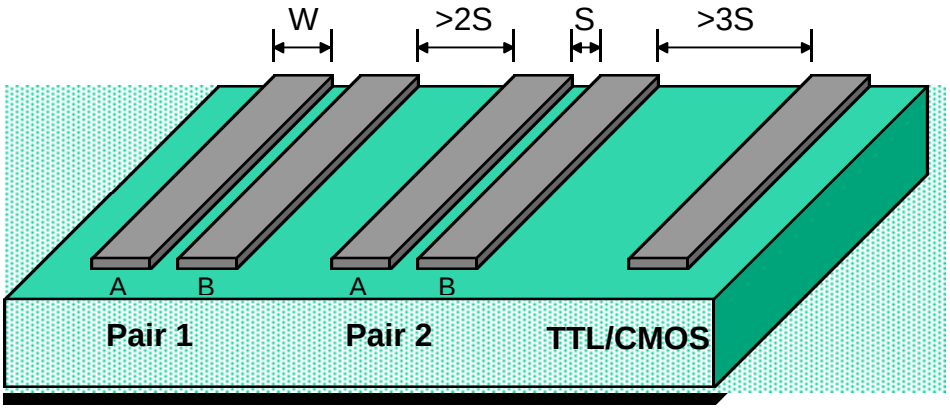


Figure 3: Pair Spacing for Differential Lines

Bypassing capacitors are recommended for each package. A 0.1 µF is sufficient on the quad driver or receiver device (CB1 and CB2) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB21 and CB22) if desired. Traces connecting V_{CC} and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB3, CB13, and CB23 if desired.

6.1.5 Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals have a V_{OD} specification of 250mV to 450mV with a typical V_{OS} of 1.2V. Our devices have a typical V_{OD} of 300mV, but for the example below, we will use a signal between 1.0 V (V_{OL}) and 1.4 V (V_{OH}) for a 400 mV V_{OD}. The differential waveform is constructed by subtracting the Jx-1 (inverting) signal from the Jx-3 (true) signal. V_{OD} = (Jx-3) – (Jx-1). The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in *Figure 4.*

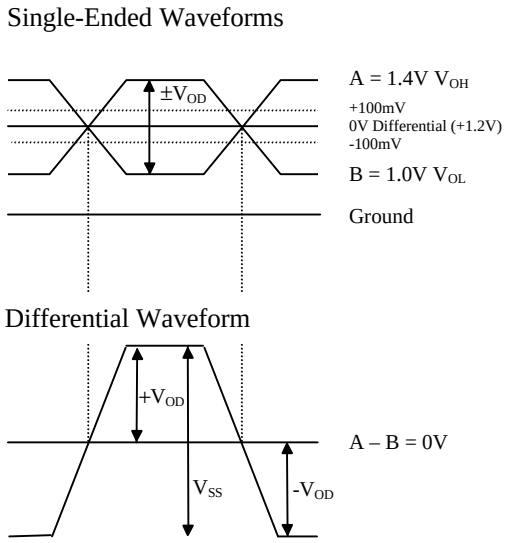


Figure 4: Single-ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #2) can be measured at the receiver inputs (test points J6-1 and J6-3). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See *Figure 5*. Note that the data rate is 100 Mbps and the differential waveform ($V_{DIFF} = D_{OUT2+} - D_{OUT2-}$) shows fast transition times with little distortion.

In *Figure 5, 6, 7* and *8*, the top two waveforms are the single-ended outputs (between the driver and receiver), the middle waveform is the calculated differential output signal from the two single-ended signals and the bottom waveform is the output TTL signal from the receiver.

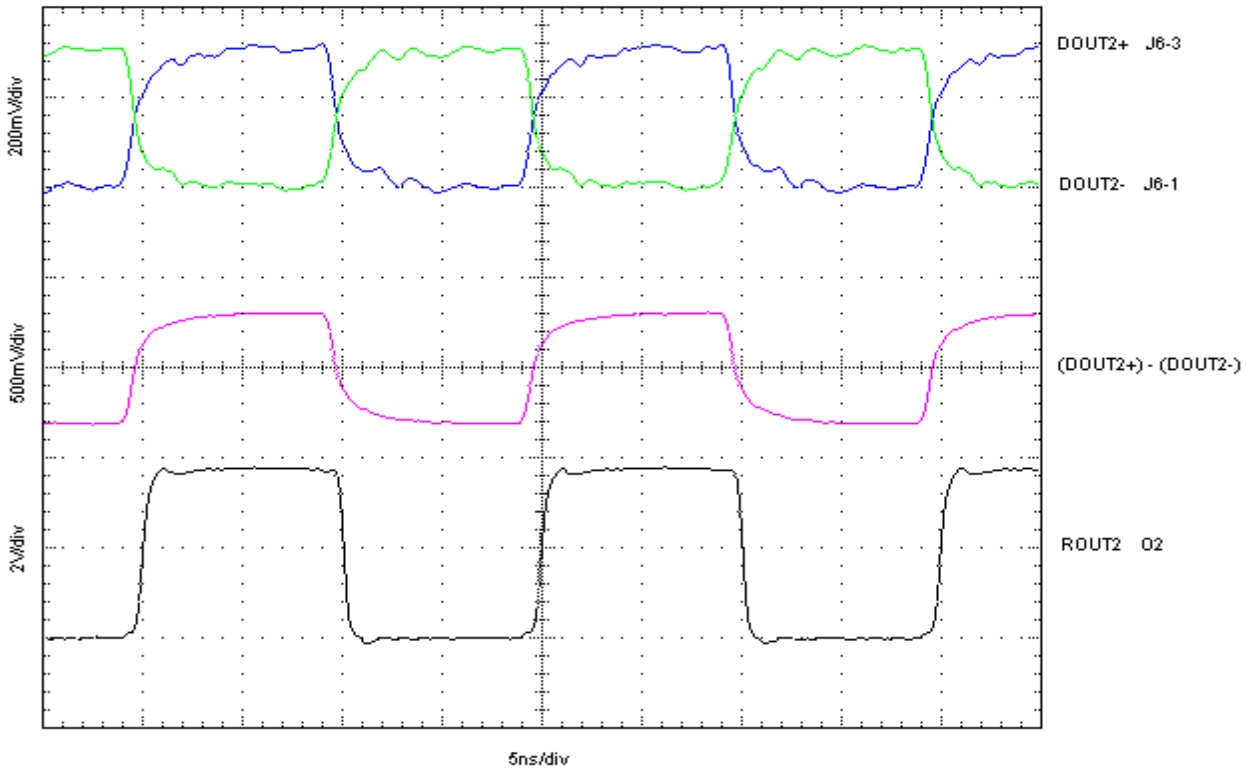


Figure 5: LVDS Channel #2 Waveforms — PCB Interconnect

The cable interconnect signal is also measured at the receiver inputs (test points J7-1 & J7-3 and J8-1 & J8-3). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with an RJ45 cable of 1 meter, 5 meters and 10 meters in length are shown in *Figure 6, 7* and *8*. Note the additional transition time slowing due to the cable's filter effects on the 5 meter and 10 meter test case.

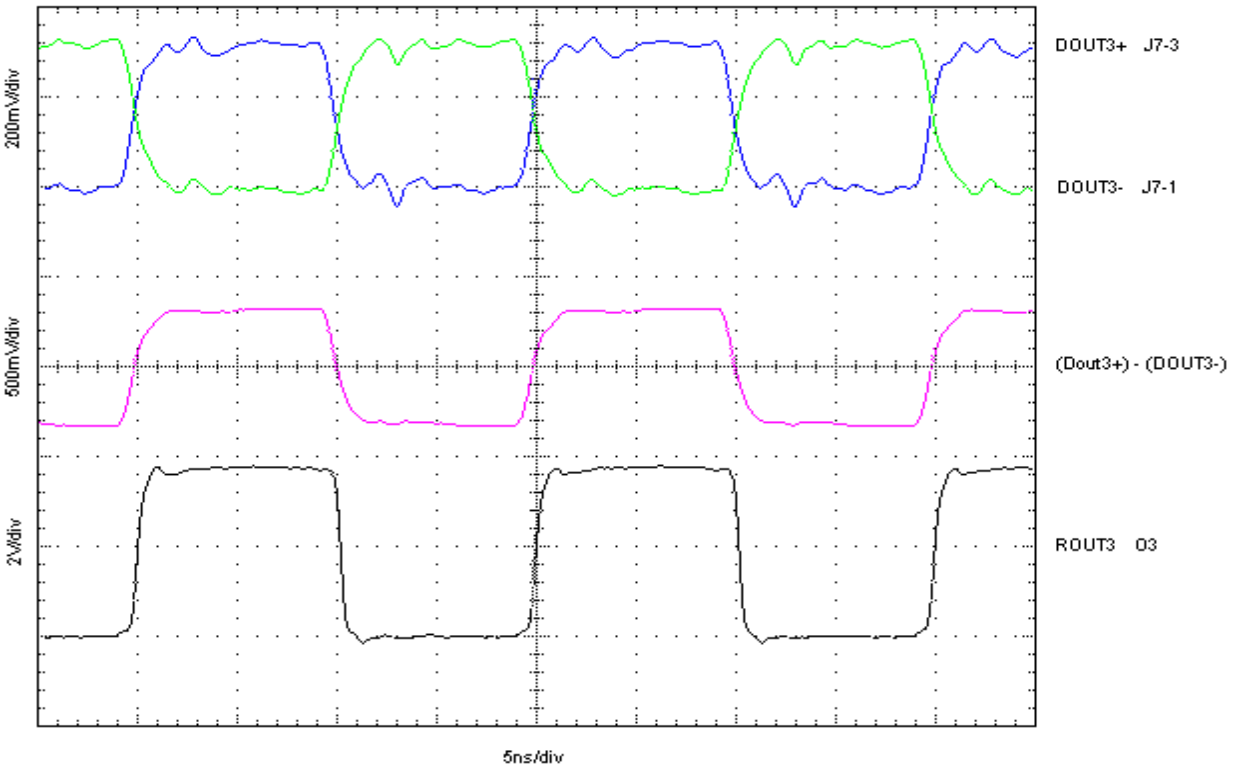


Figure 6: LVDS Channel #3 Waveforms - 1m Cable Interconnect

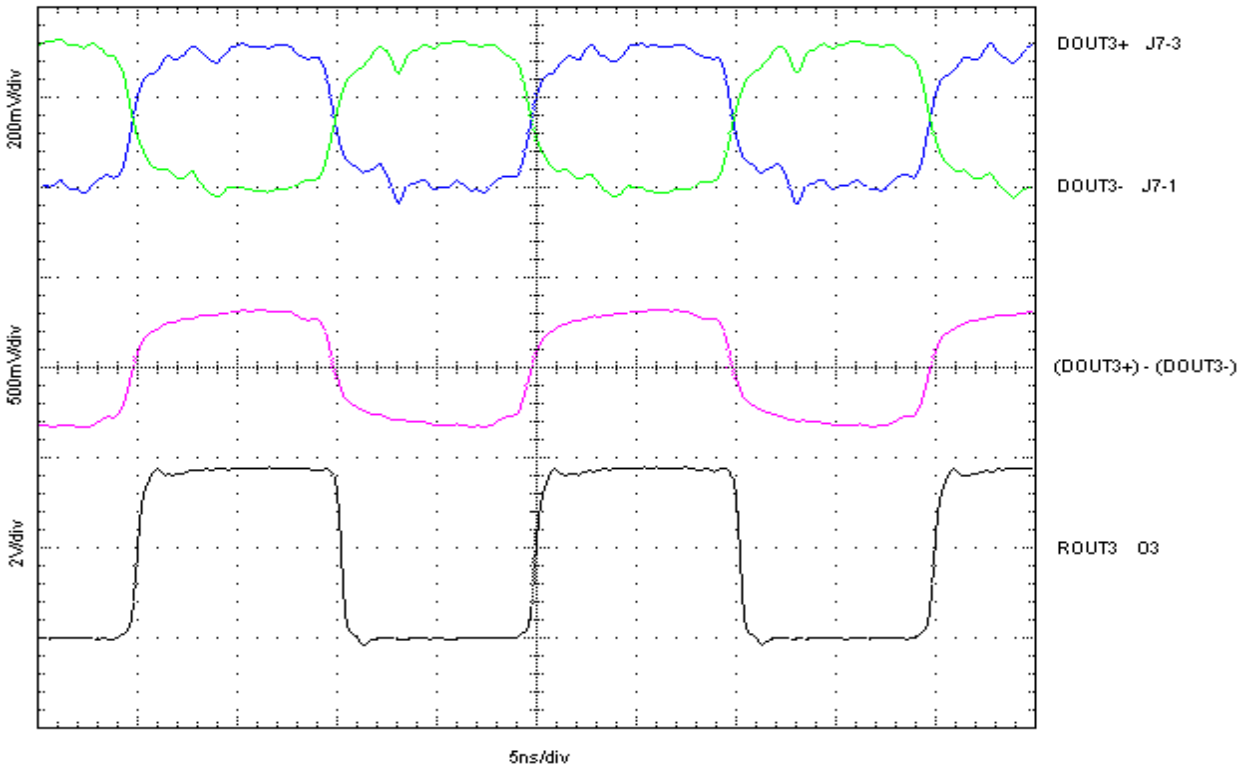


Figure 7: LVDS Channel #3 Waveforms - 5m Cable Interconnect

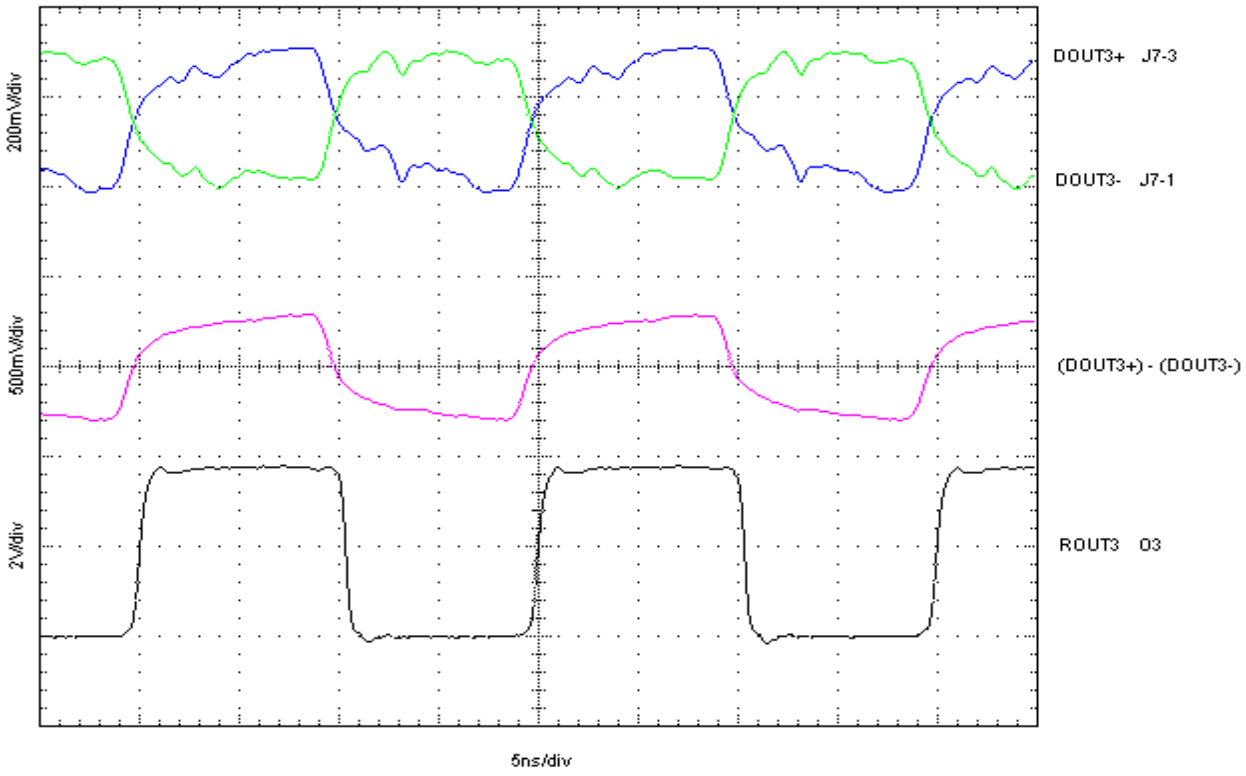


Figure 8: LVDS Channel #3 Waveforms - 10m Cable Interconnect

6.1.6 Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). Either a high impedance probe (100k Ohm or greater) or the TEK P6247 differential probe (>1GHz bandwidth) must be used. The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 GHz (4 GHz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK TDS 684B Digital Real Time scope (>1GHz bandwidth) and TEK P6247 differential probe heads. These probes offer 200kΩ, 1pF loading and a bandwidth of 1GHz. This test equipment was used to acquire the waveforms shown in *Figures 5, 6, 7, 8* and *9*.

The TEK P6247 differential probes may be used to measure the differential LVDS signal or each signal of the differential pair single-ended. This test equipment was used to acquire the waveforms differentially as well as single-endedly with the differential signal calculated by (D_{OUT+}) – (D_{OUT-}) shown in *Figure 9*. You can see that both of the differential signals look identical. The method in which you acquire the single-ended signals is important (such as matching probe types and lengths) if you intend to calculate the differential signal from the two single-ended signals.

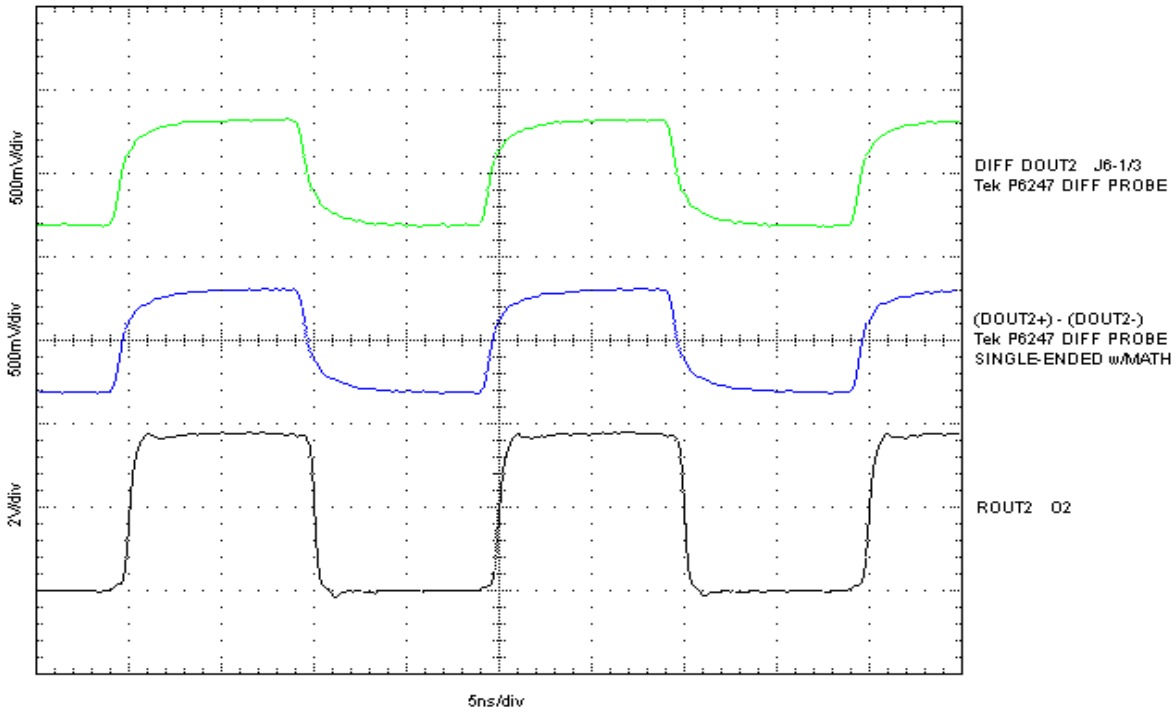


Figure 9: LVDS Channel #2 Waveforms - differential and calculated differential from single-ended waveform

LVDS waveforms may also be measured with high impedance probes such as common SD14 probe heads. These probes offer 100k Ohm, 0.4 pF loading and a bandwidth of 4 GHz. These probes connect to a TEK 11801B scope (50 GHz bandwidth). Probes with standard 50 Ohm loading should not be used on LVDS lines since they will load them too heavily. 50 Ohm probes may be used on the receiver output signal in conjunction with the 453 Ohm series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50 Ohm/(450 Ohm + 50 Ohm) or 1/10) of the output signal and the receiver output is loaded with 500 Ohm to ground.

6.1.7 Demo PCB Options

Option 1: 453 Ohm Resistors

A provision for a series 453 Ohm resistor (RS1, RS2, RS3 and RS4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 453 Ohm resistor a standard 50 Ohm scope probe may be used (500 Ohm total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver

The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J3). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the driver, connect the jumper to the power plane, to disable the driver connect the jumper to the ground.

Option 3: Disabling the LVDS Receiver

The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J4). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the receiver, connect the jumper to the power plane, to disable the receiver connect the jumper to ground.

Option 4: Cables

Different cables may also be tested (different lengths, materials, constructions). A standard RJ45 8-pin connector/pinout has been used (J1 and J2). Simply plug in the RJ45 1 meter or 5 meter cables included in the kit or build a custom cable.

Option 5: SMA or SMB Connectors

Both SMA and SMB connectors will fit the footprint on the boards for the driver inputs I1-4, receiver outputs O1-4 and the single receiver inputs I5-6. The board is loaded with SMBs on I4 and O4.

Option 6: Receiver Termination (Channel #1B)

The separate receiver input signals can be terminated separately (50 Ohm on each line to ground) utilizing pads RT5 (inverting to ground) and RT6 (true input to ground) for a signal generator interface. In addition, a single 100 Ohm differential resistor (across pads RT5 and RT6) can be used if the device is to be driven by a differential driver. Be sure to remove the 50 Ohm termination resistors RT5 and RT6 if you plan to use the 100 Ohm differential resistor.

6.1.8 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (Ground) to the pierced lug terminal marked GND

2) Connect the power supply lead to the pierced lug terminal marked VCC (3.3V)

3) Set J3 & J4 jumpers to the power plane ("ON") to enable the drivers and receivers

4) Connect enclosed RJ45 cable between connectors J1 and J2.

5) Connect a signal generator to the driver input (I4) with:

a) frequency = 50 MHz (100 Mbps)

b) V_{IL} = 0V & V_{IH} = 3.0V

c) t_r & t_f = 2 ns

d) duty cycle = 50% (square wave)

5) Connect differential probes to test points J8-1 and J8-3

6) View LVDS signals using the same voltage offset and volts/div settings on the scope with the TEK P6247 differential probes. View the output signal on a separate channel from test point O4. The signals that you will see should resemble *Figure 5*.

6.1.9 Common Mode Noise

When the receiver (DS90LV048A) is enabled, a small amount of common mode noise is passed from the output of the receiver to the inputs as shown in *Figure 10*. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. A design improvement was made to the DS90LV048A to reduce the magnitude of the noise coupled back to the inputs, reducing the feedback by 30% compared to prior devices. This noise will not be observed if the receiver device is disabled by setting J4 to "OFF" as shown in *Figure 11*.

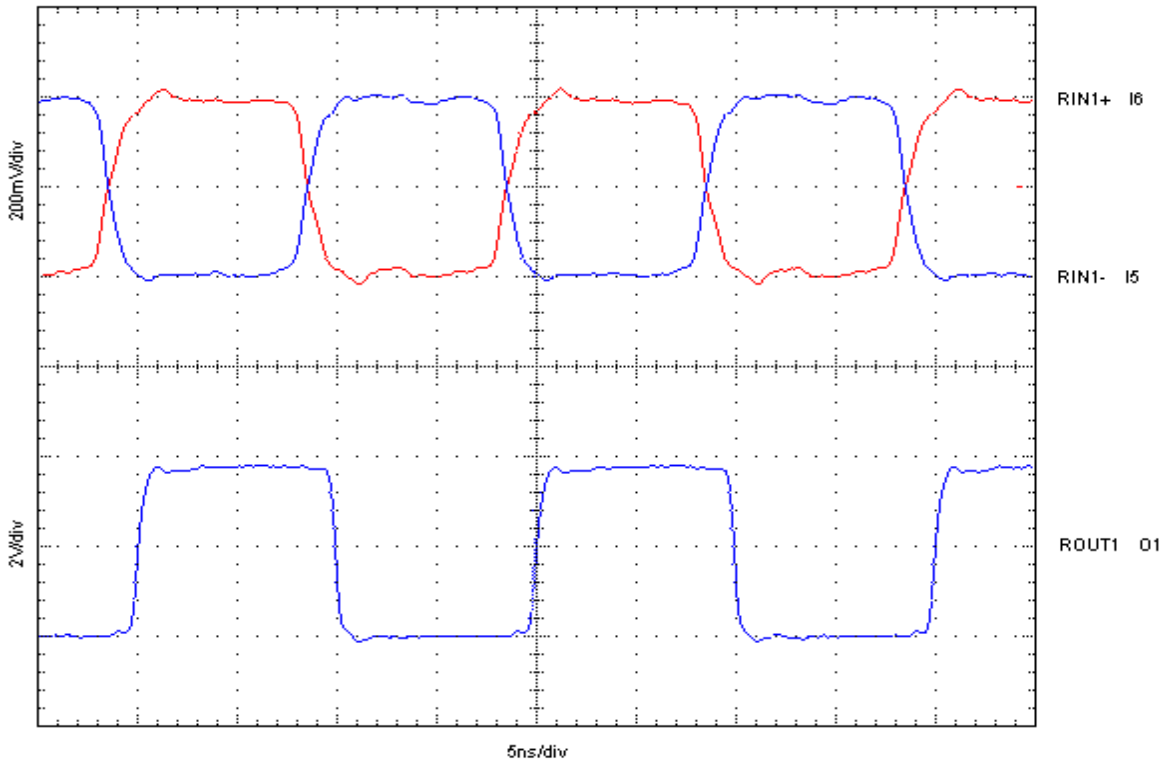


Figure 10: LVDS Cannel #1B Waveforms – A Small Amount of Common Mode Noise Coupled from Output to Input

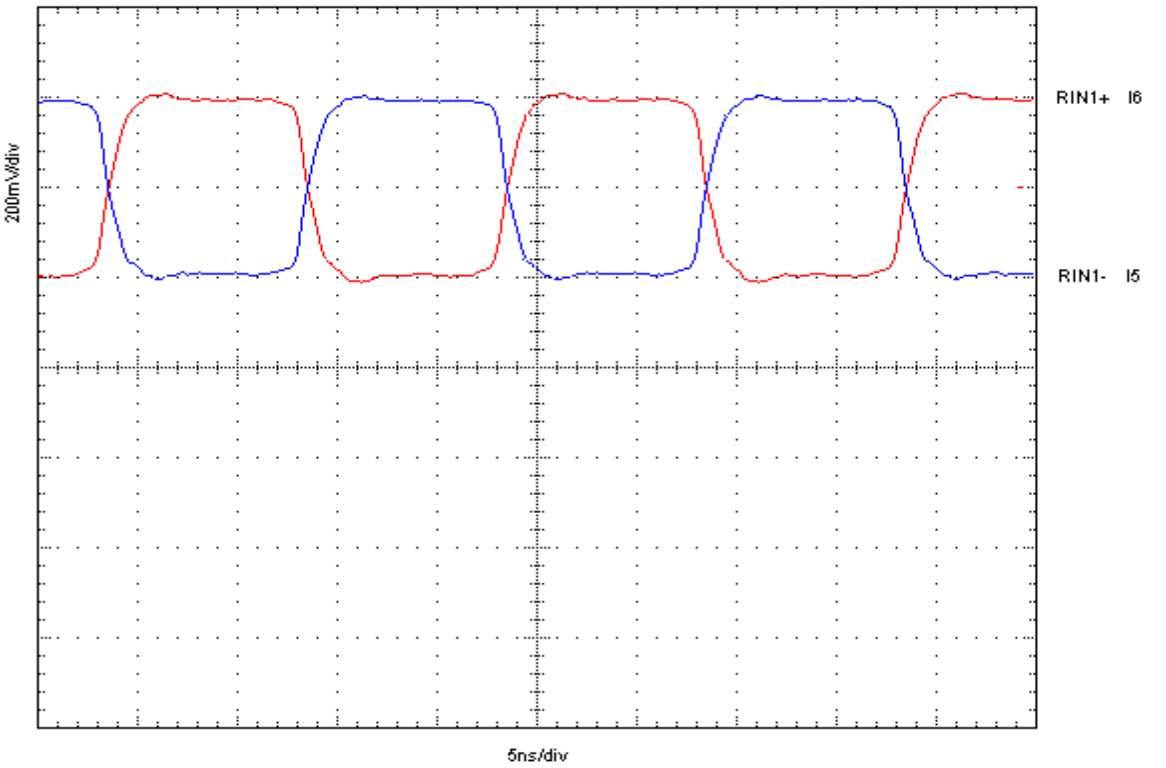


Figure 11: LVDS Channel #1B Waveforms – Output Disabled

6.1.10 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for high speed data transmission applications.

6.1.11 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK TDS 684B Digital Real Time scope, TEK 11801B scope
Probes	TEK P6247 differential probe, TEK SD-14 probe

Bill of Materials

Type	Label	Value/Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L TSSOP	DS90LV047ATMTC
IC	U2	(Quad Receiver)	1	16-L TSSOP	DS90LV048ATMTC
Connector	J1, J2	(8-pin RJ45)	2		AMP P/N 558310-1
Resistor	RT1-6	50Ω	6	RC0805	
Resistor	RL1-4	100Ω	4	RC0805	
Resistor	RS1, RS2, RS3, RS4	453Ω	0/4	RC0805	not loaded
Capacitor	CB1, CB2, CB3	0.1µF	3	CC0805	
Capacitor	CB13	0.01µF	1	CC0805	
Capacitor	CB21, CB22, CB23	0.001µF	3	CC0805	
Capacitor	CBR1	10µF, 35V	1	D	Solid Tantalum Chip Capacitor
Headers	J3, J4	3 lead header	2		100 mil spacing (single row header)
Headers	J5, J6, J7, J8	4 lead header	4		100 mil spacing (double row header)
Jumpers		0.1" jumper post shunts	2		
SMB Jack	I4, O4		2	SMB Connector	Johnson P/N 131-3701-201
* SMB Jack or SMA Jack	I1-3, I5-6, O1-3		0/8	SMB Connector SMA Connector	Johnson P/N 131-3701-201 Johnson P/N 142-0701-201
Plug (banana)	V_{CC}, GND	Uninsulated Standard Pierced Lug Terminal	2		Johnson P/N 108-0740-001
Cable		RJ45 Cable	2		1 meter and 5 meter
Legs			4		
Bolts/washers			4		
PCB			1		LVDS47/48PCB

* Note: On the evaluation board, inputs I1-3, I5-6 and outputs O1-3 are not loaded with connectors. These inputs and outputs can be loaded with either SMBs (P/N 131-3701-201) or SMAs (P/N 142-0701-201).

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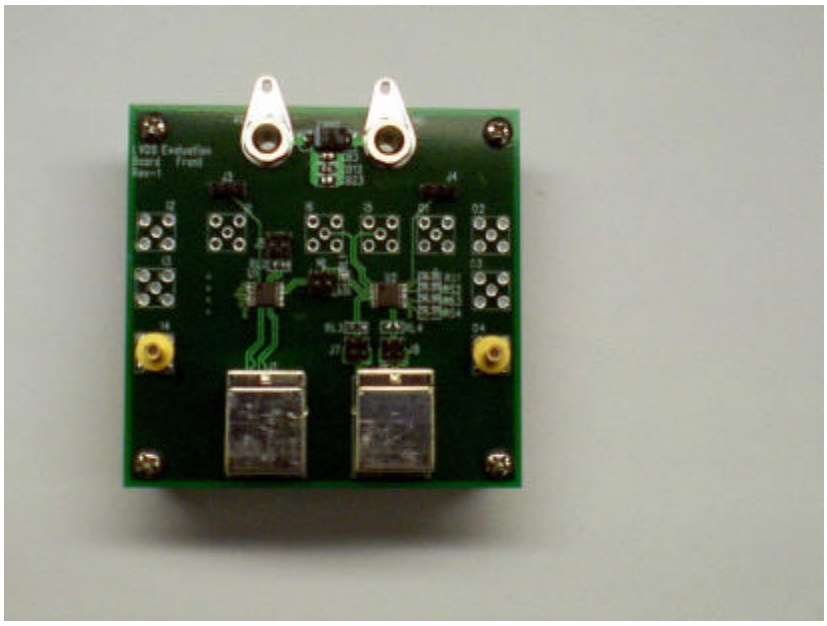

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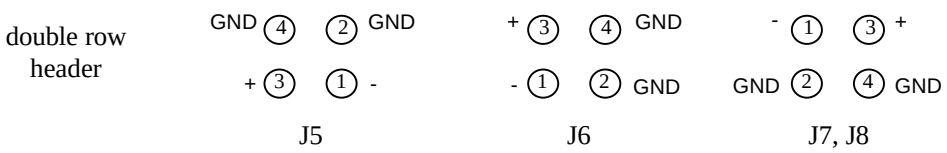
6.1.1 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of RJ45 cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation kit is LVDS47/48EVK. In this application note, the following differential signal nomenclature has been used: "Jx-3" represents the true signal and "Jx-1" represents the inverting signal. On the PCB, the true signal is represented by a '+' and the inverting signal is on the adjacent header pin as shown below.



The two adjacent ground pins are there to view the true or inverting signal single-endedly. Input signals are represented with an "I" while receiver outputs are represented with an "O."

6.1.2 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately. The five test cases are shown in *Figure 1*.

LVDS Channel # 1A: LVDS Line Driver

This test channel provides test points for an isolated driver with a standard 100 Ohm differential termination load. Probe access for the driver outputs is provided at test points on J5-1 and J5-3. The driver input signal (I1) is terminated with a 50 Ohm termination resistor (RT1) on the bottom side of the PCB.

LVDS Channel # 1B: LVDS Receiver

This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either two separate 50 Ohm terminations (RT5 and RT6) (each line to ground) or a 100 Ohm resistor connected across the inputs (differential). The first option allows for a standard signal generator interface. Input signals are connected at test points I5 (R_{IN-}) and I6 (R_{IN+}). A PCB option for a series 453 Ohm resistor (RS1) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is with two separate 50 Ohm terminations (RT5 and RT6) and without the series 453 Ohm resistor (RS1) for use of high impedance probes. The receiver output signal may be probed at test point O1.

LVDS Channel # 2: PCB Interconnect

This test channel connects Driver #2 to Receiver #2 via a pure PCB interconnect. A test point interface of the LVDS signaling is provided at test point J6-1 and J6-3. The driver input signal (I2) is terminated with a 50 Ohm termination resistor (RT2) on the bottom side of the PCB. The receiver output signal may be probed at test point O2. A PCB option for a series 453 Ohm resistor (RS2) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is without the series 453 Ohm resistor for use of high impedance probes. A direct probe connection is possible with a TEK P6247 differential probe high impedance probe (>1GHz bandwidth) on the LVDS signals at test points J6-1 and J6-3. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel # 3: Cable Interconnect

This test channel connects Driver #3 to Receiver #3 via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I3) is terminated with a 50 Ohm termination resistor (RT3) on the bottom side of the PCB. LVDS signals are probed via test points on J7. The receiver output signal may be probed at test point O3. A PCB option for a series 453 Ohm resistor (RS3) is also provided in case 50 Ohm probes are employed on the receiver output signal (see options section). The default setting is without the series 453 Ohm resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1GHz bandwidth) on the LVDS signals at test point J7-1 and J7-3.

LVDS Channel # 4: Cable Interconnect

This test channel connects Driver #4 to Receiver #4 also via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I4) is terminated with a 50 Ohm termination resistor (RT4) on the bottom side of the PCB. LVDS signals are probed via test points on J8. The receiver output signal may be probed at test point O4. A PCB option for a series 453 Ohm resistor (RS4) is also provided in case 50 Ohm probes are employed on the receiver output signal. The default setting is without the series 453 Ohm resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1 GHz bandwidth) on the LVDS signals at test point J8-1 and J8-3. This channel duplicates channel #3 so that it may be used for a clock function or for cable crosstalk measurements.

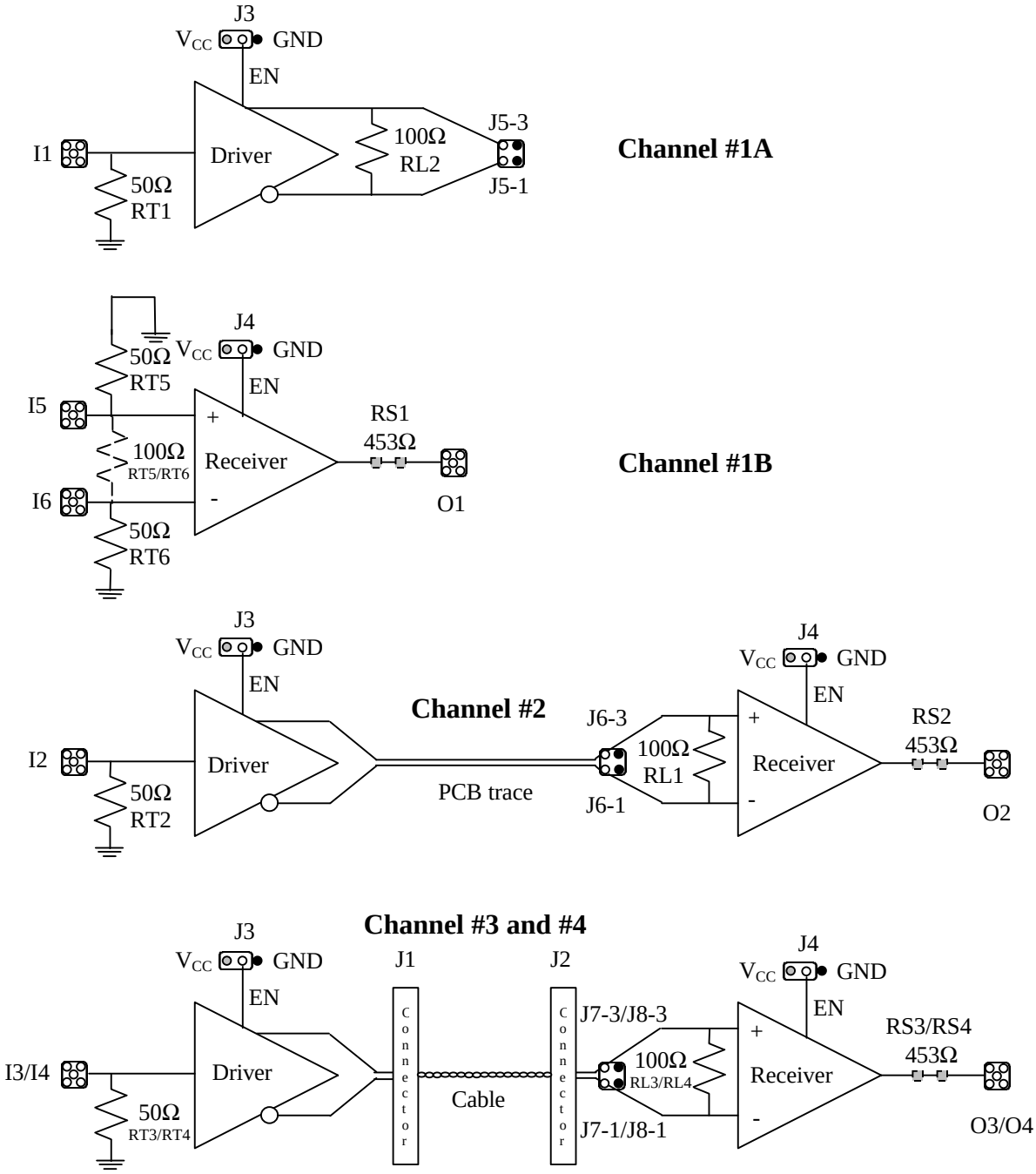


Figure 1: PCB Block Diagram

6.1.3 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a CAT 5 four twisted pair (8-pin) RJ45 cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the Ethernet standard and the cable is widely available. The connector is 8 position, with 0.10 centers and the pairs are pinned out up and down. For example pair 1 is on pins 1 and 5, not pins 1 and 2 (see *Figure 2*).

IMPORTANT NOTE: The 2 unused pairs are connected to ground. Other cables may also be used if they are built up.

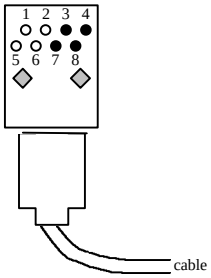


Figure 2: RJ45 Connector

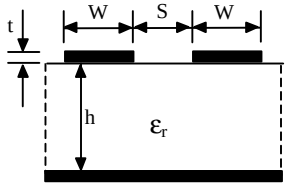
6.1.4 PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal.

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, refer to PCB layout between U1 and J1). Employing differential traces will ensure a low emission design and maximum common mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common mode. Also by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable's differential characteristic impedance). Equations for calculating differential impedance are contained in National application note AN-905 for both microstrip and stripline differential PCB traces.

For the microstrip line, the differential impedance, Z_{diff}, is:

$$Z_{diff} \cong 2Z_O (1 - 0.48e^{-0.96s/h}) \text{ Ohms}$$



For the new evaluation board h = 24 mils, s = 11mils and Z_O = 70 Ohms. Calculating the differential impedance, Z_{diff}, is:

$$Z_{diff} \cong 2Z_O (1 - 0.48e^{-0.96(11/24)}) \text{ Ohms}$$

$$2 (70) (0.69086) \text{ Ohms}$$

$$96.72 \text{ Ohms}$$

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor minimizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13 mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match, the higher the signal fidelity and the less common mode reflections will occur (lower emissions too). A typical value is 100 Ohms ±1%.

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

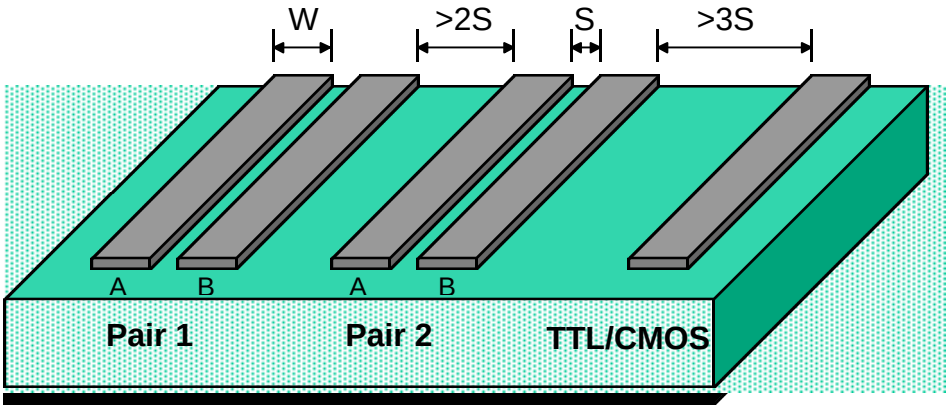


Figure 3: Pair Spacing for Differential Lines

Bypassing capacitors are recommended for each package. A 0.1 µF is sufficient on the quad driver or receiver device (CB1 and CB2) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB21 and CB22) if desired. Traces connecting V_{CC} and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB3, CB13, and CB23 if desired.

6.1.5 Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals have a V_{OD} specification of 250mV to 450mV with a typical V_{OS} of 1.2V. Our devices have a typical V_{OD} of 300mV, but for the example below, we will use a signal between 1.0 V (V_{OL}) and 1.4 V (V_{OH}) for a 400 mV V_{OD}. The differential waveform is constructed by subtracting the Jx-1 (inverting) signal from the Jx-3 (true) signal. V_{OD} = (Jx-3) – (Jx-1). The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in *Figure 4.*

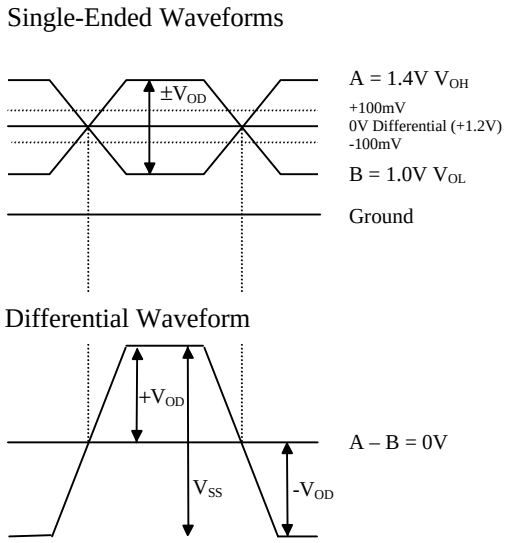


Figure 4: Single-ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #2) can be measured at the receiver inputs (test points J6-1 and J6-3). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See *Figure 5*. Note that the data rate is 100 Mbps and the differential waveform ($V_{DIFF} = D_{OUT2+} - D_{OUT2-}$) shows fast transition times with little distortion.

In *Figure 5, 6, 7* and *8*, the top two waveforms are the single-ended outputs (between the driver and receiver), the middle waveform is the calculated differential output signal from the two single-ended signals and the bottom waveform is the output TTL signal from the receiver.

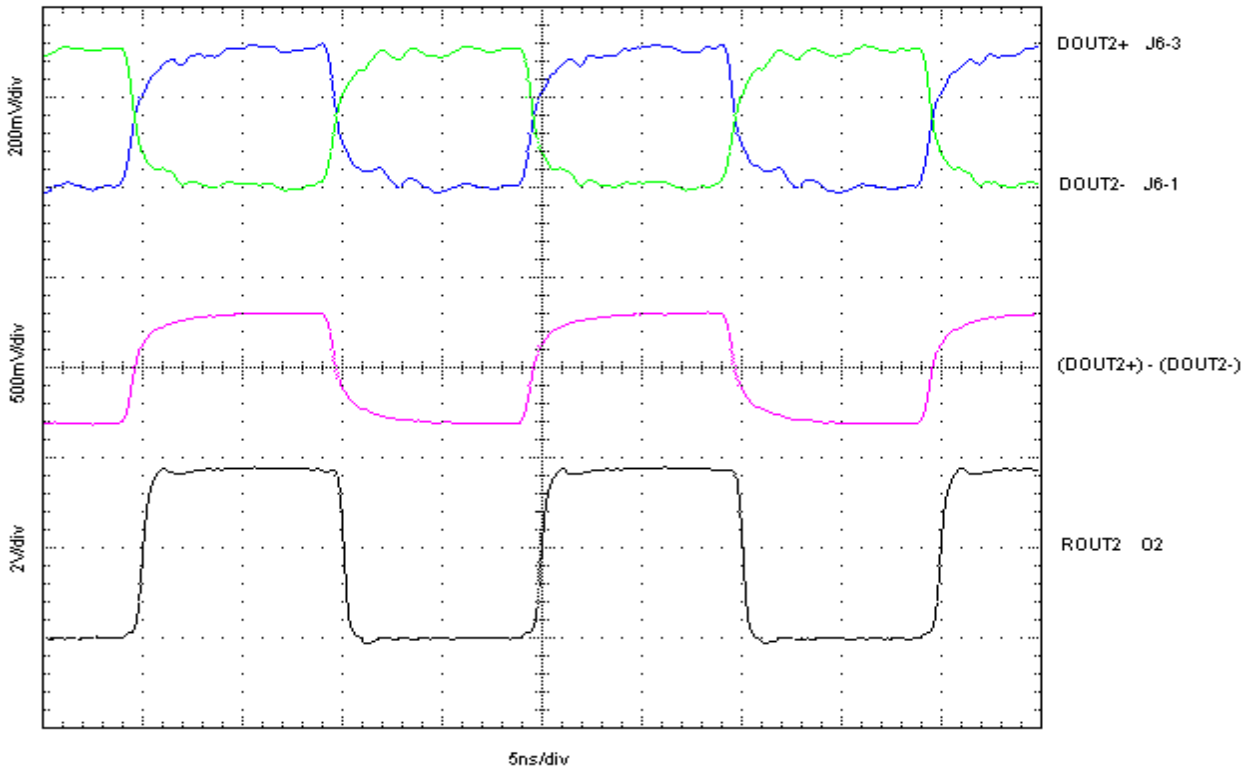


Figure 5: LVDS Channel #2 Waveforms — PCB Interconnect

The cable interconnect signal is also measured at the receiver inputs (test points J7-1 & J7-3 and J8-1 & J8-3). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with an RJ45 cable of 1 meter, 5 meters and 10 meters in length are shown in *Figure 6, 7* and *8*. Note the additional transition time slowing due to the cable's filter effects on the 5 meter and 10 meter test case.

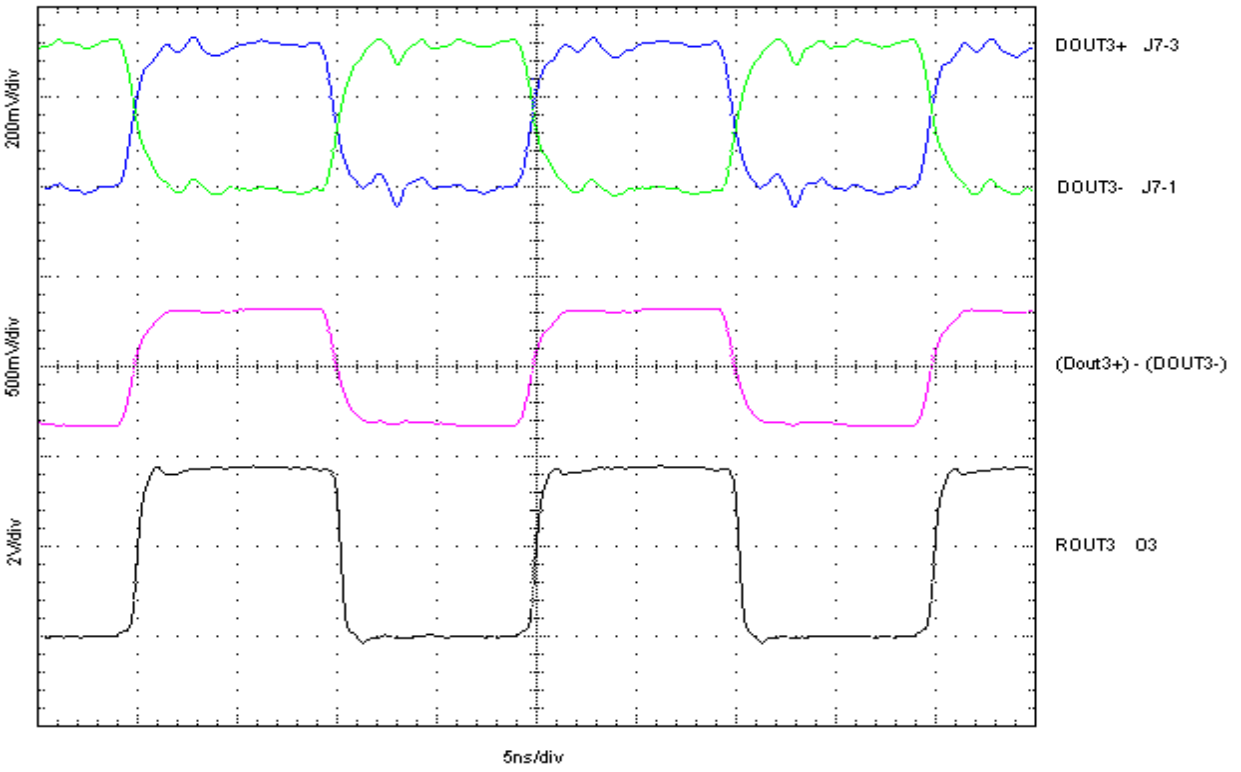


Figure 6: LVDS Channel #3 Waveforms - 1m Cable Interconnect

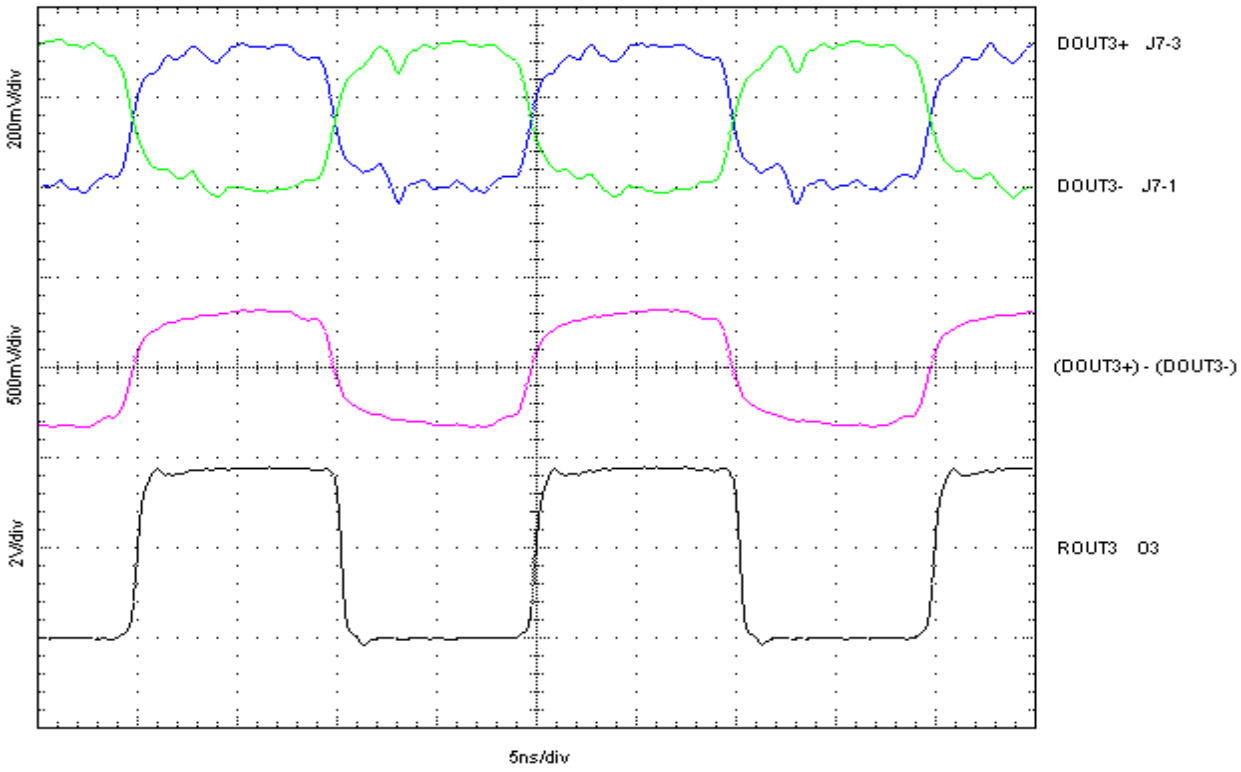


Figure 7: LVDS Channel #3 Waveforms - 5m Cable Interconnect

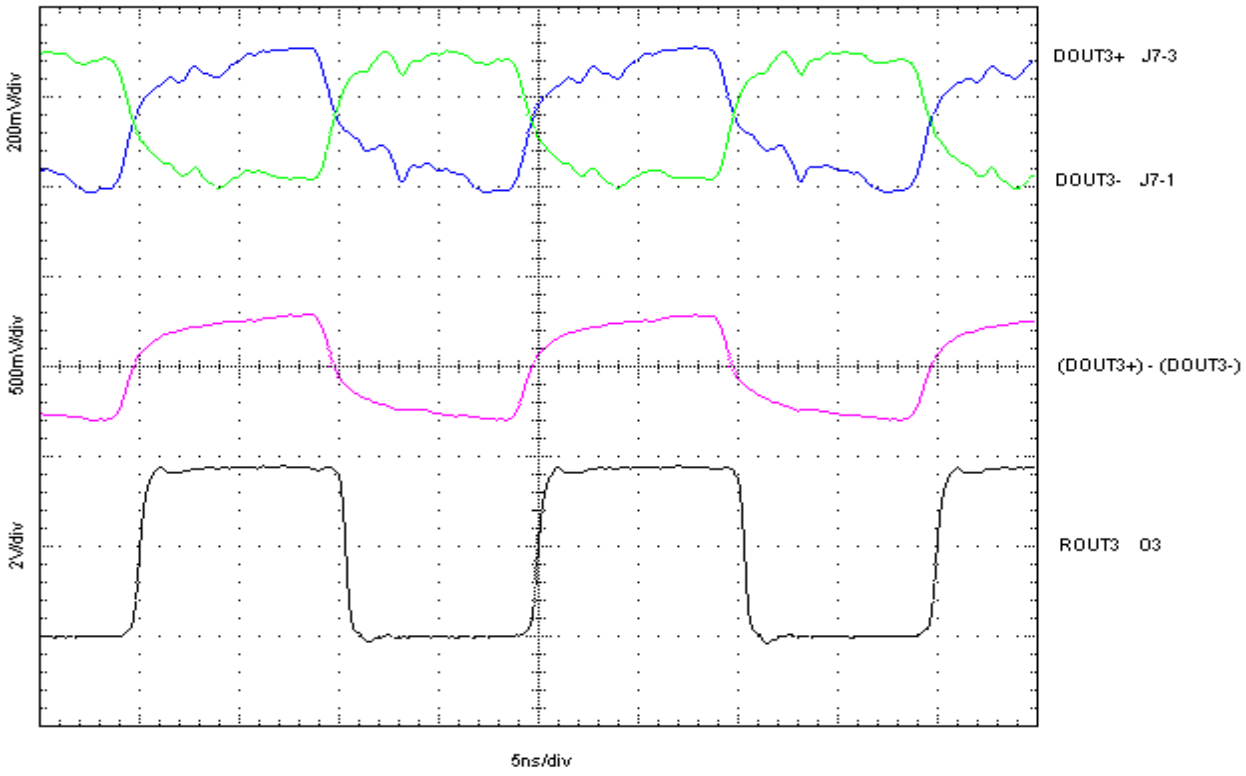


Figure 8: LVDS Channel #3 Waveforms - 10m Cable Interconnect

6.1.6 Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). Either a high impedance probe (100k Ohm or greater) or the TEK P6247 differential probe (>1GHz bandwidth) must be used. The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 GHz (4 GHz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK TDS 684B Digital Real Time scope (>1GHz bandwidth) and TEK P6247 differential probe heads. These probes offer 200kΩ, 1pF loading and a bandwidth of 1GHz. This test equipment was used to acquire the waveforms shown in *Figures 5, 6, 7, 8* and *9*.

The TEK P6247 differential probes may be used to measure the differential LVDS signal or each signal of the differential pair single-ended. This test equipment was used to acquire the waveforms differentially as well as single-endedly with the differential signal calculated by (D_{OUT+}) – (D_{OUT-}) shown in *Figure 9*. You can see that both of the differential signals look identical. The method in which you acquire the single-ended signals is important (such as matching probe types and lengths) if you intend to calculate the differential signal from the two single-ended signals.

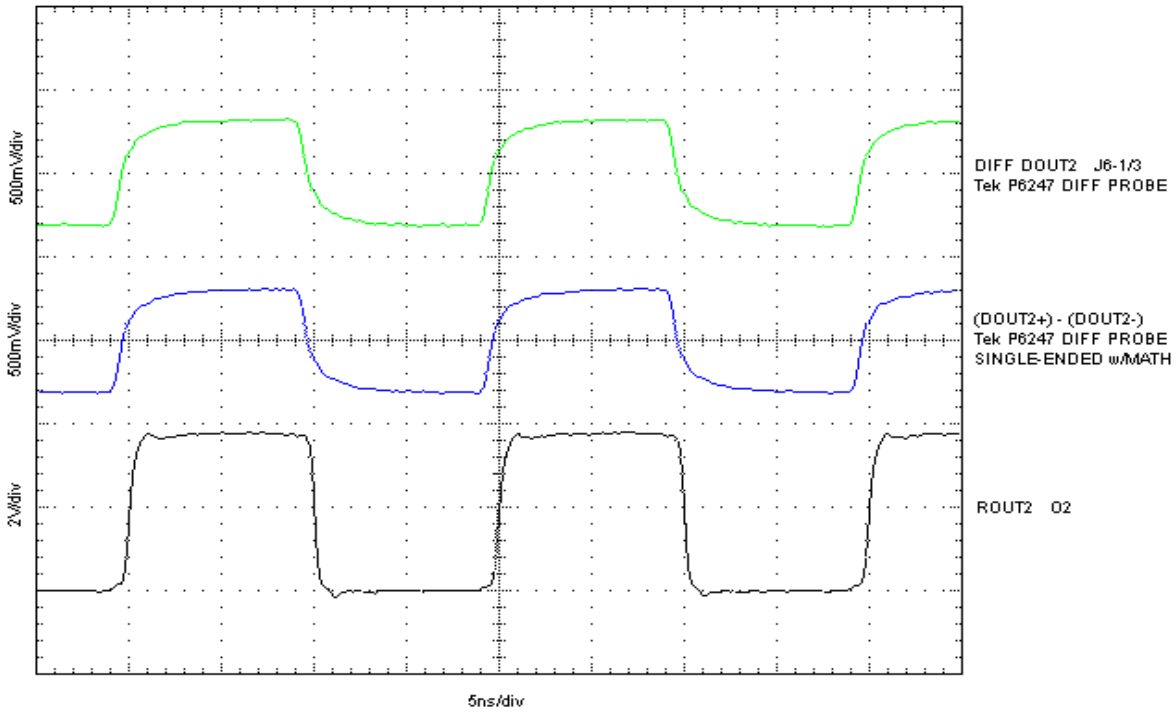


Figure 9: LVDS Channel #2 Waveforms - differential and calculated differential from single-ended waveform

LVDS waveforms may also be measured with high impedance probes such as common SD14 probe heads. These probes offer 100k Ohm, 0.4 pF loading and a bandwidth of 4 GHz. These probes connect to a TEK 11801B scope (50 GHz bandwidth). Probes with standard 50 Ohm loading should not be used on LVDS lines since they will load them too heavily. 50 Ohm probes may be used on the receiver output signal in conjunction with the 453 Ohm series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50 Ohm/(450 Ohm + 50 Ohm) or 1/10) of the output signal and the receiver output is loaded with 500 Ohm to ground.

6.1.7 Demo PCB Options

Option 1: 453 Ohm Resistors

A provision for a series 453 Ohm resistor (RS1, RS2, RS3 and RS4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 453 Ohm resistor a standard 50 Ohm scope probe may be used (500 Ohm total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver

The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J3). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the driver, connect the jumper to the power plane, to disable the driver connect the jumper to the ground.

Option 3: Disabling the LVDS Receiver

The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J4). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the receiver, connect the jumper to the power plane, to disable the receiver connect the jumper to ground.

Option 4: Cables

Different cables may also be tested (different lengths, materials, constructions). A standard RJ45 8-pin connector/pinout has been used (J1 and J2). Simply plug in the RJ45 1 meter or 5 meter cables included in the kit or build a custom cable.

Option 5: SMA or SMB Connectors

Both SMA and SMB connectors will fit the footprint on the boards for the driver inputs I1-4, receiver outputs O1-4 and the single receiver inputs I5-6. The board is loaded with SMBs on I4 and O4.

Option 6: Receiver Termination (Channel #1B)

The separate receiver input signals can be terminated separately (50 Ohm on each line to ground) utilizing pads RT5 (inverting to ground) and RT6 (true input to ground) for a signal generator interface. In addition, a single 100 Ohm differential resistor (across pads RT5 and RT6) can be used if the device is to be driven by a differential driver. Be sure to remove the 50 Ohm termination resistors RT5 and RT6 if you plan to use the 100 Ohm differential resistor.

6.1.8 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (Ground) to the pierced lug terminal marked GND

2) Connect the power supply lead to the pierced lug terminal marked VCC (3.3V)

3) Set J3 & J4 jumpers to the power plane ("ON") to enable the drivers and receivers

4) Connect enclosed RJ45 cable between connectors J1 and J2.

5) Connect a signal generator to the driver input (I4) with:

a) frequency = 50 MHz (100 Mbps)

b) V_{IL} = 0V & V_{IH} = 3.0V

c) t_r & t_f = 2 ns

d) duty cycle = 50% (square wave)

5) Connect differential probes to test points J8-1 and J8-3

6) View LVDS signals using the same voltage offset and volts/div settings on the scope with the TEK P6247 differential probes. View the output signal on a separate channel from test point O4. The signals that you will see should resemble *Figure 5*.

6.1.9 Common Mode Noise

When the receiver (DS90LV048A) is enabled, a small amount of common mode noise is passed from the output of the receiver to the inputs as shown in *Figure 10*. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. A design improvement was made to the DS90LV048A to reduce the magnitude of the noise coupled back to the inputs, reducing the feedback by 30% compared to prior devices. This noise will not be observed if the receiver device is disabled by setting J4 to "OFF" as shown in *Figure 11*.

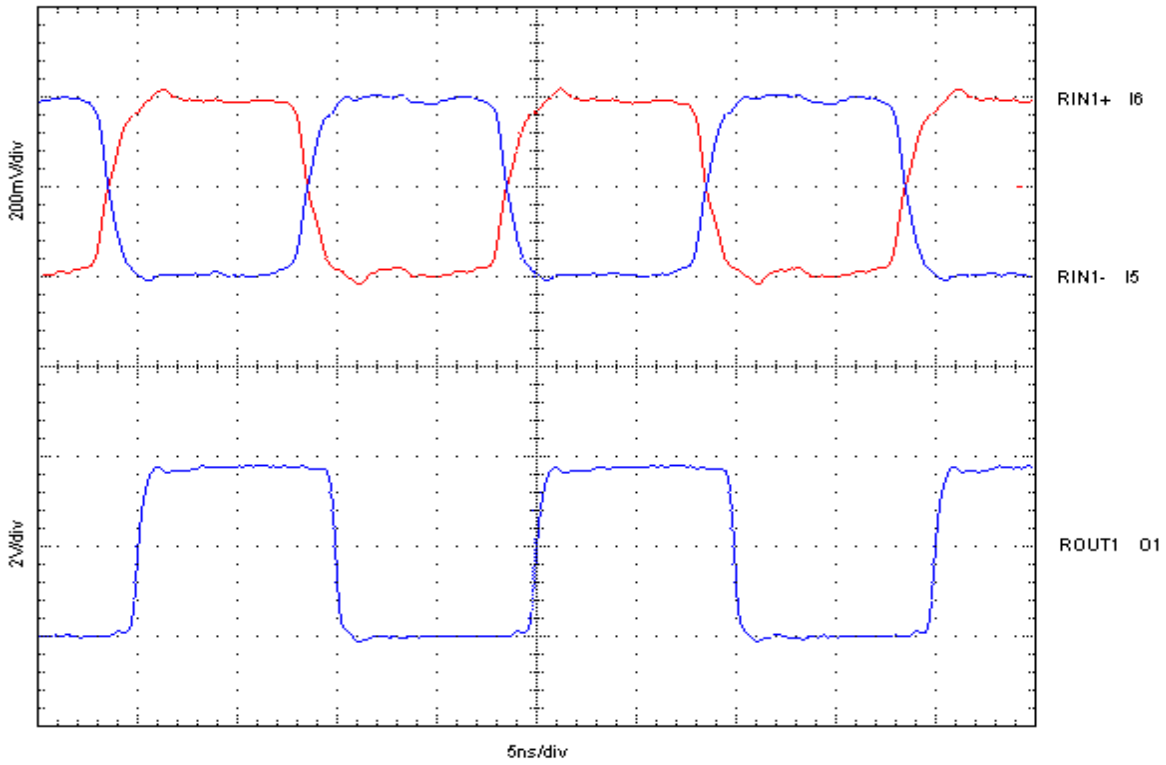


Figure 10: LVDS Cannel #1B Waveforms – A Small Amount of Common Mode Noise Coupled from Output to Input

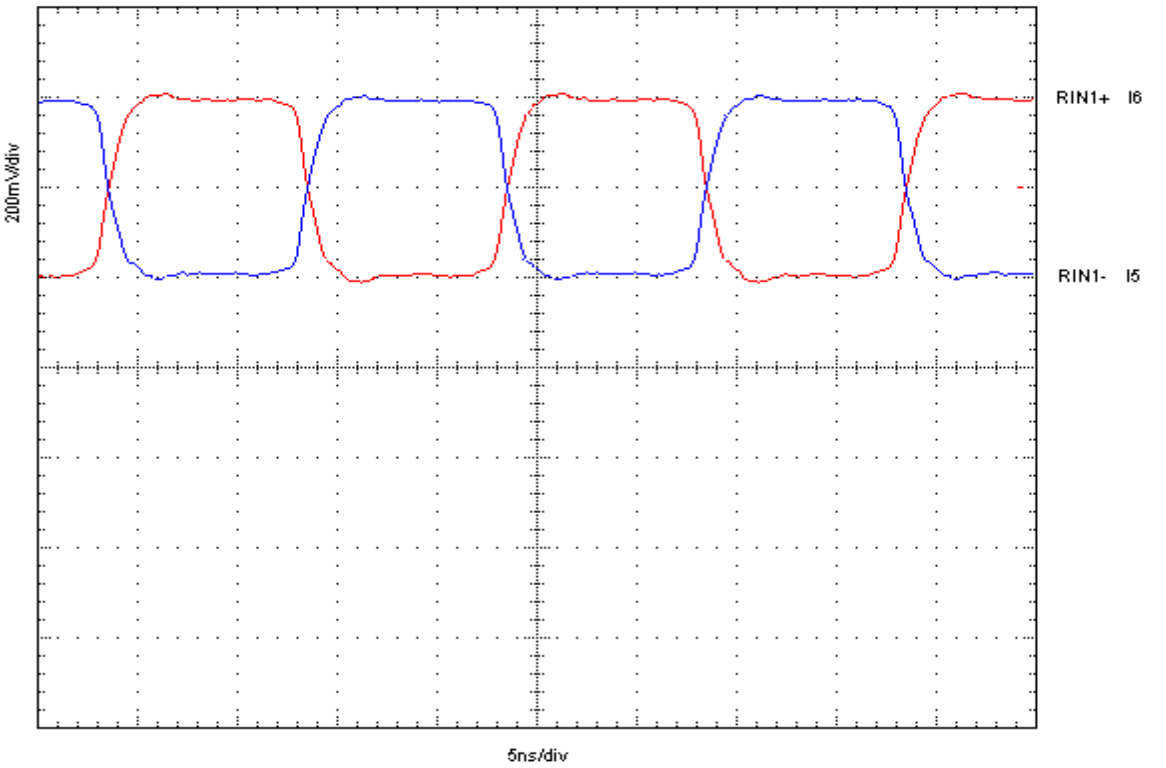


Figure 11: LVDS Channel #1B Waveforms – Output Disabled

6.1.10 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for high speed data transmission applications.

6.1.11 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK TDS 684B Digital Real Time scope, TEK 11801B scope
Probes	TEK P6247 differential probe, TEK SD-14 probe

Bill of Materials

Type	Label	Value/Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L TSSOP	DS90LV047ATMTC
IC	U2	(Quad Receiver)	1	16-L TSSOP	DS90LV048ATMTC
Connector	J1, J2	(8-pin RJ45)	2		AMP P/N 558310-1
Resistor	RT1-6	50Ω	6	RC0805	
Resistor	RL1-4	100Ω	4	RC0805	
Resistor	RS1, RS2, RS3, RS4	453Ω	0/4	RC0805	not loaded
Capacitor	CB1, CB2, CB3	0.1µF	3	CC0805	
Capacitor	CB13	0.01µF	1	CC0805	
Capacitor	CB21, CB22, CB23	0.001µF	3	CC0805	
Capacitor	CBR1	10µF, 35V	1	D	Solid Tantalum Chip Capacitor
Headers	J3, J4	3 lead header	2		100 mil spacing (single row header)
Headers	J5, J6, J7, J8	4 lead header	4		100 mil spacing (double row header)
Jumpers		0.1" jumper post shunts	2		
SMB Jack	I4, O4		2	SMB Connector	Johnson P/N 131-3701-201
* SMB Jack or SMA Jack	I1-3, I5-6, O1-3		0/8	SMB Connector SMA Connector	Johnson P/N 131-3701-201 Johnson P/N 142-0701-201
Plug (banana)	V_{CC}, GND	Uninsulated Standard Pierced Lug Terminal	2		Johnson P/N 108-0740-001
Cable		RJ45 Cable	2		1 meter and 5 meter
Legs			4		
Bolts/washers			4		
PCB			1		LVDS47/48PCB

* Note: On the evaluation board, inputs I1-3, I5-6 and outputs O1-3 are not loaded with connectors. These inputs and outputs can be loaded with either SMBs (P/N 131-3701-201) or SMAs (P/N 142-0701-201).