

About the ToPSync™ ACS9550T

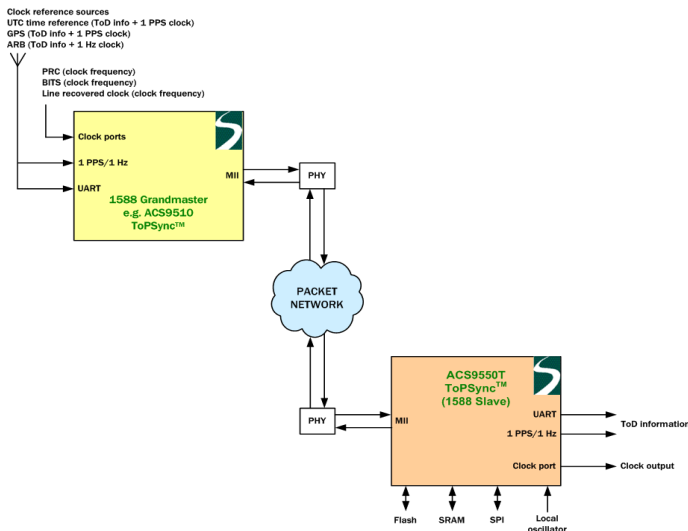
The ToPSync™ ACS9550T ASSP utilizes Semtech's ToPSync™ technology which, in conjunction with an appropriate Precision Time Protocol (PTP) Grandmaster, can be used for many applications which require a reference frequency that is traceable to a remote, centralized, frequency source, or a time or phase reference that is aligned to a central reference point of phase or time.

Whilst the distribution of a common frequency reference has been a key technology in most telecom networks since the beginning of digital networks, the techniques used do not work on packet switched networks. A new technique is required, and the ACS9550T has been developed using a combination of PTP and adaptive packet delay filtering. Although PTP was conceived to use on-path support such as boundary clocks or transparent clocks, the packet delay filtering of the ACS9550T renders such support unnecessary.

As an example, if WiBro/WiMax transmitter stations do not have a common phase across the regions in which they overlap, interslot interference can occur. For this application, it is not enough to distribute a frequency reference since the individual path delays to each transmitter would result in individual phases with consequent interference. A sensible solution to this problem is to use a two-way timing protocol such as PTP to cancel out the path delay and provide a common phase at each transmitter. This can be achieved even on legacy packet networks that have no on-path support, making it possible to time wireless transmitters over existing packet networks.

For occasions when the timing packet stream fails, the ACS9550T includes a holdover mode to maintain timing within defined limits until the stream can be re-established.

System diagram



Features

- **Fully integrated** - IEEE1588 (PTP) Slave function providing reference frequency output. Time-of-Day (ToD) output and one pulse per second (PPS) output. Powerful integrated processor running clock recovery algorithm (a combination of PTP and adaptive packet delay filtering).
- **PTP Grandmaster selection** - configured or automatic (according to the PTP Best Master Clock algorithm). Multiple Grandmasters supported.
- **Powerful network delay analysis** delivers full time alignment in the slave over hostile networks (including Layer 2 & 3 routed).
- **Dynamic adaptation** to delay variations. Tolerant to network loading changes (ramps and steps), routing changes and temporary outages.
- **Operational support** - unicast and multicast operation.
- **Configurable DiffServ codepoint** - for high priority packet routing.
- **Precision holdover.**
- **Interfaces for:**

Time-aligned output pair:

1 PPS and 125 MHz divided by n (n = 4 to 125000).

Six frequency-aligned outputs:

1 Hz and programmable frequency 1 kHz to 62.5 MHz.

Media Independent Interface (Ethernet port).

Serial peripheral interface (SPI).

Local oscillator (reference frequency for internal clock frequency).

SRAM port.

JTAG boundary scan port.

- **Supports** operation with a local oscillator accurate to ± 20 ppm or better.
- **Time alignment** performance better than $\pm 1 \mu\text{s}$ on a managed 5-switch GbE network under G.8261⁴ test conditions.*
- **Frequency alignment** performance better than ± 10 ppb on a managed 5-switch GbE network under G.8261⁴ test conditions.*
- **Standard compliance** - IEEE 1588 v2¹, G.8261⁴.
- **BGA package** - 360 pin, 20 mm x 20 mm, 1 mm pitch.
- **Lead-free version available** - RoHS⁵ and WEEE⁶ compliant.

* This is an indication of Semtech tested performance and is not guaranteed across all types of switches and network conditions. Please contact Semtech ToPSync™ support for further details.

Principles of operation

The ACS9550T provides standards-based timing for equipment used in packet switched networks. Control of the device is exercised by an API. The ACS9550T also has a Self-Test capability that checks for defective operation prior to use.

The ACS9550T provides timing solutions that deliver a performance better than that required by the G.8261⁴ standard. The device can align its timebase with that of the PTP Grandmaster and can generate time-of-day signals as well as clock signals. The device filters packet delay variations and maintains phase/time alignment with the Grandmaster, without the need for PTP assistance in intermediary network nodes (such as boundary clocks or transparent clocks). Possible applications include:

- Providing six programmable rate clock (up to 62.5 MHz), allowing wireless operators to migrate to packet-based backhaul technology and eliminate T1/E1 interfaces, while maintaining the required timing to all network elements.
- Providing a 1 PPNs signal, with or without associated ToD information, which is aligned with the timebase of a central Grandmaster clock, thereby supporting applications which require a common phase to be available around a network (such as wireless applications using TDD technologies).

The ACS9550T operates as a slave in accordance with the PTP best master clock algorithm (BMCA), or via configuration that allows the device to operate with another clock selection mechanism.

The ACS9550T has holdover and free-run features for conditions when no timing packet streams are available. The stability of the output clocks during such self-timing activities is dependent on the performance of an external oscillator that controls the internal clocks. The oscillator should be chosen to suit the frequency accuracy and phase stability requirements of the application.

The ACS9550T performs all the functions required for a complete, stand-alone, clock recovery system - including hardware time-stamping, PTP protocol, network noise suppression, network re-route accommodation and holdover, and provides outputs for applications that require continuation of frequency, phase and time. A serial peripheral interface is provided for communication with a host microprocessor.

An API is provided for configuration and status monitoring. The API offers system developers the means to produce appropriate application software to configure and control the ACS9550T and thus integrate the required functionality from the device into their synchronization scheme.

The ACS9550T requires:

- 1 MB of SRAM
- a generic packet PHY with appropriate termination circuitry.

References to standards

- [1] IEEE Std. 1588™ V2 -2008 (2008).
- [2] ITU-T G.823 (03/2000).
- [3] ITU-T G.824 (03/2000).
- [4] ITU-T G.8261 (former G.pactiming).
- [5] RoHS Directive 2002/95/EC.
- [6] Waste electrical and electronic equipment (WEEE) 2003.

Associated documents

Refer also to the ACS9550T Datasheet, User Guide and Application Programming Interface document.

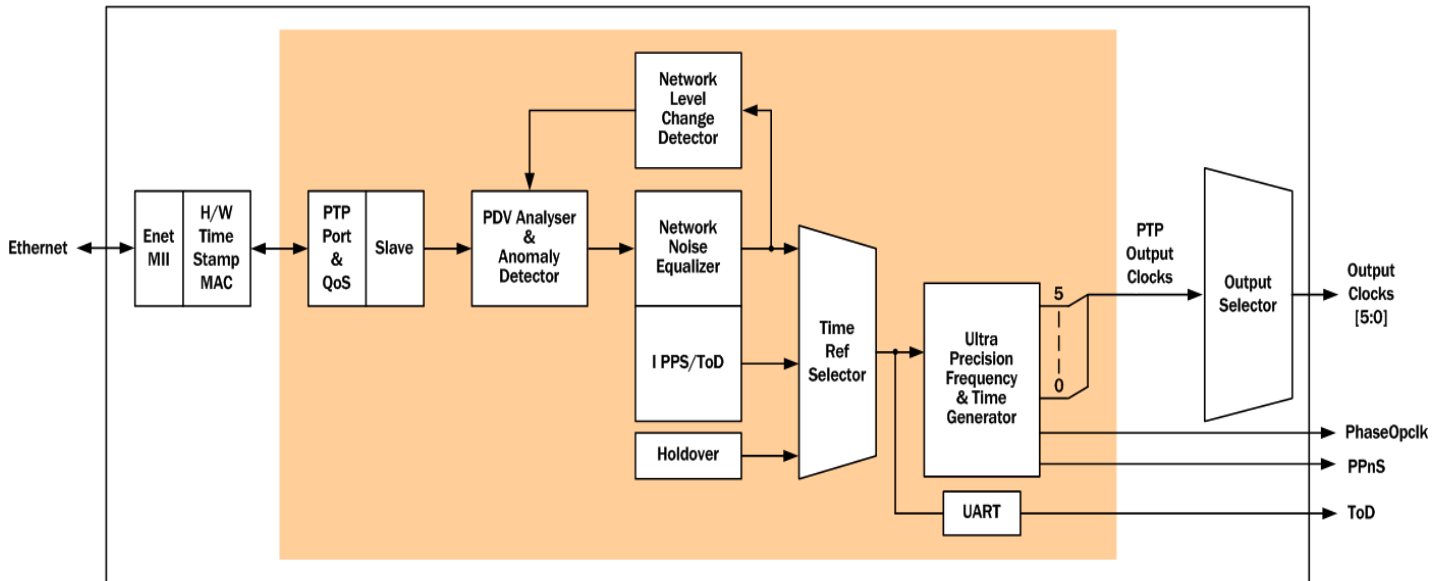
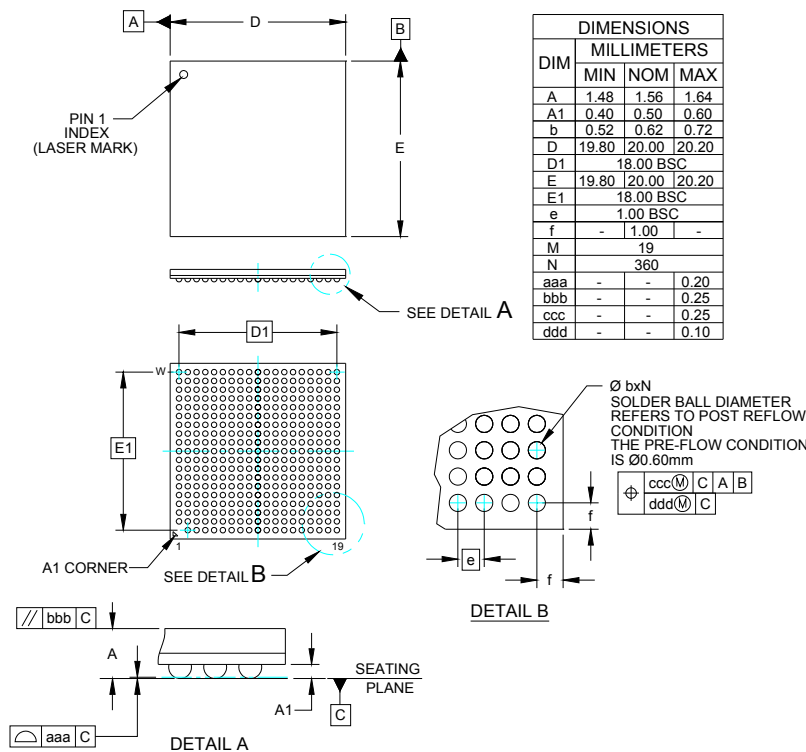
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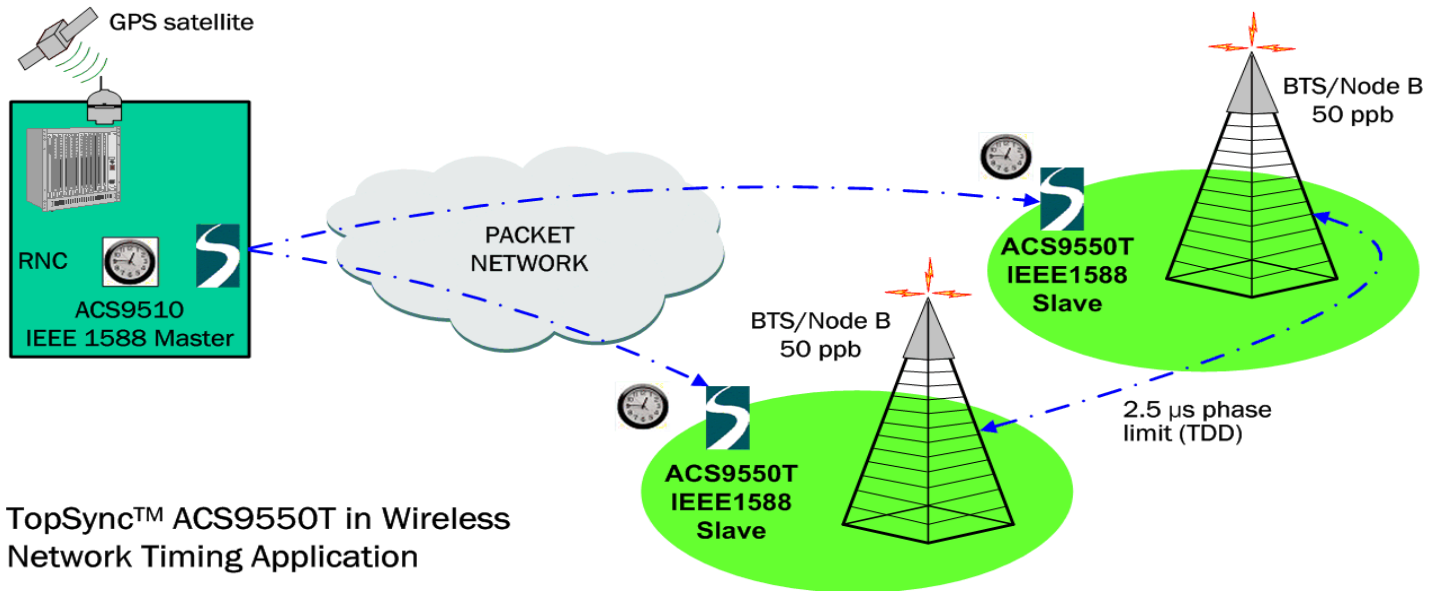
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Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure that equipment employing this device is compliant to all relevant standards.

ToPSync™ is a registered trademark of the Semtech Corporation. All other manufacturers' trademarks are hereby acknowledged.

Block diagram of the ACS9550T

ACS9550T package information


Typical application



TopSync™ ACS9550T in Wireless Network Timing Application

Ordering information

Part number	Description
ACS9550T	TopSync™ Timing-over-packet synchronization ACS9550T.

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