ACS9510 ToPSync™

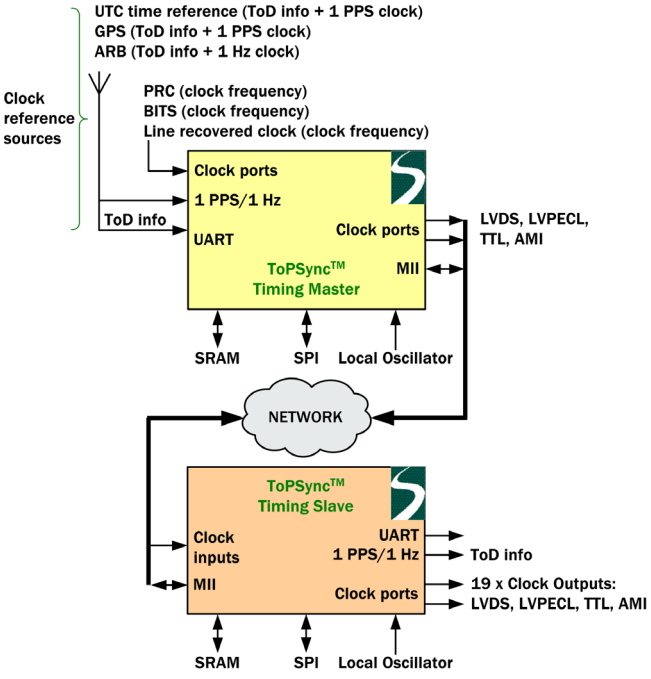
Single-chip master/slave timing synchronization solution for legacy and packet networks

ADVANCED COMMS & SENSING **FINAL PRODUCT BRIEF**

About the ACS9510

The ACS9510 combines Semtech's SETS (TDM timing) and ToPSync™ (PTP timing) technologies to accommodate applications where a remote clock signal must be locked to a central frequency source, or a clock must be aligned to a central time source. TDM timing functionality is used for frequency-locking applications in SDH/SONET/SyncE equipment. ToPSync™ technology transports a reference clock across a packet switched network without special adaptations of switches or routers, and is ideal for carrying timing across a legacy packet-switched network.

System diagram



Standards

The ACS9510 complies with these standards:

[1] IEEE Std. 1588™ (2008).
[2] ITU-T G.812 (06/1998).
[3] ITU-T G.813 (08/1996).
[4] ITU-T G.823 (03/2000).
[5] ITU-T G.824 (03/2000).
[6] ITU-T G.8261/G.8262 (formerly G.pactiming).
[7] Telcordia GR-1244-CORE, Issue 2 (12/2000).
[8] Telcordia GR-253-CORE, Issue 3 (09/ 2000).
[9] RoHS Directive 2002/95/EC.
[10] Waste electrical and electronic equipment (WEEE) 2003.

* This is an indication of Semtech tested performance and is not guaranteed across all types of switches and network conditions. Please contact Semtech ToPSync™ support for further details.

Features

PTP timing features

- **PTP Grandmaster selection** - automatic or manual PTP master/slave mode selection.
- **Powerful network delay analysis** - delivers full time-alignment in the slave over hostile networks (including Layer 2 & 3 routed).
- **Dynamic adaptation** - to network delay variations. Network loading change tolerant (ramps and steps).
- **Time alignment** - better than ±1 µs on a managed 5-switch GbE network under G.8261[6] test conditions.*
- **Frequency alignment** - better than ±10 ppb on a managed 5-switch GbE network under G.8261[6] test conditions.*

TDM timing features

- **Programmable TDM Timing bandwidth** - for wander and jitter tracking/attenuation, 0.1 Hz to 70 Hz in 10 steps.
- **Automatic hit-less source switchover** - on loss of input.
- **Output clock phase adjustment** - in 6 ps steps to ±200 ns.
- **Precision holdover** - accuracy better than 3 x 10^{-10} (manual), 7.5 x 10^{-14} (instantaneous). Holdover stability defined by choice of external crystal oscillator.

Device features

- **Fully integrated** - IEEE1588[1] PTP network timed/reference timed solution. Integrates hardware precision timestamping with on-the-fly insertion (no follow-up packets required). Powerful processor and clock recovery algorithm integrated.
- **Timing synchronization on a chip** - supporting transitions from legacy circuit networks to new packet technology.
- **Suitable applications** - Stratum 3, 4E, 4, SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) and Ethernet, IEEE1588[1] PTP.
- **Clocks** - 20 clock inputs and 19 clock outputs.
- **Ports** - MII, SPI-compatible and JTAG.
- **Time-of-day (ToD)** - 1 PPS top-of-second signal plus current-time-since-epoch message.
- **Output characteristics:**

  Time-aligned output pair:
  1 PPS and 125 MHz divided by n (n = 4 to 125000).

  Frequency-aligned outputs:
  1 Hz and programmable frequency 1 kHz to 62.5 MHz.

  Low jitter frequency-aligned outputs:
  n x E1, n x DS1, frame sync + multi-frame sync clocks.
  SONET and SDH OC-n rates: 3.84 MHz to 155.52 MHz.

- **Local oscillator** - operation with XO of frequency accuracy to ±20 ppm or better.
- **BGA package** - 360 pin, 20 mm x 20 mm, 1 mm pitch. Lead-free version - RoHS[9] and WEEE[10] compliant.

Principles of operation

The ACS9510 is a multi-role device with multiple operating modes. All modes support a large number of output clocks that are locked to the selected timebase:

TDM Timed mode - in which the timebase is derived from clocks, or recovered clocks, such as SONET, SDH, PDH, SyncE, BITS, SSU, etc. This mode supports PTP Grandmaster functions that transport the timing to a remote node. The ToD output from a PTP Slave is ToPSync™ time, not UTC or TAI time.

PTP Network Timed mode - where the timebase is obtained from a packet network and the ACS9510 operates as a PTP Slave. In the PTP Network Timed mode, the device cannot support PTP Grandmaster functions because the PTP is in a slave state.

Reference Timed mode - in which timing derives from a local source such as a local oscillator, GPS, or another point of accurate frequency and/or time. This mode supports PTP Grandmaster functions to transport the timing to a remote node. If the reference input contains UTC or TAI (such as GPS), then the PTP Slave output is UTC or TAI. If ToD information is not available at the master, then the PTP Slave delivers ToPSync™ time.

Self Test - in which the device self-checks for consistency, tests the external SRAM for faults, and performs rudimentary checks of the external Ethernet PHYs.

In all modes, a highly accurate timebase holdover operates if the selected reference fails. Also the ACS9510 implements selectable automatic switching between modes - for example, hitless switching between clock references in TDM Timed mode, and automatic switchover to PTP Network Timed mode if all available clocks fail.

The ACS9510 provides timing solutions that deliver a performance better than that required by the G.813[3]/G.823[4]/G.824[5]/G.8261[§]/8262[6] standards. As a PTP Slave, the device can align its timebase with that of the PTP Grandmaster and generate time-of-day signals as well as clock signals. In this state, the device filters packet delay variations and maintains phase/time alignment with the Grandmaster, without the need for PTP assistance in intermediary network nodes (such as boundary clocks or transparent clocks).

Possible applications include:

- Providing a network clock for circuit-emulation service clock-recovery using differential timing (when conventional network timing in PDH/TDM networks is available; or from packet-timing).
- Providing a 5 MHz, 10 MHz or chip-rate clock, allowing wireless operators to migrate to packet-based backhaul technology and eliminate T1/E1 interfaces, while maintaining the required timing to all network elements.
- Providing a 1 PPS signal which is aligned with the timebase of a central Grandmaster clock.
- This supports applications which require a common phase to be available around a network (such as wireless applications using TDD technologies).

At reset, the operating mode can be configured between the TDM Timed, PTP Network Timed, Reference Timed and Self-Test modes by a 2-bit SYSMODE port. In TDM Timed mode, operation is identical to the ACS8520. In the network and reference timed modes, master or slave operation occurs in accordance with the PTP BMC algorithm or via configuration (so that the device can operate with another clock-selection mechanism).

In all modes except Self-Test, the ACS9510 has holdover and free-run features for conditions when no references are available. The stability of the output clocks during self-timing activities depends on the performance of an external oscillator that controls the internal clocks. The oscillator should be chosen to suit the frequency accuracy and phase stability requirements of the application.

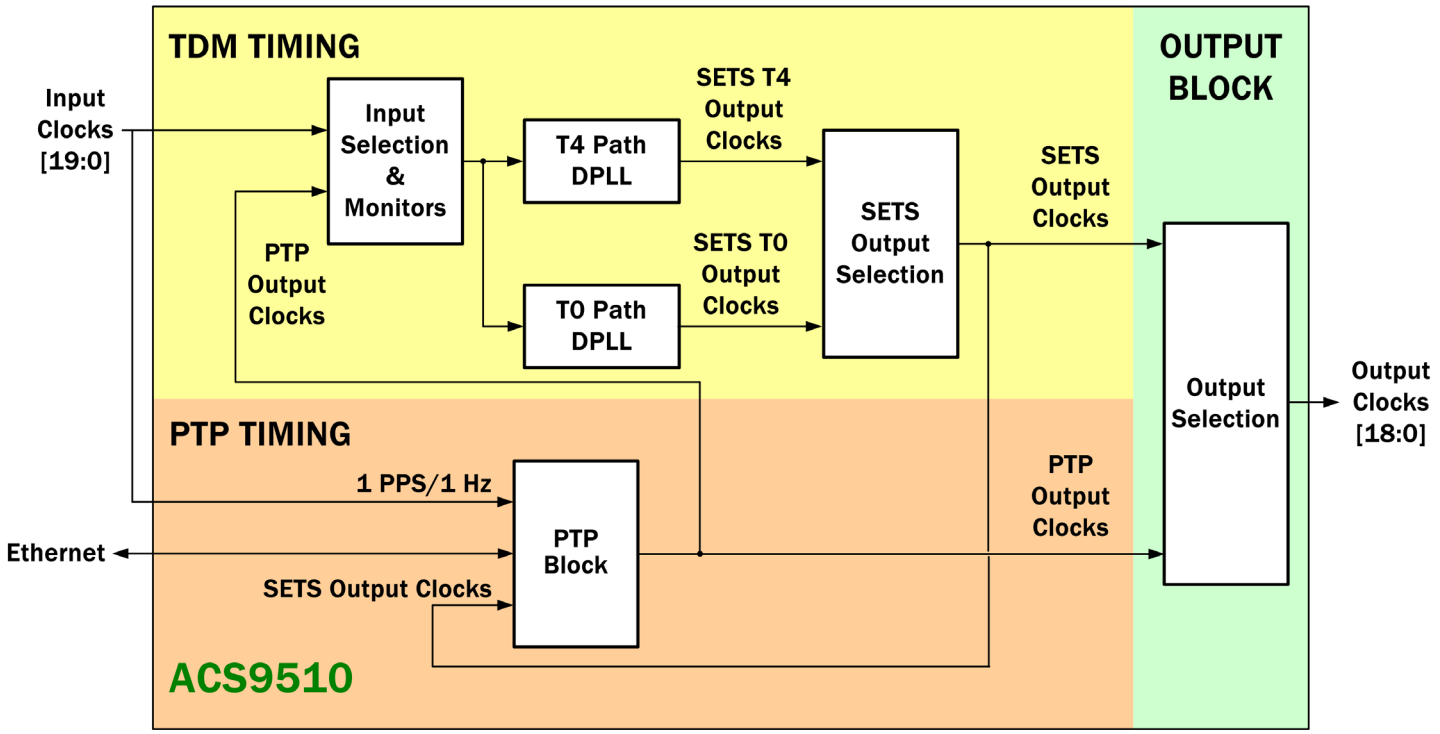
In the network and reference timed modes, the ACS9510 performs all the functions required for a complete, stand-alone, clock recovery system, including hardware time-stamping, PTP protocol, network noise suppression, network re-route accommodation and holdover, and provides outputs for applications that require continuation of frequency, phase and time. A serial peripheral interface compatible port is provided to communicate with a host microprocessor for any configuration and status monitoring that may be required.

Operationally the ACS9510 supports uni-cast communication, and multi-cast PTP network addressing. Quality of service is enhanced by configurable DiffServ codepoint for high priority packet routing.

An API is provided for configuration and status monitoring. The API offers system developers the means to produce appropriate application software to configure and control the ACS9510 and so integrate the required functionality from the device into their synchronization scheme.

The ACS9510 requires 1 MB of SRAM and generic packet PHYs with appropriate termination circuitry.

Block diagram of the ACS9510



TDM timing

Paths T1 (line-recovered clocks) or T3 (station clocks) are used as reference sources to generate T0 (SEC or equipment clock) and T4 (station clock) outputs locked to the selected reference source(s). The T0 and T4 clocks can be generated simultaneously from separate references. All input frequencies are available to both clock paths, and any one input clock is chosen by a selector in each path, where a priority table configured by external software controls which input clock is selected. Each input channel is monitored for activity and frequency offset, input failure, and change of line status or SSM value. If the currently-selected input is disqualified, it is dropped and the input with the next highest priority is automatically used. Noise-transfer, phase-transient-generation, holdover, etc. are within standardized requirements. Protection switching guards the application against local and remote failures.

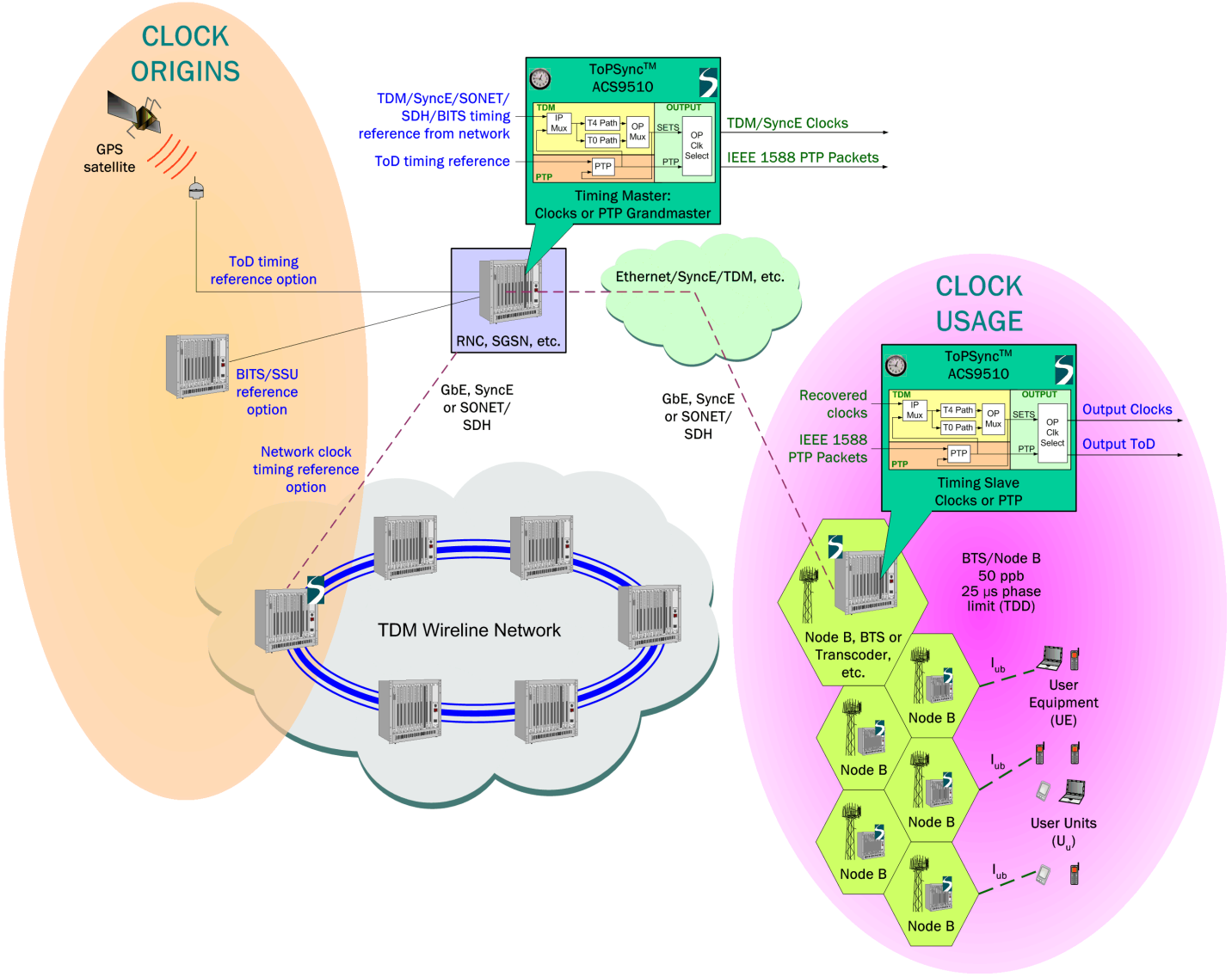
PTP timing

In the PTP Network Timed and Reference Timed modes, the ACS9510 supports the timing requirements of generic packet network applications. The device can act as a PTP Grandmaster or a PTP Slave. The selection between master or slave operation can be automatic, or directly configured. In PTP Grandmaster operation, the ACS9510 communicates with a community of PTP Slaves on the same network. The input reference port consists of input clocks and a UART port. The IPCLK ports are supplied with a 1 PPS signal aligned to the external timebase. The UART port carries timing messages from the external time source. In PTP Slave operation, the ACS9510 receives PTP timing messages from its master clock, timestamps the arrival of PTP event messages, and filters the packet delay variation to deliver a timebase closely aligned to that of the master clock. Conventional clock signals are also generated, with their rate of phase advancement locked to the timebase rate.

Outputs

The 19 output clocks [OPCLK18:0] are obtained by sophisticated multiplexing under the control of API calls. A wide range of output clock frequencies is available. In PTP Network Timed and Reference Timed modes, the frequency of each output clock OPCLK [15:0] is individually programmable via the API. In the TDM Timed mode, the frequency of each output clock OPCLK [7:0] and OPCLK [18:16] is individually programmable via registers.

Typical application

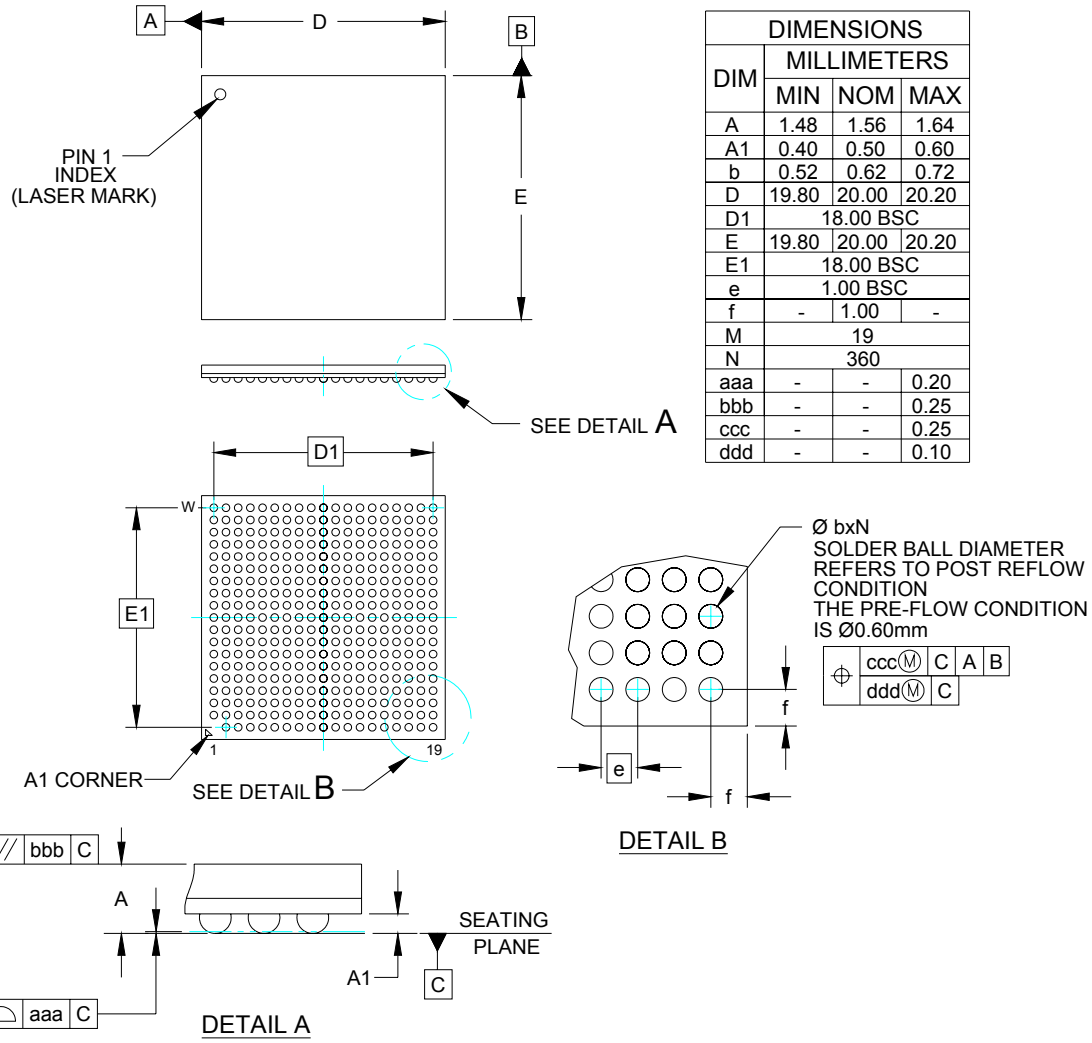


The diagram shows a wireless backhaul application in a legacy network. An ACS9510 master effects the network bridging/ transition, communicating with slaves in the Node B/BTS equipment. For total flexibility, the slaves are ACS9510 devices. If the network uses SyncE/TDM recovered clocks, the slaves can be ACS8520B devices. For applications employing PTP timing only, the slaves can be ACS9593 devices.

Together, the ACS9510 master and the Semtech slave devices synchronize the timing over the entire network, using reference clocks derived from the network itself, or a ToD reference and timing messages (e.g. from a satellite) from the source.

Reference clocks can be routed over the network as generic clocks or packets, and packets can be routed as packets or generic clocks. No modification of the network switching and routing equipment is necessary to accommodate legacy applications or networks built on emerging technology.

ACS9510 package information



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.48	1.56	1.64
A1	0.40	0.50	0.60
b	0.52	0.62	0.72
D	19.80	20.00	20.20
D1		18.00 BSC	
E	19.80	20.00	20.20
E1		18.00 BSC	
e		1.00 BSC	
f	-	1.00	-
M		19	
N		360	
aaa	-	-	0.20
bbb	-	-	0.25
ccc	-	-	0.25
ddd	-	-	0.10

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE AND "N" IS THE NUMBER OF ATTACHED SOLDER BALLS.

Disclaimers & acknowledgements

This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Semtech Corporation reserves the right to make changes to this product without notice. Customers are advised to obtain the latest version of the documentation before placing orders.

Operation of this device is subject to the customer's implementation and design practices. It is the responsibility of the customer to ensure that equipment employing this device is compliant to all relevant standards.

ToPSync™ is a registered trademark of the Semtech Corporation. All other manufacturers' trademarks are hereby acknowledged.

Ordering information

Part number	Description
ACS9510	TopSyncTM Timing-over-packet synchronization technology master/slave 1588 device.
ACS9510T	Lead (Pb)-free packaged version of ACS9510. RoHS and WEEE compliant.

Notes

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