

EVDD430S / EVDD430CY

30A Ultra Fast MOSFET / IGBT Driver Evaluation Boards

General Description

The EVDD430S / EVDD430CY evaluation boards are general-purpose circuit boards designed to simplify the evaluation of the IXYS IXDS430, IXDD430, IXDI430, and IXDN430 MOSFET / IGBT driver, as well as to provide a building block for power circuit development. Any of three IC package types, SOIC-28, 5 lead TO-220, and 5 lead TO-263 are available on two different boards. The board layouts enable the use of MOSFETs or IGBTs in the TO-247, TO-264 or SOT-227 packages and also allow the driven devices to be mounted to a heat sink. In doing so, the board assemblies can be used as a ground referenced, low side power switch for both single-ended and push-pull configurations. The board layout for all three driver packages allows the device tabs to be soldered or strapped to a ground plane for improved cooling in high-power, high frequency applications with large MOSFET devices. The layouts have also been optimized for minimal trace routing and maximized area to reduce inductance and enhance performance.

Figures 1 and 2 are photographs of the front and back of the EVDD430CY board loaded with an IXDI430CI TO-220 driver while figures 3 and 4 show the EVDD430S board equipped with the IXDS430S 28 pin SOIC package. The low level inputs are shown at various points on the boards. The 'Signal In' is a TTL or CMOS level compatible input which controls the on or off state of the power device Q1or Q2. 'Disable' is a optional input, depending on which device is installed, and controls the Tri-State output (IXDD430, and IXDS430 devices only). The Tri-State mode could be used in a motor drive circuit in which an over current could be detected and then a disabling signal fed back, to control the turn off of an IGBT at a slower rate through a seperate 'bleed off' resistor. The 'VCC-IN' is the low voltage (8.5-35V) supply input. Figures 5 and 6 illustrate the mounting of a TO-247, TO-264, SOT-227 power devices.

Circuit Operation

The schematic diagrams for the evaluation boards are shown in Figures 8 and 9. The external drive signal is applied to 'Signal In' test point. The PCBs also provide solder pads across the 50 Ohm input resistor R4 so that a coax can be soldered directly to the board. The PCBs have been designed in an attempt to minimize parasitic inductance associated with long and narrow traces. Large attachment points have been provided so that the user can connect larger wire or copper strap to minimize loop inductance. The diode, resistor combination of DA and RA provides a controlled rate discharge path for the gate of the power device when the Enable function forces the driver into its Tri-State mode. In this mode, the turn-off time of the power device is determined by the time constant of the input gate capacitance $\mathbf{C}_{\text{\tiny iss}}$ and the value of the resistor RA. RA has not been loaded so that the user may choose the value which best suits the design.

The drive output is attached to the MOSFET / IGBT via the gate drive resistor positions. The resistors can be replaced with values to optimize the turn on, turn off performance of the design. The IXDS430S also includes seperate drive output source / sink pins and the EVDD430S evaluation board is arranged such that the turn on rate can be different from the turn off rate via the seperated output pins of the device. The IXD_430 C and Y output pins are internally connected and have just one set of gate resistors.

Finally, the devices are available with an undervoltage trip point of 8.5V or 11.75V, see order table. If the supply voltage dips below this fixed point, drive to the power device is disabled. This feature is selectable on the EVDD430S PCB by way of JP2 while JP1 provides the option to invert the drive signal.

Ordering Information					
Part Number	Companion Device (1)		Options		
EVDD430CI	IXDD430CI	TO-220	UV = 11.75	NI with Enable	
EVDD430MCI	IXDD430MCI	TO-220	UV = 8.5	NI with Enable	
EVDD430YI	IXDD430YI	TO-263	UV = 11.75	NI with Enable	
EVDD430MYI	IXDD430MYI	TO-263	UV = 8.5	NI with Enable	
EVDI430CI	IXDI430CI	TO-220	UV = 11.75	Inverting	
EVDI430MCI	IXDI430MCI	TO-220	UV = 8.5	Inverting	
EVDI430YI	IXDI430YI	TO-263	UV = 11.75	Inverting	
EVDI430MYI	IXDI430MYI	TO-263	UV = 8.5	Inverting	
EVDN430CI	IXDN430CI	TO-220	UV = 11.75	NI	
EVDN430MCI	IXDN430MCI	TO-220	UV = 8.5	NI	
EVDN430YI	IXDN430YI	TO-263	UV = 11.75	NI	
EVDN430MYI	IXDN430MYI	TO-263	UV = 8.5	NI	
EVDS430SI	IXDS430SI	28 pin SOIC	UV / Invert =	Selectable w/ Enable	

UV = Under Voltage Trip Point, NI = Non Inverting

(1) Companion device to be mounted by user.



Figure 1 EVDD430CY Evaluation board with 5 lead TO-220 driver installed.



Figure 3 EVDD430S Evaluation board.

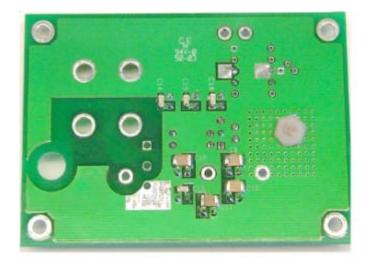


Figure 2 EVDD430CY Evaluation board, back side.

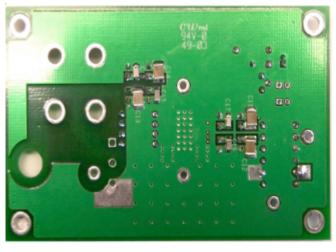


Figure 4 EVDD430S Evaluation board, back side.

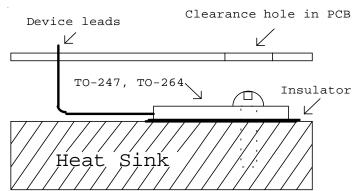


Figure 5 Evaluation board side view showing a power device installed in a high power configuration.

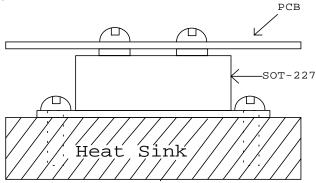


Figure 6 Evaluation board side view showing a SOT-227 power device installed in a high power configuration.

Input	Function	
Vcc In	Supply 8V-35V	
GND	Ground	
Signal In	External drive signal	
Disable	High for device disable	
INV**	Output inversion	
UVSEL**	Under voltage select	

The Evaluation Boards are supplied with either IXDD408YI, IXDD409YI, IXDI409YI, IXDN409YI or IXDD414YI 5-Pin TO-263 devices installed, depending upon the evaluation board part number ordered. To use the evaluation board with a different package type, the installed device must be removed, and the new device installed in the appropriate location.

** Available on the EVDD430S board only

Figure 7 - PCB Connection Table C13 C15 C17 C18 11 C14 0.47UF 50V C12 JP1 open for non-inverted output, jumpered for inverted 50V 50V 50V 50V 50V 50V 50V JP2 open for UVSEL at 12.5V, jumpered for 8.5V 0.01UF C_{2} \ddot{S} 2 CS 90 . C 83 60 U1 100V 10UF 35V 35V 35V 35V 35V 35V 0UF 35V 0UF 35V 27 IUF. R3 26 JP1 JP2 2K Vcc Vcc 25 R7 Drain 24 N/C OUT P 23 OUT P UVSEL R8 N/C OUT P R11 220 OUT N 21 INI 20 9 EN OUT N R9 1 Q2 SOT-227 OUT N 19 2N7000 10 INV R1 100 11 18 R10 1 GND GND 12 GND 17 GND 13 GND R6 16 GND 14 GND 15 GND R4 R2 49 9 1K Not Loaded (TP2) Figure 8 EVDD430S Schematic Diagram NPO C13 C14 C15 C16 50V C10 0.47UF 50V C11 50V C12 0.47UF 50V C9 0.01UF 50V NPO NPO NPO Vcc In (TP1) 0.01UF 5 90 5 C_{2} $^{\circ}$ 2 C2 85 35V 35V 35 35V 357 35V 35V 10UF 35V 100F R3 10K U1/U2 CI / YI package R1 Q2 T0-247 P1 Vcc P2 0 J**⊑** 93 SOT-227 R7 240 94 IN R2 1 95 EN Q1 2N7000 Disable R4 49.9 R6 1K Not Loaded

Figure 9 - EVDD430CY Schematic Diagram

NOTE: The schematic shows two MOSFET devices. However only one device can be installed at any time.

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