EVDD404
IXDD404, IXDI404 And IXDN404 Gate Driver IC Evaluation Board

General Description

The EVDD404 evaluation board is a general-purpose circuit board designed to simplify the evaluation of the IXYS IXDD404, IXDI404 and IXDN404 gate drive ICs, as well as to provide a building block for power circuit development. Either the DIP-8 (PI) or SO-16 (SI-16) gate driver package types may be installed in the driver (the DIP-8 package is factory installed). The board enables the user to drive MOSFETs or IGBTs in TO-220, TO-247, TO-264 or SOT-227 packages. The evaluation board design allows these MOSFETS to be attached to a heat sink, and in so doing the board assembly can be used as a ground referenced, low side power switch for both single-ended and push-pull configurations. Circuitry for the Tri-State function is included on the evaluation board.

Figure 1 is a photograph of the IXDD404 Evaluation Board loaded with an IXDD404PI DIP-8 driver and a SOT-227 MOSFET. The low level inputs are shown on the left side of the board. CONTROL is a TTL high true input which controls the on or off state of the power switch Q1, Q2, or Q3. ENABLE is a low true input, which controls the Tri-State output. (The Tri-State output is not used with the IXDI404 and IXDN404 ICs). VCC-IN is the low voltage, (8-25V) power input, (see Figure 3 below). Figure 2 illustrates the MOSFET mounting of a TO-220, TO-247, or TO-264 device. The MOSFET is mounted on the back side of the PCB. A large through hole is provided so that the device can be attached to a heat sink. The SOT-227 (shown in the photograph) is mounted in a similar manner.

Circuit Operation

The schematic diagram for the evaluation board is shown in Figure 4. The control gate is applied to R4 then on the input pins 2 and 4 of the IC U1 (or to pins 2 and 7 of U2, if loaded in place of U1). This signal input is followed in time by the output pins 5 and 7 of U1 (or pins 10, 11, 14 and 15 of U2, if loaded). Pins 1 and 8 of U1 and U2 are attached to +VCC via a de-coupling network comprised of R1, C3 and R10, C4. Pin 3 of U1 and pins 4 and 5 of U2 are attached to the circuit ground plane. This is the preferred arrangement of the bypassing for the Vcc input power. The enable pins 1 and 8 of U1 and U2 are attached to the drain of Q4. This device is used to level translate and provide an invert function for the Tri-State mode. The drain of Q4 is also attached to the gate of the MOSFET thru RA1 and DA1. In the Tri-State mode the turn off time of the power MOSFET is determined by the time constant of the input gate capacitance C_{iss} and the value of the resistor RA1. See the IXDD404 data sheet for additional information on this mode of operation.

The U1 output is available at pins 5 and 7 of U1 (or pins 10, 11, 14 and 15 of U2, if loaded). These are attached to the MOSFET via the two one-Ohm resistors R5 and R7. The values of these resistors may be changed to optimize the performance of the specific device being driven. The board is designed to parallel the two outputs of the IXDD404 IC, generating up to 8A of output current. If only one output channel is desired, the other channel may be disabled by removing either R5 or R7, thereby disconnecting that channel's output from the MOSFET gate.

There are three test points on the board: Control, Gate and Drain. These allow the user to easily attach an oscilloscope probe and the associated ground to the circuit to verify performance.

Figure 1 - EVDD404 Evaluation Board
SOT-227 Device Installed For Illustration Purposes Only

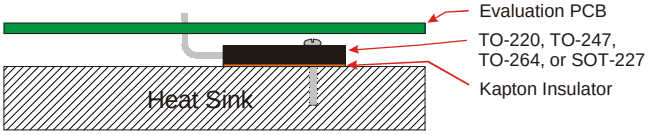


Figure 2 - EVDD404 Side View Showing Power Device Installed In A High-Power Configuration

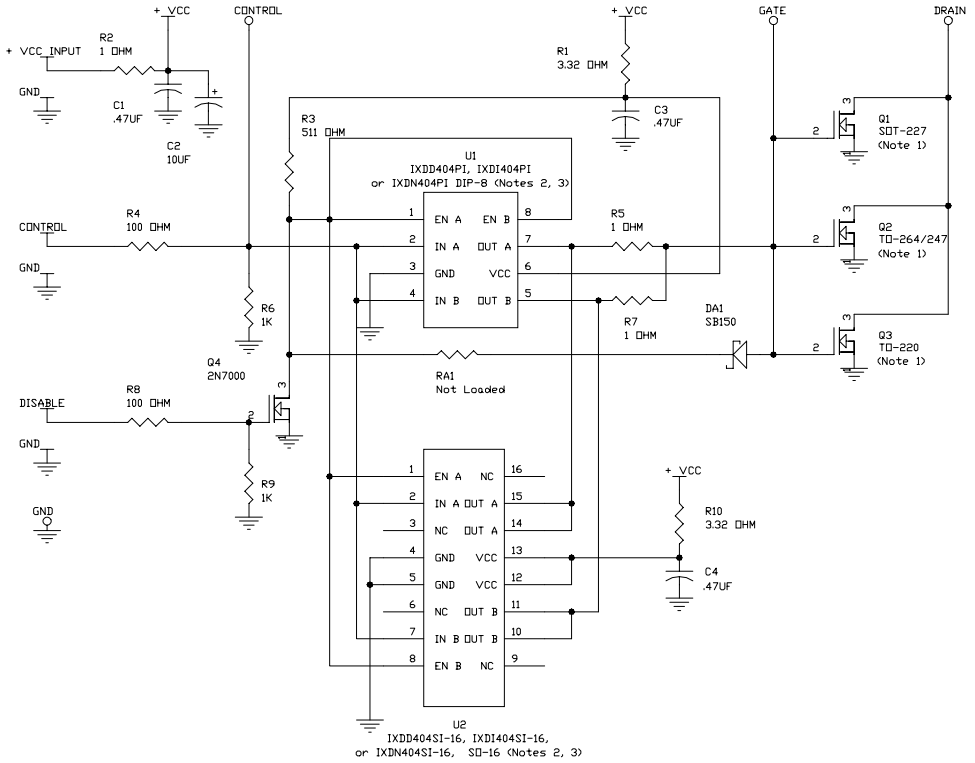
INPUT	FUNCTION
CONTROL	Control Input - 3V into 1K Ohms
GND1	Ground 1
ENABLE	LOW = True, HIGH = Tri-State Mode
GND2	Ground 2
VCC-IN	VCC input - 8V to 25V
GND 3	Ground 3

Figure 3 - Input Pin-Out Table

The EVDD404 is supplied with the DIP-8 (PI) device installed. To use the evaluation board with a different package type, the installed device must be removed, and the new device installed in the appropriate location.

ORDERING INFORMATION	
Part Number	**Installed Device**
EVDD404	IXDD404PI DIP-8
EVDI404	IXDI404PI DIP-8
EVDN404	IXDN404PI DIP-8

Figure 4 - EVDD404 Schematic Diagram



NOTES: 1) The schematic shows all three output switches, however only one device can be installed at any one time.
2) U1 reflects the DIP- 8 package type (PI), and U2 reflects the SO-16 (SI-16) package type. However only one device may be installed and used in the evaluation board at one time.
3) The EN (Enable) pin is not used with the IXDI404 and IXDN404 devices.

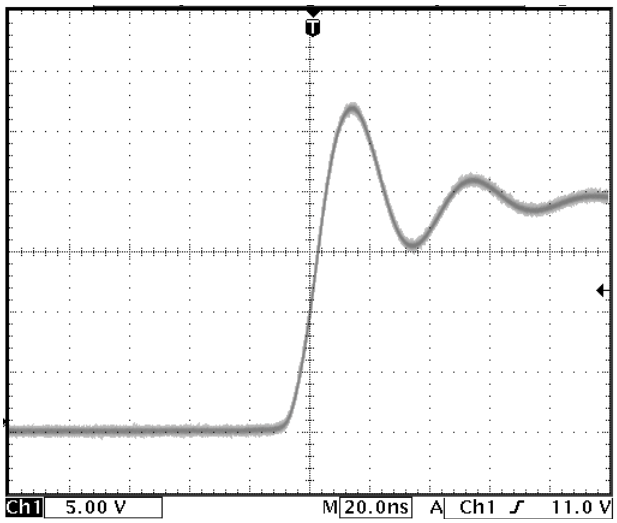


Figure 5 - IXDD404 10ns Gate Rise Time
CL=1800pF

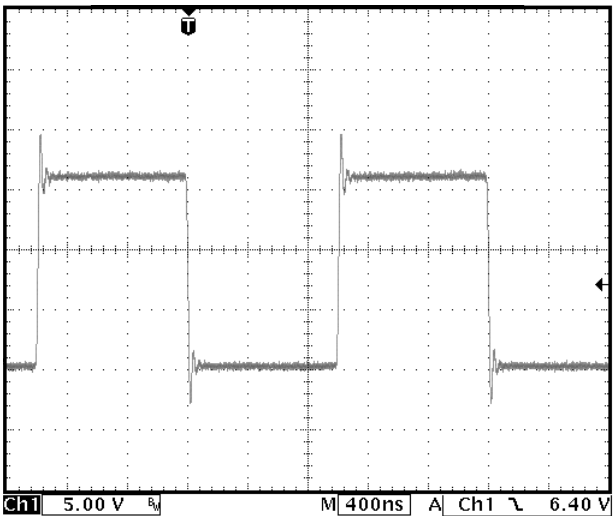


Figure 6 - IXDD404 Typical Output Waveform
F=500KHz, CL=1800pF

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