LMK04000 Family

Precision Clock Conditioner with Dual PLLs and Integrated VCO
Evaluation Board Operating Instructions

National Semiconductor Corporation
Interface Division
Precision Timing Devices

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General Description

The LMK040xx Evaluation Board simplifies evaluation of the LMK040xx Precision Clock Conditioner with Dual PLLs and Integrated VCO. Configuring and controlling the board is accomplished using National Semiconductor's *CodeLoader* software, which can be downloaded from the following URL:
http://www.national.com/analog/timing/codeloader

The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The *CodeLoader* software is used to program the internal registers of the LMK040xx device through a MICROWIRE™ interface.

The following block diagram illustrates the functional architecture of the LMK040xx clock conditioner. It features a cascaded, dual PLL arrangement, available internal loop filter components for PLL2, internal VCO with PLL2 for frequency synthesis, and clock distribution section with individual channel dividers and delay adjustment blocks. The dual reference clock input to PLL1 provides fail-safe redundancy for phase locked loop operation. The cascaded PLL architecture allows PLL1 to be used as a jitter cleaner for an incoming reference clock that contains excessive phase noise. This requires the user to select an external oscillator (VCXO or crystal) that provides the desired phase noise performance at the output of the clock channels. This external oscillator becomes the reference clock for PLL2 and along with the phase noise characteristics of PLL2 and the internal VCO, determines the final phase noise performance at F_{OUT} and the output of the clock distribution section.

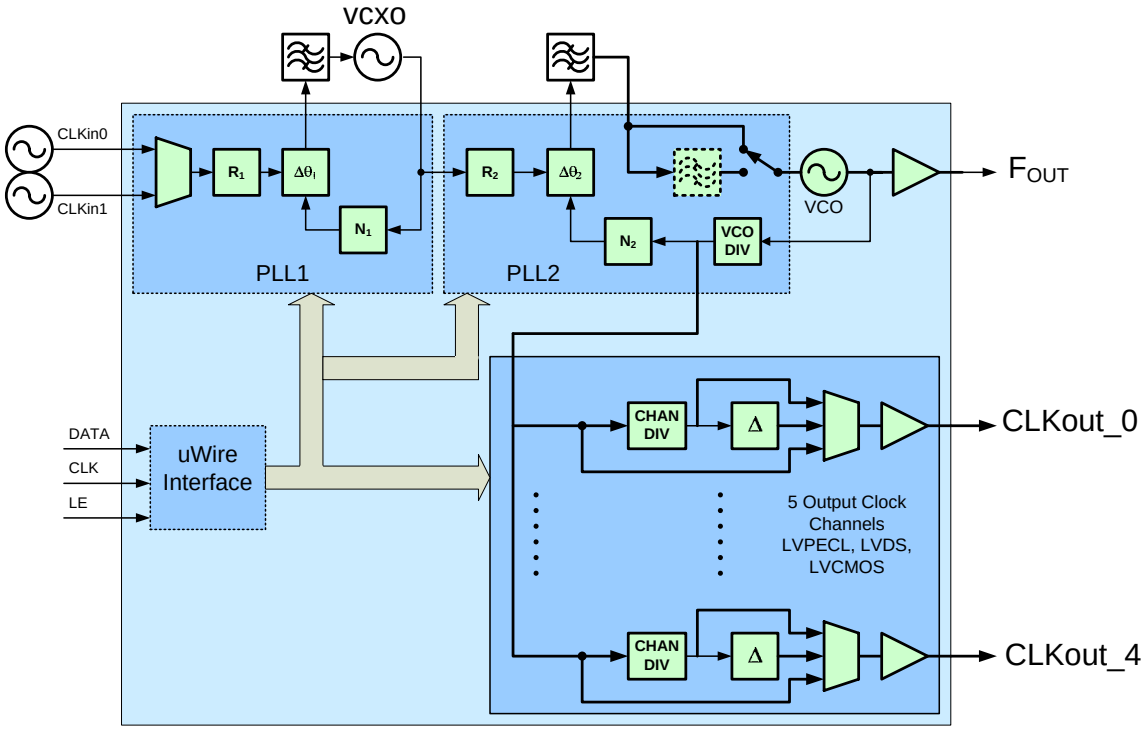


Figure 1. Functional Block Diagram of the LMK040xx Dual PLL Precision Clock Conditioner with External VCXO module.

PLL1 has been designed to work with either an off-the-shelf VCXO package or with a user-designed discrete implementation that employs a crystal resonator and associated tuning components. The following block diagram shows an example of a discretely implemented VCXO using a crystal resonator.

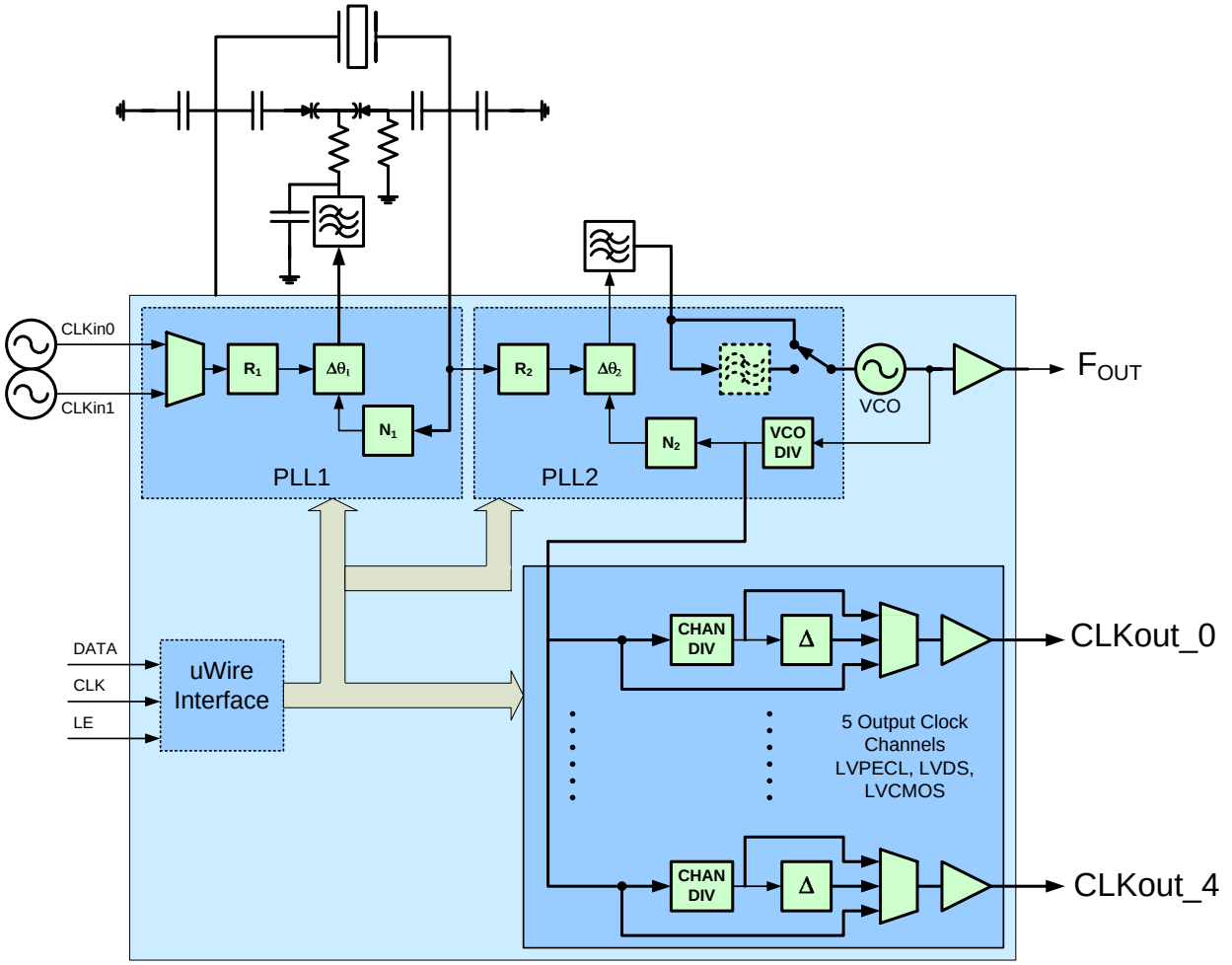


Figure 2. LMK040xx with the XTAL Resonator option and Tuning Circuit

LMK040xx evaluation boards are typically configured with both a VCXO and crystal-based oscillator circuit. The VCXO frequency may either be 100 MHz or 61.44 MHz. The crystal frequency is typically 12.288 MHz. These evaluation board instructions apply to either configuration. Figure 3 illustrates the oscillator circuit based on a pullable crystal resonator.

Note: only one of the oscillators (VCXO or crystal) is activated in the default board configuration. The user may switch between oscillator types by removing and replacing certain components on the board. Instructions for modifying the board are presented in Appendix G.

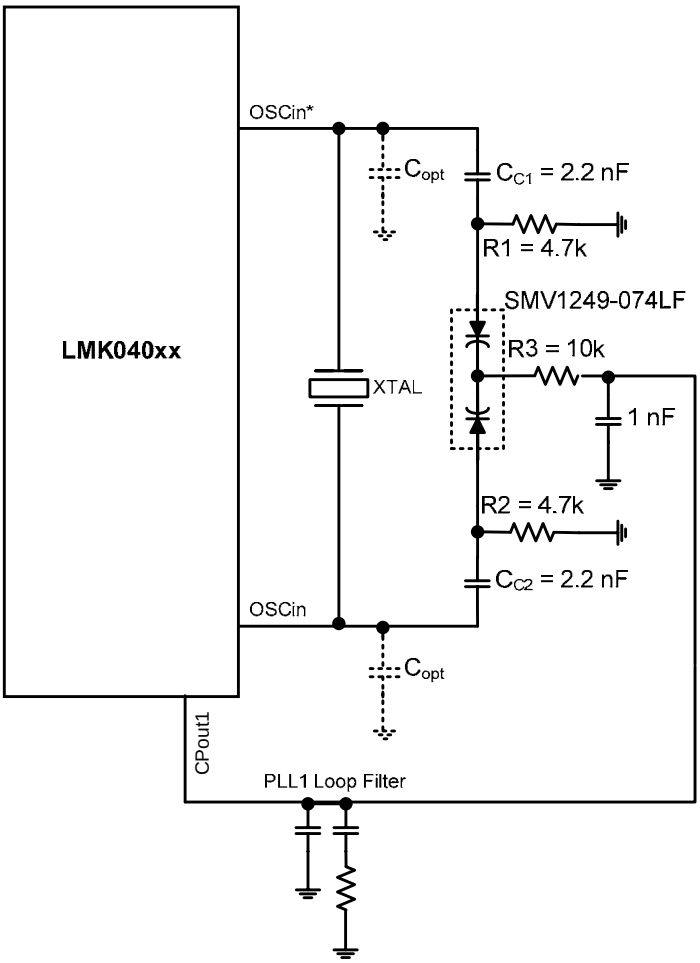


Figure 3. XTAL Oscillator Circuit diagram

The following image shows the VCXO version of the board.

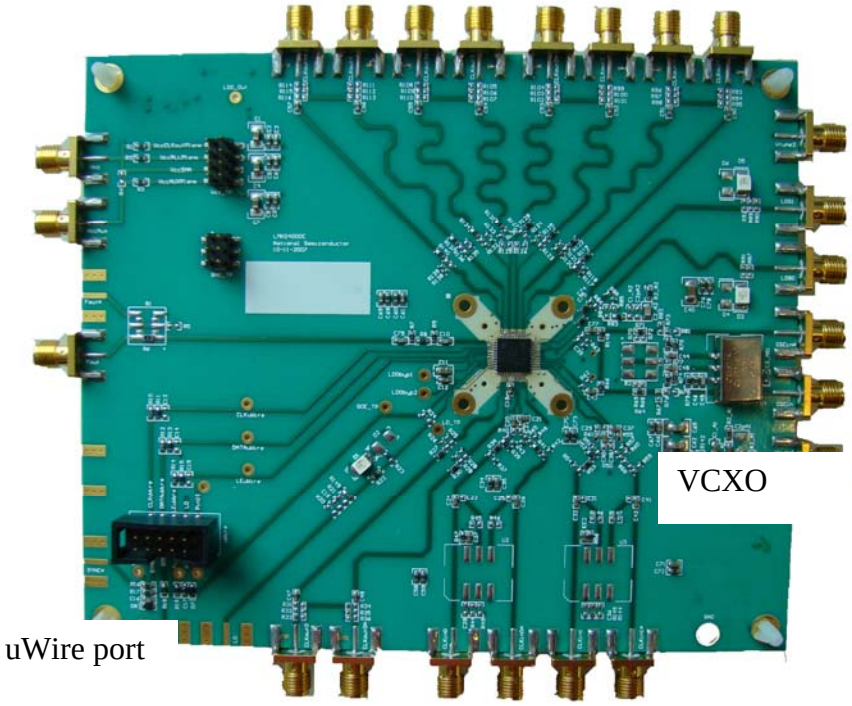


Figure 4. LMK040xx Evaluation board with On-board VCXO Module.

The next image shows the board with crystal installed. The surface mount crystal is installed on the bottom side of the board, along with the other components of the oscillator.

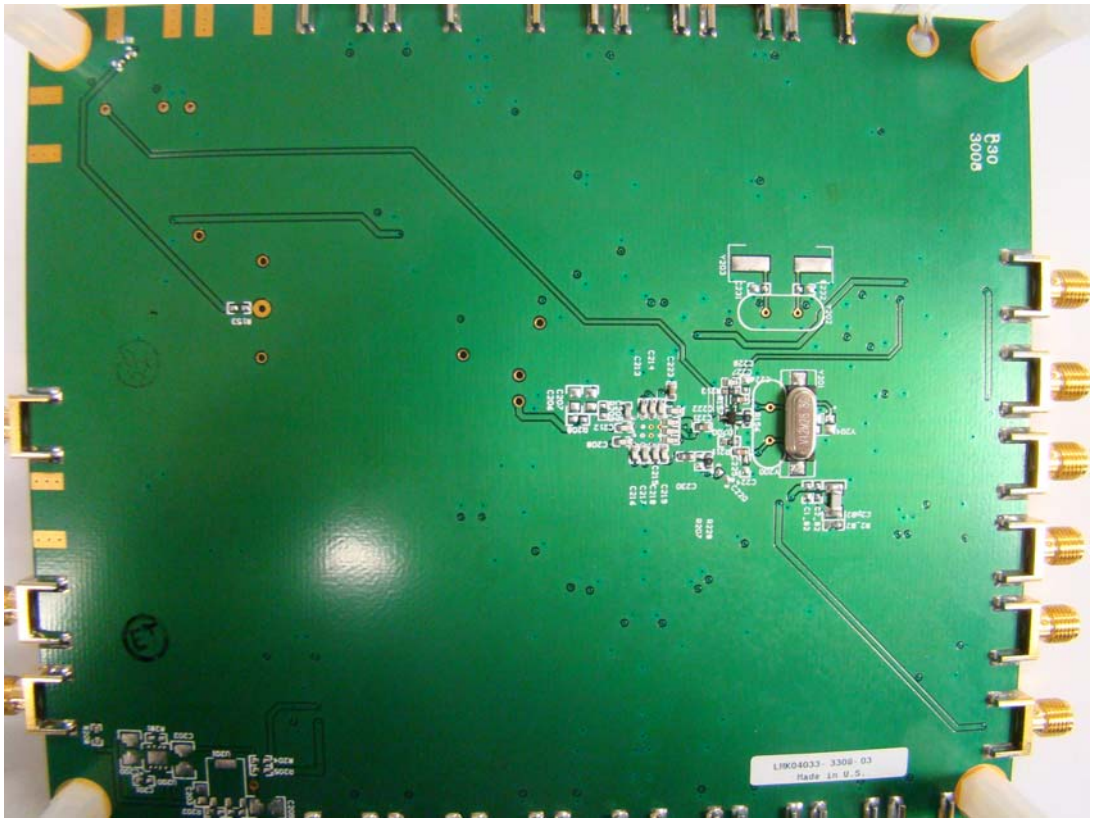


Figure 5. LMK040xx Evaluation Board with XTAL Resonator

The following table illustrates the clock output options for the LMK040xx family.

Table 1. LMK040XX Clock Output Configuration

Part Number	CHAN0	CHAN1	CHAN2	CHAN3	CHAN4	VCO Frequency
LMK04011BISQ	LVPECL/ 2VPECL	LVPECL/ 2VPECL	LVPECL/ 2VPECL	LVPECL/ 2VPECL	LVPECL/ 2VPECL	1430 MHz – 1570 MHz
LMK04031BISQ	LVDS	LVPECL/ 2VPECL	LVCMOS	LVPECL/ 2VPECL	LVDS	1430 MHz – 1570 MHz
LMK04033BISQ	LVDS	LVPECL/ 2VPECL	LVCMOS	LVPECL/ 2VPECL	LVDS	1840 MHz – 2160 MHz

Note: LVPECL/2VPECL is software programmable.

Evaluation Board Kit Contents

The evaluation board is typically shipped with a parallel port cable that is used to interconnect the board to a PC LPT port, enabling the board to be programmed. The kit may also include one or more BALUN boards. Each BALUN board is configured to accept a differential signal input and provide a single-ended signal output. This enables the differential clock outputs of the LMK040xx to be connected to test equipment or to drive single-ended circuits. The user should be aware that there is some attenuation of the clock signal when using these boards.

Appendix F contains typical frequency response data for the BALUN boards.

NOTE: If the board contains an ADT2-1T BALUN, DC bias on the input signals is blocked at the output. If the board contains an ADTL2-18, DC bias on the input will be passed to the output. This may be unacceptable for some types of test equipment.

PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded PLL architecture, the first PLL affectively substitutes the phase noise of a low noise oscillator (VCXO or crystal resonator) for the phase noise of a "dirty" reference clock. The first PLL is typically configured with a narrow loop bandwidth in order to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference. If the jitter of the VCXO is superior to that of the reference clock, the loop bandwidth of the second PLL can be made much wider relative to the first PLL.

The loop filters on the LMK040xx evaluation board are setup using this approach. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 100 Hz), while the loop filter of PLL2 has been configured for a wide loop bandwidth (> 50 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. The following tables contain the parameters for PLL1 and PLL2 for each oscillator option. National's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. For more information, please visit:

http://www.national.com/analog/timing/codeloader

Table 2. PLL1 and PLL2 Parameters for Crystal Mode operating with a 12.288 MHz XTAL.

XTAL OSC Option PLL 1 Loop Filter			
Phase Margin	61º	**Kϕ**	100 uA
Loop Bandwidth	10 Hz	**Fcomp**	1024 kHz
Ref Clk Frequency	122.88 MHz	**Output Frequency**	12.288 MHz (To PLL 2)
Supply Voltage	3.3 Volts	**VCO Gain**	1.5 kHz/Volt
Loop Filter Components	C1 = 330 nF	C2 = 10 uF	R2 = 3.9k ohms
XTAL Option PLL 2 Loop Filter			
Phase Margin	66º	**Kϕ**	1600 uA
Loop Bandwidth	54 kHz	**Fcomp**	12.288 MHz
Crystal Frequency	12.228 MHz (From PLL1)	**Output Frequency**	1474.56 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt
Loop Filter Components	C1 = 0	C2 = 6.8 nF	R2 = 2.7k ohms
C3 = 100 pF	C4 = 110 pF	R3 = 0.6k ohms	R4 = 0.2k ohms

Note: PLL Loop Bandwidth is a function of Kϕ, Kvco, N as well as loop components. Changing Kϕ and N will change the loop bandwidth.

Table 3. PLL1 and PLL2 Parameters for VCXO Option, 100 MHz.

100 MHz VCXO option PLL 1 Loop Filter			
Phase Margin	50º	**Kϕ**	100 uA
Loop Bandwidth	20 Hz	**Fcomp**	1 MHz
Ref Clk Frequency	10 MHz	**Output Frequency**	100 MHz (To PLL 2)
Supply Voltage	3.3 Volts	**VCO Gain**	4 kHz/Volt
Loop Filter Components	C1 = 100 nF	C2 = 680 nF	R2 = 39k ohms
100 MHz VCXO Option PLL 2 Loop Filter			
Phase Margin	79º	**Kϕ**	3200 uA
Loop Bandwidth	301 kHz	**Fcomp**	50 MHz
VCXO Frequency	100 MHz (From PLL1)	**Output Frequency**	1500 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt
Loop Filter Components	C1 = 0	C2 = 12 nF	R2 = 1.8 k ohms
C3 = 0	C4 = 10 pF	R3 = 0.6k ohms	R4 = 0.2k ohms

Note: PLL Loop Bandwidth is a function of Kϕ, Kvco, N as well as loop components. Changing Kϕ and N will change the loop bandwidth.

Table 4. PLL1 and PLL2 Parameters for VCXO Option, 61.44 MHz

61.44 MHz VCXO option PLL 1 Loop Filter			
Phase Margin	50º	**Kϕ**	100 uA
Loop Bandwidth	20 Hz	**Fcomp**	1.024 MHz
Ref Clk Frequency	122.88 MHz	**Output Frequency**	61.44 MHz (To PLL 2)
Supply Voltage	3.3 Volts	**VCO Gain**	2.5 kHz/Volt
Loop Filter Components	C1 = 100 nF	C2 = 680 nF	R2 = 39k ohms
61.44 MHz VCXO PLL 2 Loop Filter			
Phase Margin	74º	**Kϕ**	1600 uA
Loop Bandwidth	185 kHz	**Fcomp**	61.44 MHz
VCXO Frequency	61.44MHz (From PLL1)	**Output Frequency**	1474.56 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt
Loop Filter Components	C1 = 0	C2 = 12 nF	R2 = 1.8 k ohms

C3 = 50 pF	C4 = 10 pF	R3 = 0.6k ohms	R4 = 0.2k ohms

Note: PLL Loop Bandwidth is a function of Kϕ, Kvco, N as well as loop components. Changing Kϕ and N will change the loop bandwidth.

Quick Setup

CodeLoader and the installation instructions may be downloaded from National's Precision Clock Conditioner web site:

http://www.national.com/analog/timing/codeloader

For basic operation:

1. Connect a low noise **3.3 V** power supply to the **VCC SMA** connector. If there is no jumper between **VccSMA** and **VccAUXPlane**, either install a jumper or connect a 3.3VDC supply to the **VCCAux** SMA Connector located at the top left of the board.

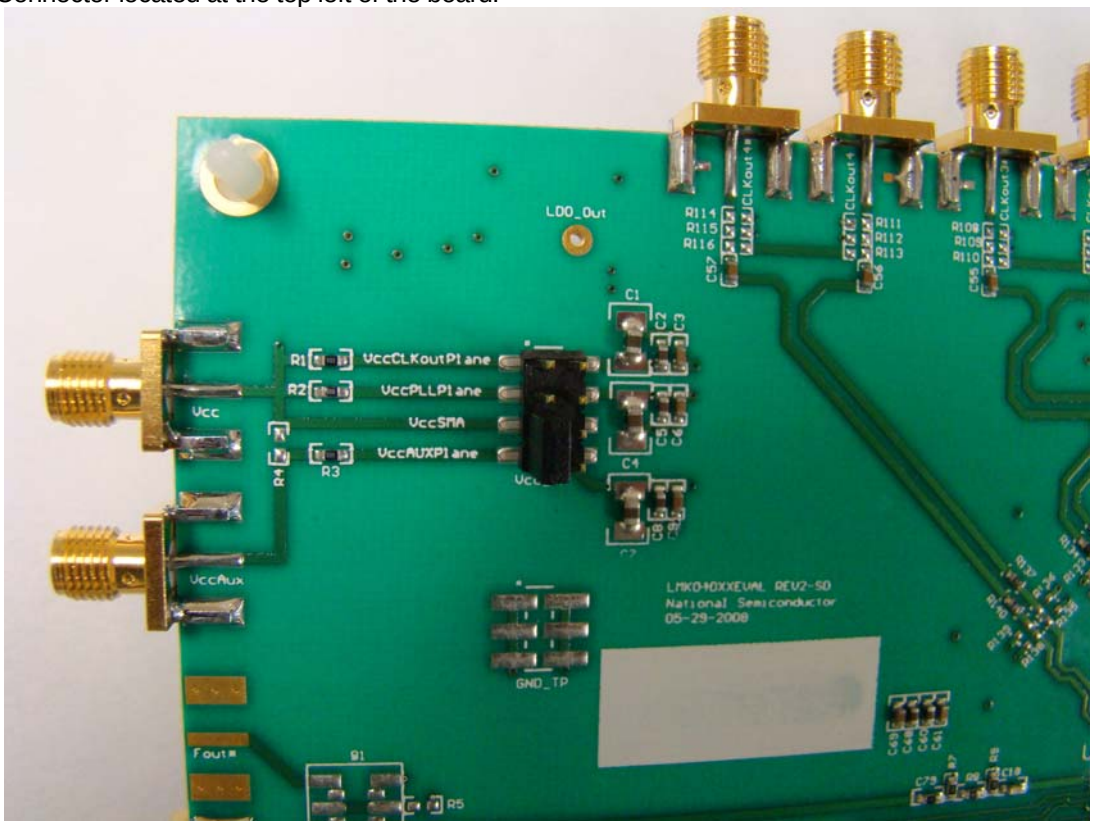


Figure 6. Evaluation Board Power Connectors

2. Connect the programming interface to the board using one of the following options:
   - Option 1, LPT cable: Connect the PC directly to the evaluation board with the LPT-to-uWire cable supplied with the board, plugging the cable into an LPT port on the computer and then the 10 pin ribbon connector to the 10-pin uWire header located on the lower left corner of the evaluation board. **The cable can be removed after programming to minimize noise and EMI.**
   - Option 2, USB cable with adaptor board: Connect the PC directly to the USB interface board using the USB cable. Connect the USB interface board to the evaluation board with the short

flat cable supplied with the board, plugging the cable into the 10-pin uWire header located on the lower left corner of the evaluation board.

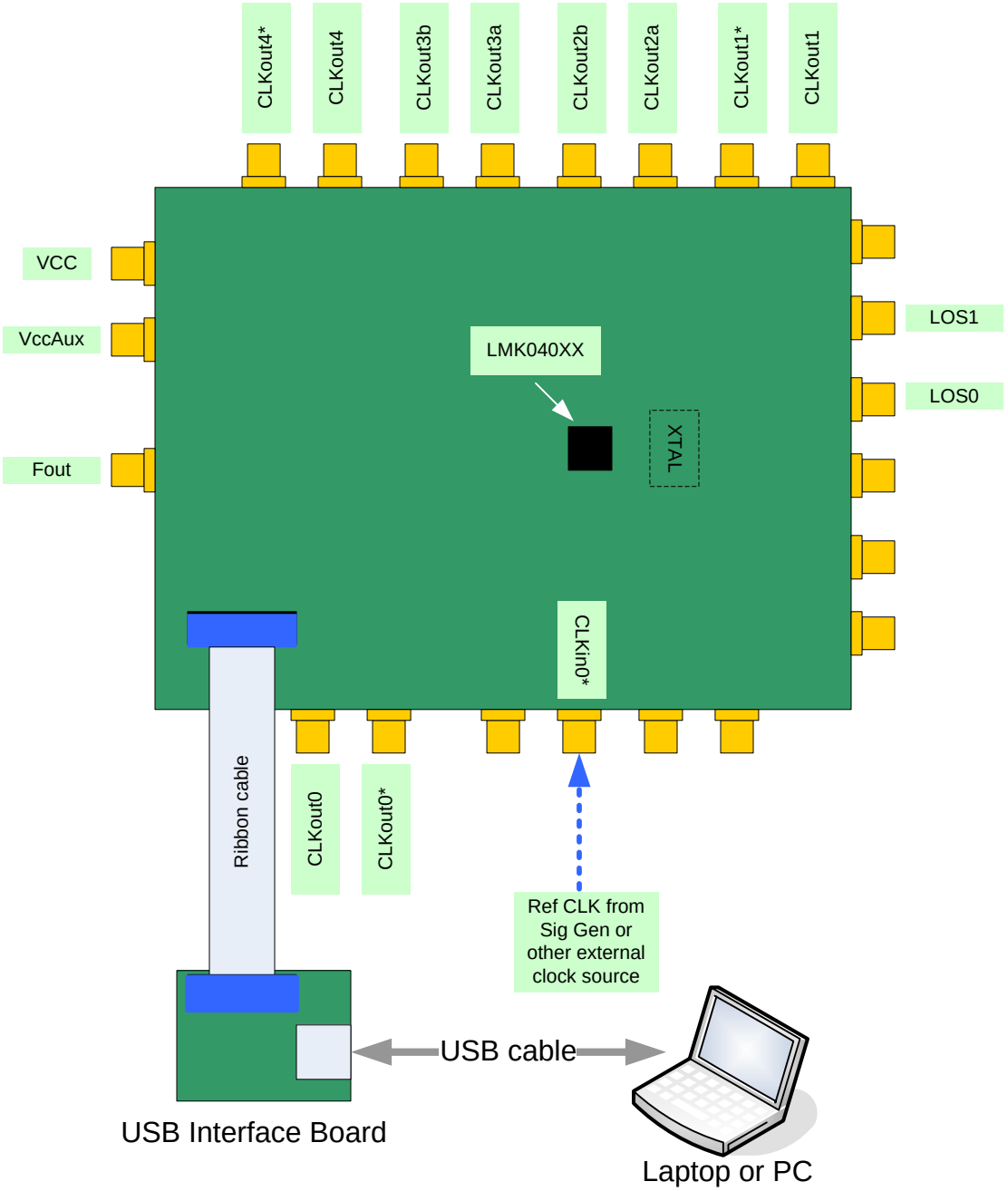


Figure 7. USB Programming Connection

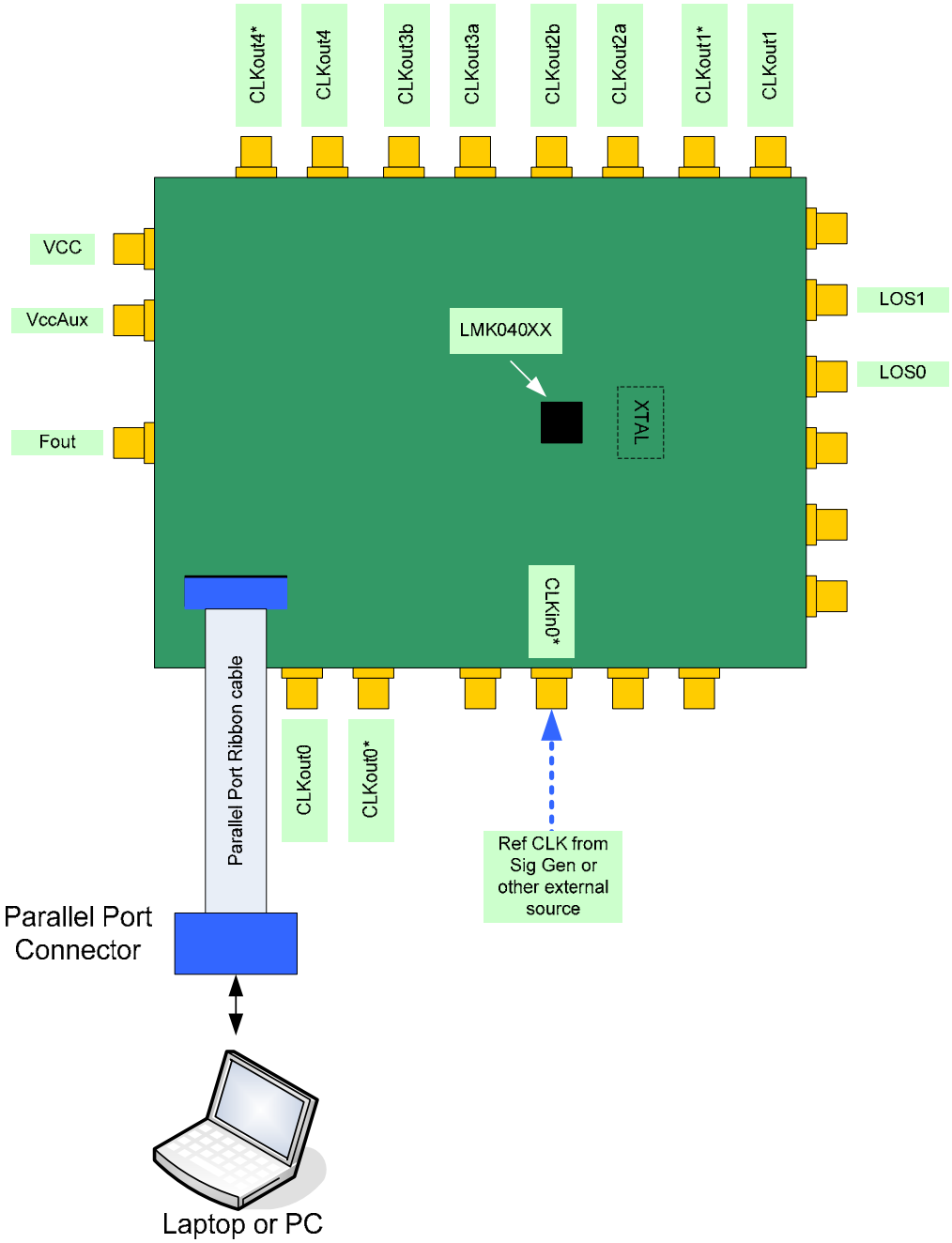


Figure 8. Parallel Port Programming Connection

3. Connect a low noise reference clock source (122.88 MHz for the XTAL option or 61.44 MHz VCXO option, 10 MHz for the 100 MHz VCXO option) to the CLKin0* SMA connector (CLKin0 may be left unconnected, as the default configuration of the board uses a single-ended input for the reference). This is the default reference input. The power level of the reference input should be 6 dBm +/- 1 dBm for best performance. The reference input to the LMK040xx is AC coupled so the reference source may be either AC or DC biased. The default signal path configuration is singled-ended. Using a differential reference source requires modification of the board. A sinusoidal or square signal may be used, though better performance may be obtained with a higher slew rate on the input clock.
4. Install the latest version of CodeLoader from National's web site.

5. Copy codeldr.ini, other *.ini files and *.mac files supplied with the evaluation board into the CodeLoader installation directory. Device specific configuration files include LMK04011.ini, LMK04031.ini and LMK04033.ini. As additional versions of the LMK04000 family are released, they will be accompanied by specific *.ini files.
6. Start CodeLoader. See Appendix A for a brief tour of CodeLoader features.
7. Choose the appropriate device from the **Select Device** drop down menu under the **Clock Conditioners** group.
8. Several common default configurations have been prepared to enable simplified programming of the board. These configurations have been stored in multiple *.mac files that have been supplied with the evaluation board. Table 5 (see next page) lists these configurations. If the user desires to use a custom configuration, it is recommended that one of the *.mac files listed in Table 5 be selected as a starting point. The selected configuration can then be edited and customized to the user's requirements. ***To load a *.mac file***, open the "**File**" menu, then select "**Restore**". If Step 5 above was completed, all *.mac files should be saved in the CodeLoader installation directory on the user's PC. Navigate to this directory, otherwise, navigate to the directory where the files are stored and select the desired file. After a few seconds, the CodeLoader configuration fields will be updated with the settings stored in the file. A user modified *.mac configuration can be saved using the "**Save**" option under the **File** menu.
9. Select the **Bits/Pins** tab. To enable the VCO output pin (F_{out}), check the box labeled "EN_Fout".
10. To enable the individual clock channel outputs, go to the **Clock Outputs** tab. In the Clock Output field, select "Enable" for the desired output clock from the drop down menu corresponding to the relevant clock channel.
11. See Figure 9 through Figure 13 on the following pages for illustrations of the contents and fields contained in each of the CodeLoader configuration tabs.
12. Note: the default communications port is USB. To switch to parallel port (LPT) mode, select the "**Port Setup**" tab, then select **LPT** in the "**Communications Mode**" block, located in the upper left corner of the page. LPT1, LPT2 and LPT3 are available options. USB mode can only be used if a USB interface board is used.
13. After device configuration in CodeLoader is complete, program the LMK040xx by pressing CTRL+L on the PC keyboard or select "Load Device" from **Keyboard Controls** menu. CTRL+L should be pushed after any configuration change.
14. **After programming, the uWire cable can be unplugged from the evaluation board to minimize noise and EMI.**

Table 5. LMK040XX Eval Board and CodeLoader *.mac File Cross Reference

LMK040XX Device family	VCXO / XTAL	VCXO/XTAL Frequency (MHz)	PLL1 Reference clock (MHz)	Configuration file (*.mac)
LMK040X1	VCXO	100	10	Std_LMK040X1_10MHZ_ref_100MHZ_VCXO.mac
LMK040X1	VCXO	61.44	122.88	Std_LMK040X1_122_88MHZ_ref_61_44MHZ_VCXO.mac
LMK040X1	Crystal	12.288	122.88	Std_LMK040X1_XTAL_1X_122_88MHZ_Ref.mac
LMK040X1	Crystal	12.288	122.88	Std_LMK040X1_XTAL_2X_122_88MHZ_Ref.mac
LMK040X3	VCXO	61.44	122.88	Std_LMK040X3_122_88MHZ_ref_61_44MHZ_VCXO.mac

Evaluation Board Notes

1. F_{out} is AC-coupled. A 3 dB pad is installed between the F_{out} pin and the SMA connector. The nominal output level will be -1 dBm.
2. All clock outputs are AC-coupled.
3. All LVPECL/2VPECL clock outputs are terminated to GND with a 120 ohm resistor, one on each output pin of the pair.

Evaluation Board Inputs/Outputs

The following table contains descriptions of the various inputs and outputs for the evaluation board.

Table 6. LMK040XX Evaluation Board I/O

Connector Name	Input/Output	Description
CLKout0 / CLKout0*, CLKout1 / CLKout1*, CLKout2 / CLKout2*, CLKout3 / CLKout3*, CLKout4 / CLKout4*	Output	Differential clock output pairs. See Table 1 for format depending on part number. If LVCMOS, each output can be independently configured (non-inverted, inverted, tri-state, and LOW). All clock outputs are AC-coupled.
Fout	Output	When enabled, buffered VCO output. AC-coupled. The default configuration on the board contains a 3-dB attenuator on the Fout signal.
Vcc	Input	DC power supply for the LMK040xx device. Note: The LMK040xx family contains internal voltage regulators for the VCO, PLL and related circuitry. The clock outputs do not have an internal regulator. A clean power supply is required for best performance.
VccAux	Input	DC power supply for on-board VCXOs, reference oscillators, and Global Output Enable (GOE). Notes: 1. Vcc and VccAux power buses may be interconnected by placing a jumper on the VCC_TP header. 2. VCOs and VCXOs are sensitive to power supply noise. If the board is configured with and on-board VCXO or on-board reference clock, best performance will be achieved if a clean power supply is connected to VccAux.
CLKin0/CLKin0*, CLKin1/CLKin1*	Input	Reference clock inputs for PLL1. The default board configuration is setup for a single-ended reference source at CLKin0* (CLKin0 pin is AC-coupled to ground). The format of the clock input buffer is programmable in CodeLoader on the **Bits/Pins** tab, and may be either bi-polar junction mode or MOS mode. The input power level for an AC-coupled ***differential*** input should be between -2 dBm and +13 dBm for bipolar mode and between +4 dBm and +13 dBm for MOS mode. If either clock input is driven using a ***single-ended*** signal, the signal level should be between -8 dBm and +8 dBm for bipolar mode, and between -2 dBm and +10 dBm in MOS mode. If a DC-coupled clock is used to drive either of the inputs, the peak voltage level must be at least 2 volts and the minimum voltage no greater than 0.4 volts. By default CLKin0 is the active input in either of the auto-switching modes (*CLKin0 non-revertive, CLKin0 revertive*). When loss of CLKin0 is detected, the device automatically switches to CLKin1 if an active reference clock is attached. See data sheet for further explanation.
LOS0, LOS1	Output	Loss-of-Signal indicator (CMOS) for CLKin0/0* and CLKin1/1*. See data sheet for further explanation of the LOS pins.

Connector Name	Input/Output	Description
OSCin/OSCin*	Input	If the evaluation board is not configured with an on-board VCXO module or on-board crystal-based VCXO, an external VCXO may be attached to the OSCin/OSCin* SMA connectors. Either a differential or single-ended device may be used. If a single-end device is used, OSCin* should be tied to GND through a capacitor that matches the AC-coupling capacitor value used for the OSCin pin. Pads for this capacitor are located close to the OSCin* pin. This capacitor is not placed for either of the default configurations of the board. See the LMK04000 data sheet for OSCin port signal specifications.
Vtune1	Output	Tuning voltage output from the loop filter for PLL1. This control voltage should be connected to the voltage control pin if an external VCXO is used. Note: Resistor R143 must be populated with a zero ohm resistor to control an off-board VCXO.
Vtune2	Output	Available to monitor the tuning voltage for the internal VCO. Resistor R84 must be populated with a zero ohm resistor.
uWire	Input/Output	10-pin header programming interface for the board. CLK, DATA and LE signal lines. Each of these signals can be monitored through test points on the board.
LD_TP	Output	Test point attached to the LD pin of the device. The LD pin is attached to a multiplexer inside the device and may be programmed with a variety of internal signals for monitoring internal device functions and troubleshooting. See data sheet for further explanation. The *lock detect* signal is accessible through this pin.

Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply. An Agilent 6623A Triple power supply with LC filters on the output to reduce noise was used in creating these evaluation board instructions.

Phase Noise / Spectrum Analyzer

For measuring phase noise an Agilent E5052A Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052A is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

For measuring delay an Agilent Infiniium DSO81204A was used.

Appendix A
CodeLoader Settings

To view the function of any bit on the CodeLoader configuration tabs, place the cursor over the desired bit register label and click the right mouse button on it for a description.

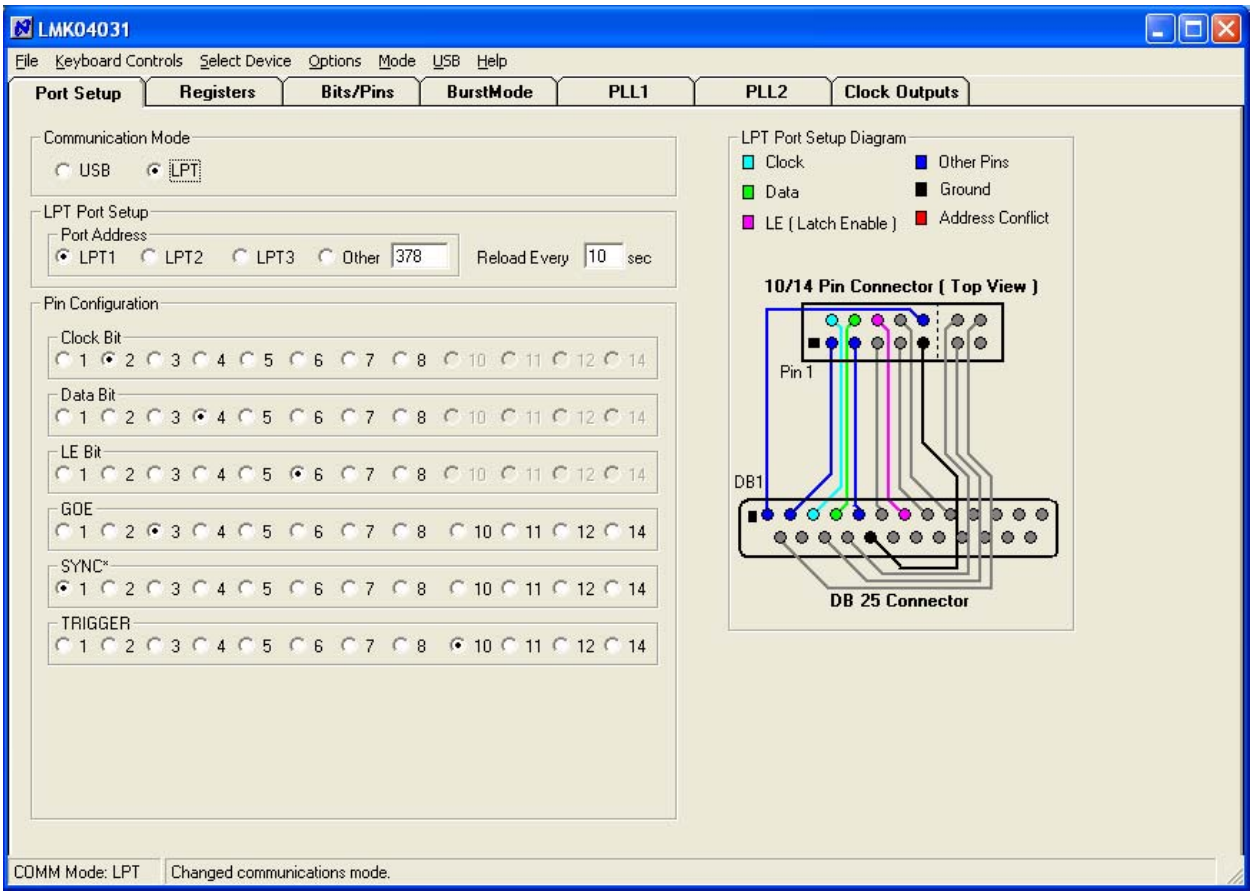


Figure 9. Port Setup tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally SHOULD NOT be changed by the user.

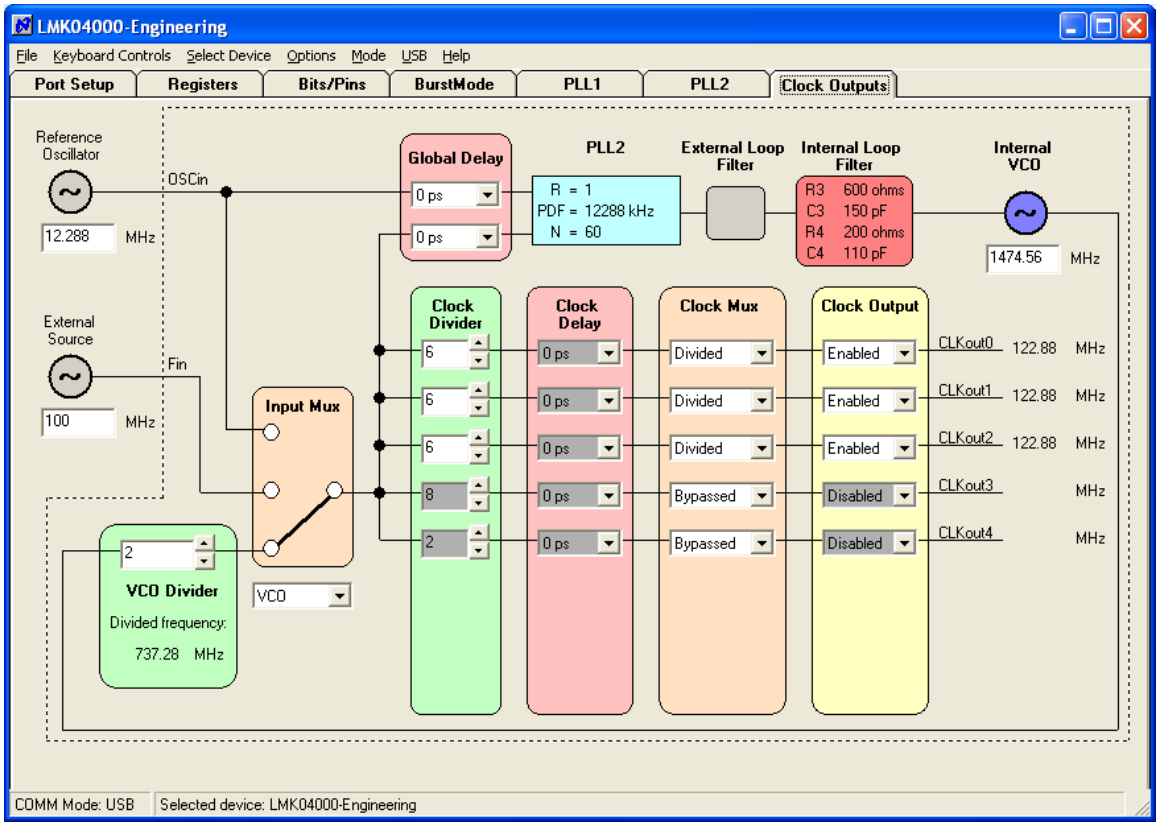


Figure 10. Clock Outputs tab

The clock outputs tab allows the user to Enable/Disable individual clock channels, select the clock mode (Bypass/Divided/ Delayed/ Divided & Delayed), set the channel delay value (if Delay is enabled), and the channel divider value (2,4,6,…,510).

This tab also allows the user to select the VCO Divider value (2,3,…,8). Note that the total PLL2 N divider value is composed of both the VCO Divider value and the N value shown in the blue box in the image, and is given by: N_{TOTAL} = VCO Divider * N.

Clicking on the blue box that contains R, PDF and N values takes the user to the PLL2 tab where these values may be changed.

Clicking on the components in the box containing the Internal Loop Filter values allows the user to change these component values.

The Reference Oscillator value field may be changed in either the Clock Outputs tab or the PLL2 tab. Note this value MUST match the value of the on-board VCXO (or XTAL option).

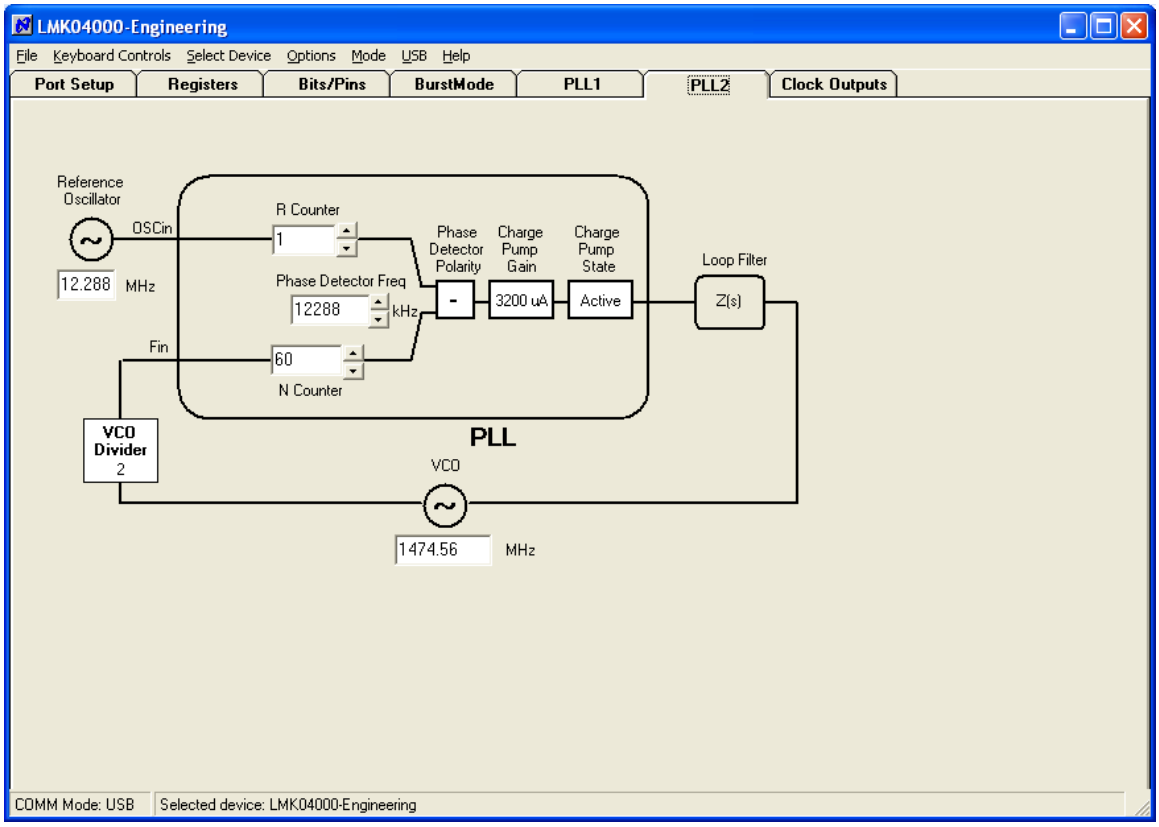


Figure 11. PLL2 tab.

The PLL2 tab allows the user to change:

- VCO frequency
- PLL2 Phase detector frequency
- PLL2 R-counter value
- PLL2 N-counter value
- The frequency of the external VCXO (or XTAL oscillator). ***Note: This value must be entered in both the PLL1 and PLL2 tabs.***
- PLL2 Charge pump gain
- PLL2 Charge pump state.

Any changes made on this tab are reflected in the Clock Outputs tab. Note that the PLL2 Phase Detector polarity is fixed and cannot be changed by the user. Also note that the VCO frequency should conform to the specified frequency range for the device (see Table 1).

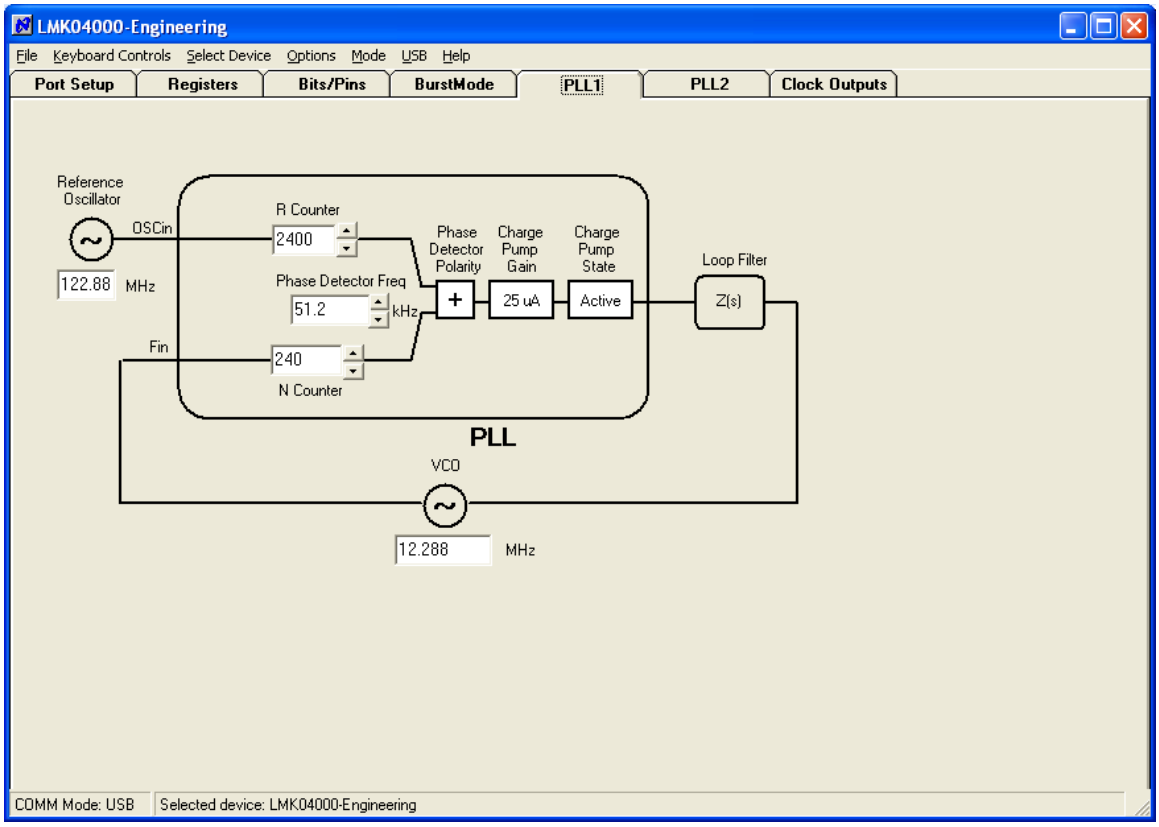


Figure 12. PLL1 tab.

The PLL1 tab allows the user to change:

- External VCXO (or XTAL oscillator) frequency. ***Note: This value must be entered in both the PLL1 and PLL2 tabs.***
- PLL1 Phase detector frequency
- PLL1 R-counter value
- PLL1 N-counter value
- CLKin (Reference) oscillator frequency
- PLL1 Phase Detector polarity (external VCXO tuning slope)
- PLL1 Charge pump gain
- PLL1 Charge pump state.

Note that the value entered in the **Reference Oscillator** frequency field on the PLL1 tab must match the **Reference Oscillator** frequency entered on the PLL2 tab.

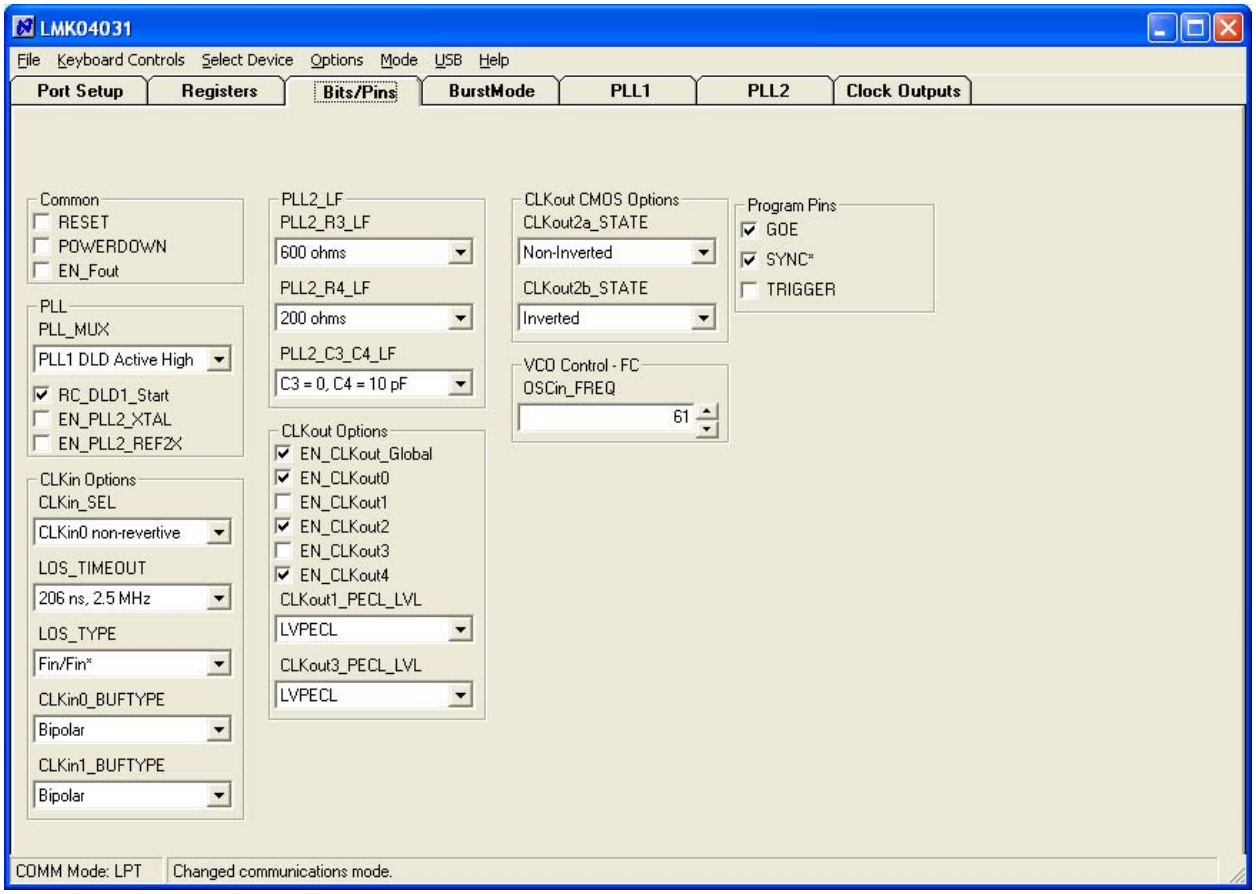


Figure 13. Bits/Pins tab.

The Bits/Pins tab allows the user to:

- setup various clock output options. This will also be reflected on the **Clock Outputs** tab.
- Manipulate GOE and SYNC signal states (through the 10-pin header)
- Select internal loop filter components for PLL2
- Select Reference clock functional mode: CLKin_SEL (Manual or Auto-revertive)
- Select the Loss-of-Signal (LOS) output type (LOS_TYPE).
- Select the reference clock input buffer type: CLKin0_BUFTYPE and CLKin1_BUFTYPE (MOS or Bipolar junction)
- Enable/disable crystal mode: EN_PLL2_XTAL.
- Enable/disable PLL2 reference clock (OSCin) frequency doubler mode: EN_PLL2_REF2X.
- Set the OSCin (VCXO or XTAL) frequency (OSCin_FREQ). **NOTE: This value should match the Reference Oscillator values entered in the PLL1 and PLL2 tabs. It is important to enter the correct frequency value in this field, as it is used by the internal state machine of the LMK040XX to execute its calibration and tuning routine for the internal VCO**. An incorrect value may result in an unlocked condition for the synthesizer.

Appendix B: Typical Phase Noise Performance Plots

The following table lists the test conditions used for the phase noise measurements for the crystal oscillator option:

Table 7 . LMK040XX test conditions, XTAL Oscillator Option

Parameter	Value
PLL1 Reference clock input	CLKin0*, single-ended, CLKin0 AC-coupled to GND
PLL1 Reference Clock frequency	122.88 MHz
PLL1 Phase detector frequency	1024 kHz
PLL1 Charge Pump Gain	100 uA
VCXO frequency	12.288 MHz, Ecliptek ECX-6465
PLL2 phase detector frequency	12.288 MHz
PLL2 Charge Pump Gain	3200 uA
PLL2 REF2X mode	disabled

NOTE: All jitter measurements are for a 100 Hz to 20 MHz integration bandwidth.

The following plot illustrates the phase noise measured at F_{OUT}, CLKout0 (LVDS), CLKout1 (LVPECL), and CLKout2 (LVCMOS) using the XTAL oscillator option.

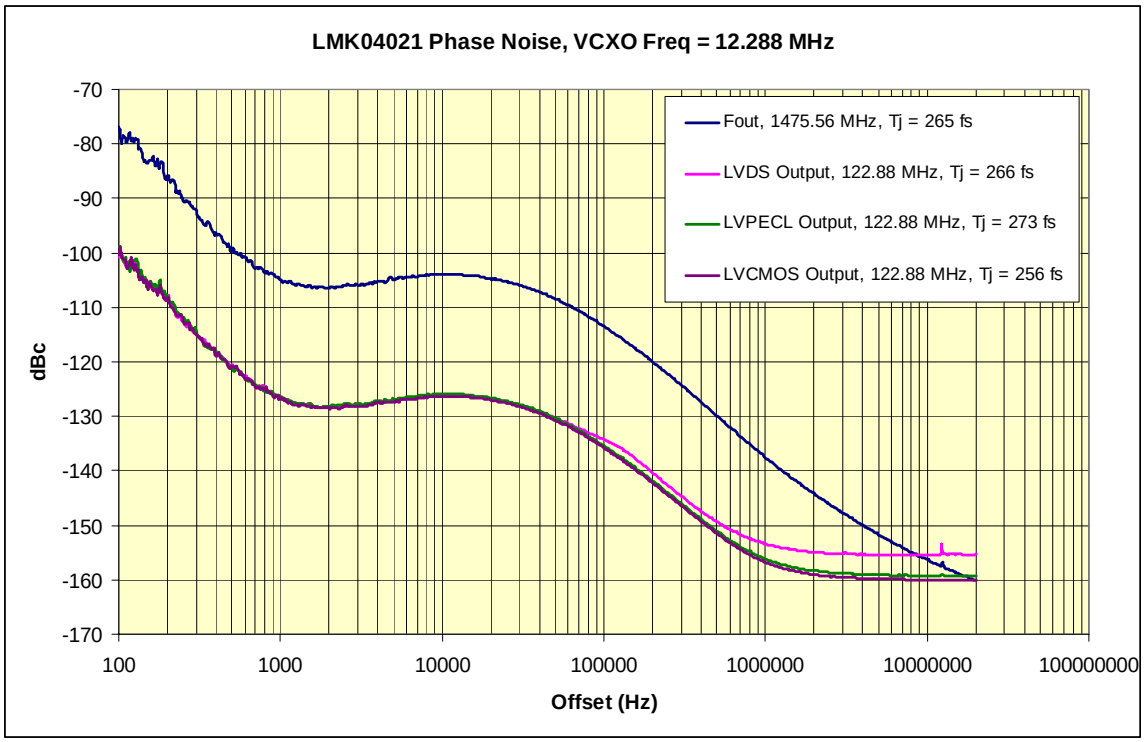


Figure 14. Typical Phase Noise Performance at F_{out}, Fvco = 1474.56 MHz, Fcomp2 = 12.288 MHz. XTAL Resonator option. Jitter metrics are for an integration bandwidth of 100 Hz to 20 MHz.

The phase noise and jitter performance at the clock outputs of the LMK040XX is strongly dependent on the phase noise characteristics of the VCXO or crystal driving the OSCin port.

The next sets of phase noise plots represent typical performance achieved using modular VCXO packages with PLL1. The first set of plots contains the VCXO phase noise plots for the 100 MHz VCXO and the 61.44 MHz VCXO.

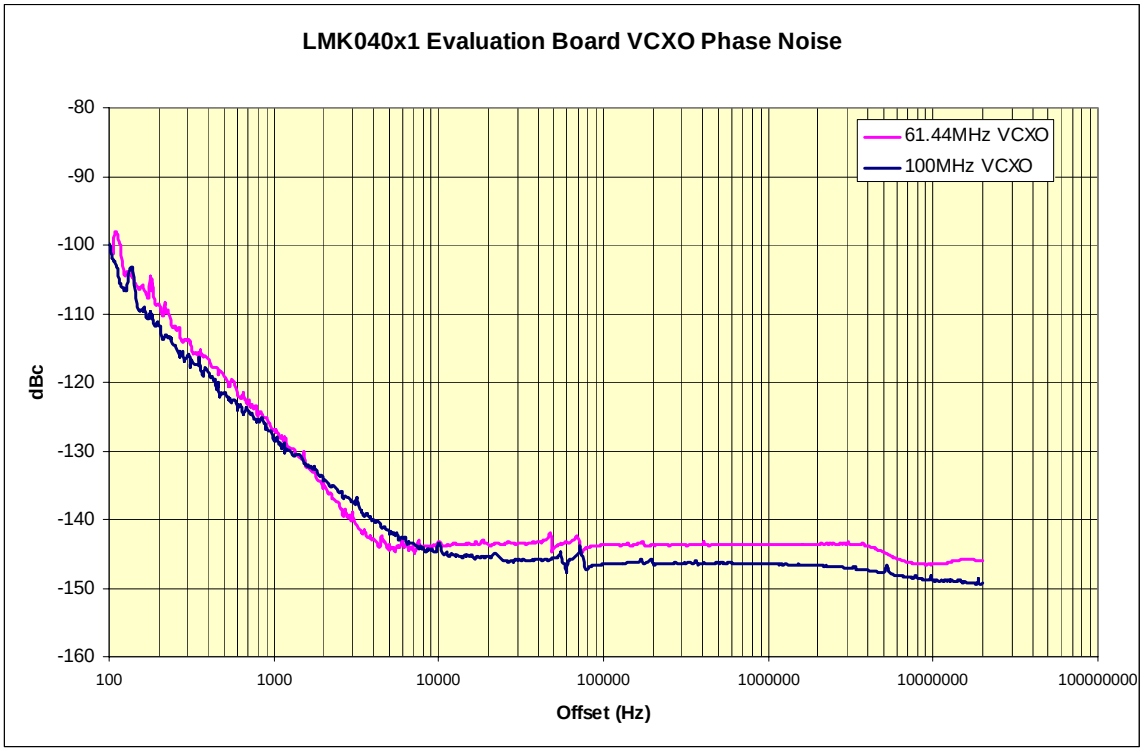


Figure 15. LMK040X1 Evaluation Board, typical VCXO Phase Noise, 100 MHz and 61.44 MHz VCXOs.

The following table lists the test conditions used for the phase noise measurements based upon the VCXO option, 100 MHz:

Table 8. LMK040XX test conditions, 100 MHz VCXO Option, LMK04021

Parameter	Value
PLL1 Reference clock input	CLKin0, single-ended, CLKin0* AC-coupled to GND
PLL1 Reference Clock frequency	100 MHz
PLL1 Phase detector frequency	1000 kHz
PLL1 Charge Pump Gain	100 uA
VCXO frequency	100 MHz, Crystek CVPD-920
PLL2 phase detector frequency	50 MHz
PLL2 REF2X mode	disabled
PLL2 Charge Pump Gain	3200 uA

The following plot illustrates the phase noise performance of the LMK040XX using the VCXO option. The VCXO represented in these plots is a Crystek CVPD-920-100MHz LVPECL model.

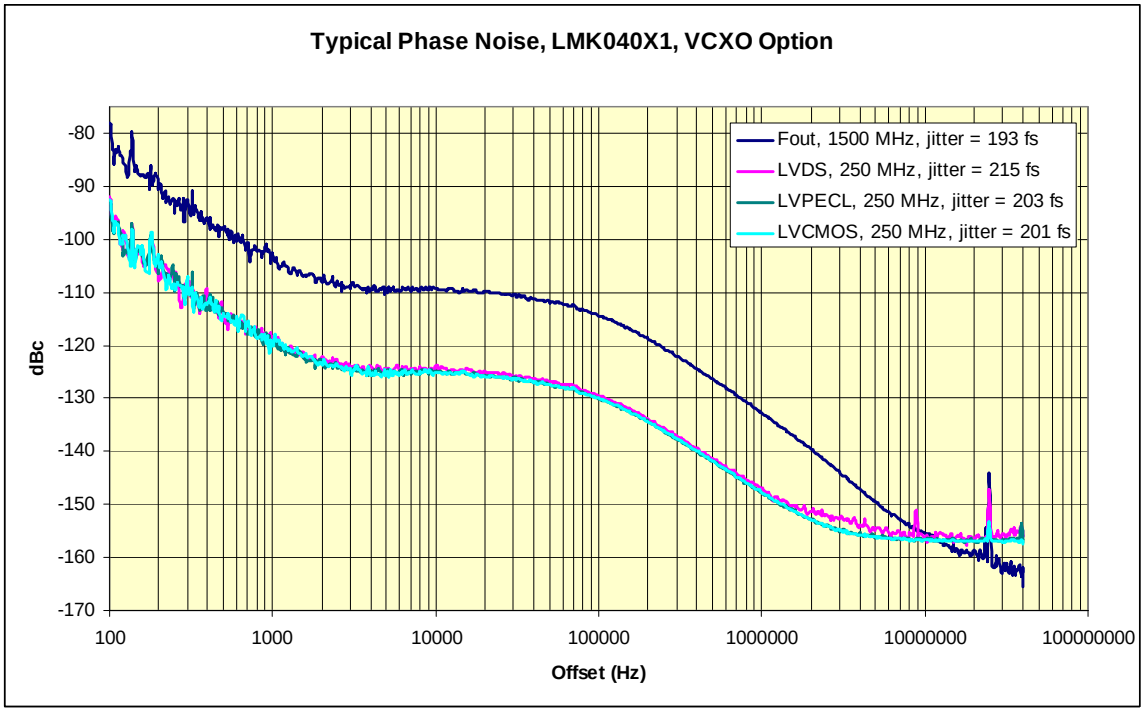


Figure 16. Typical Phase Noise, LMK040X1, VCXO Option (100 MHz). Jitter metrics are for an integration bandwidth of 100 Hz to 20 MHz.

The following plot illustrates the phase noise performance of the LMK040XX using the VCXO option. In this case, the VCXO is a Crystek CVPD-920-61.44 MHz LVPECL model.

Table 9. Test Conditions for Phase Noise Measurements, 61.44 VCXO option, LMK04020

Parameter	Value
PLL1 Reference clock input	CLKin0*, single-ended, CLKin0 AC-coupled to GND
PLL1 Reference Clock frequency	61.44 MHz
PLL1 Phase detector frequency	1024 MHz
PLL1 Charge Pump Gain	100 uA
VCXO frequency	61.44 MHz, Crystek CVPD-920
PLL2 phase detector frequency	61.44 MHz
PLL2 REF2X mode	disabled
PLL2 Charge Pump Gain	1600 uA

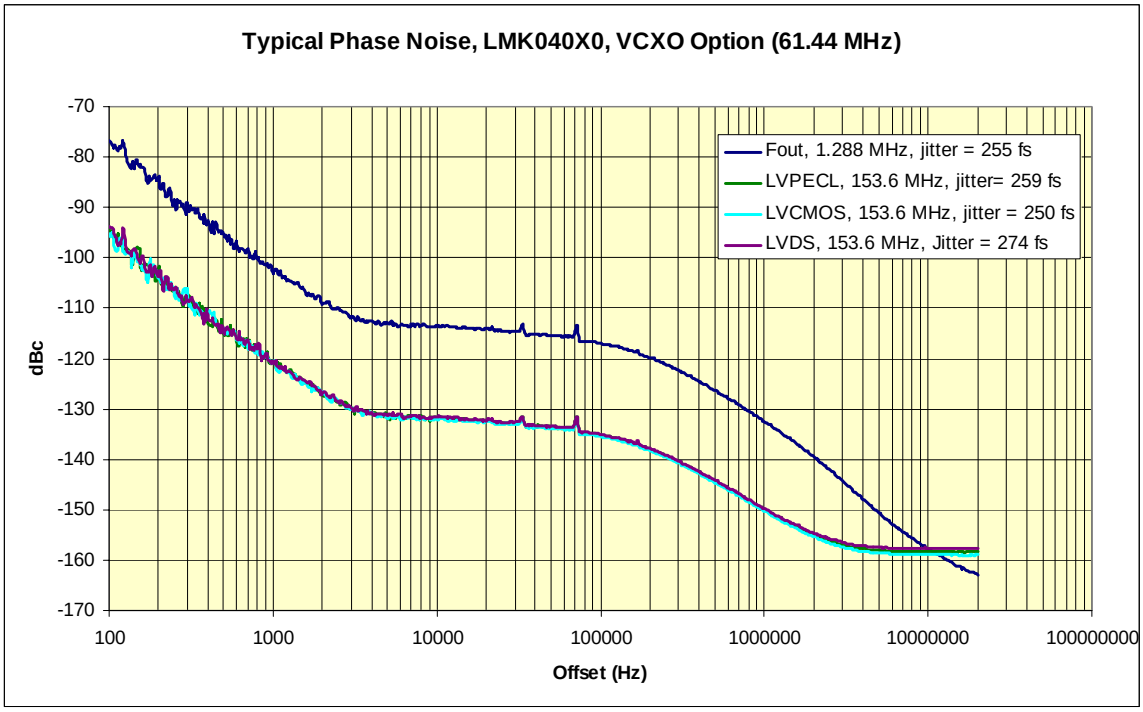
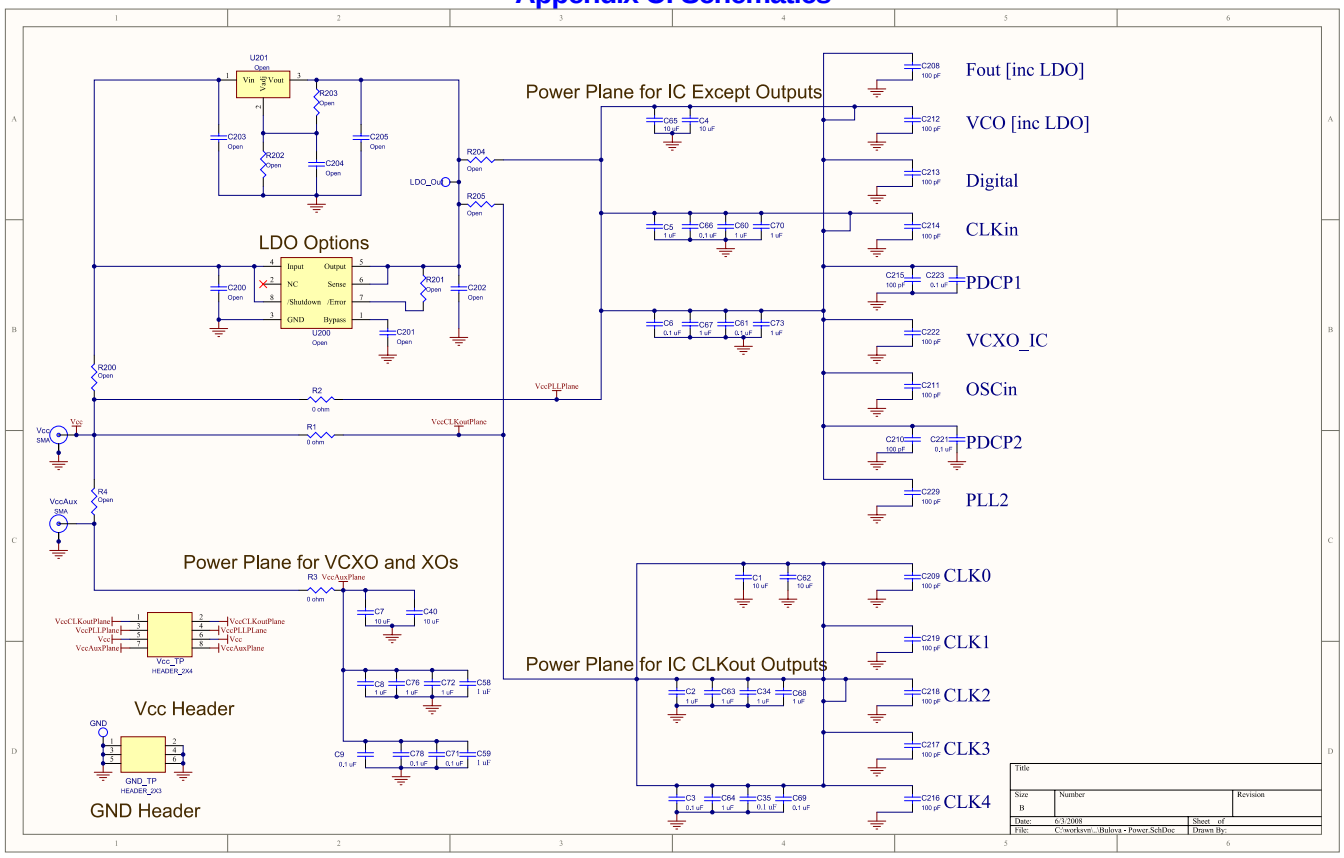
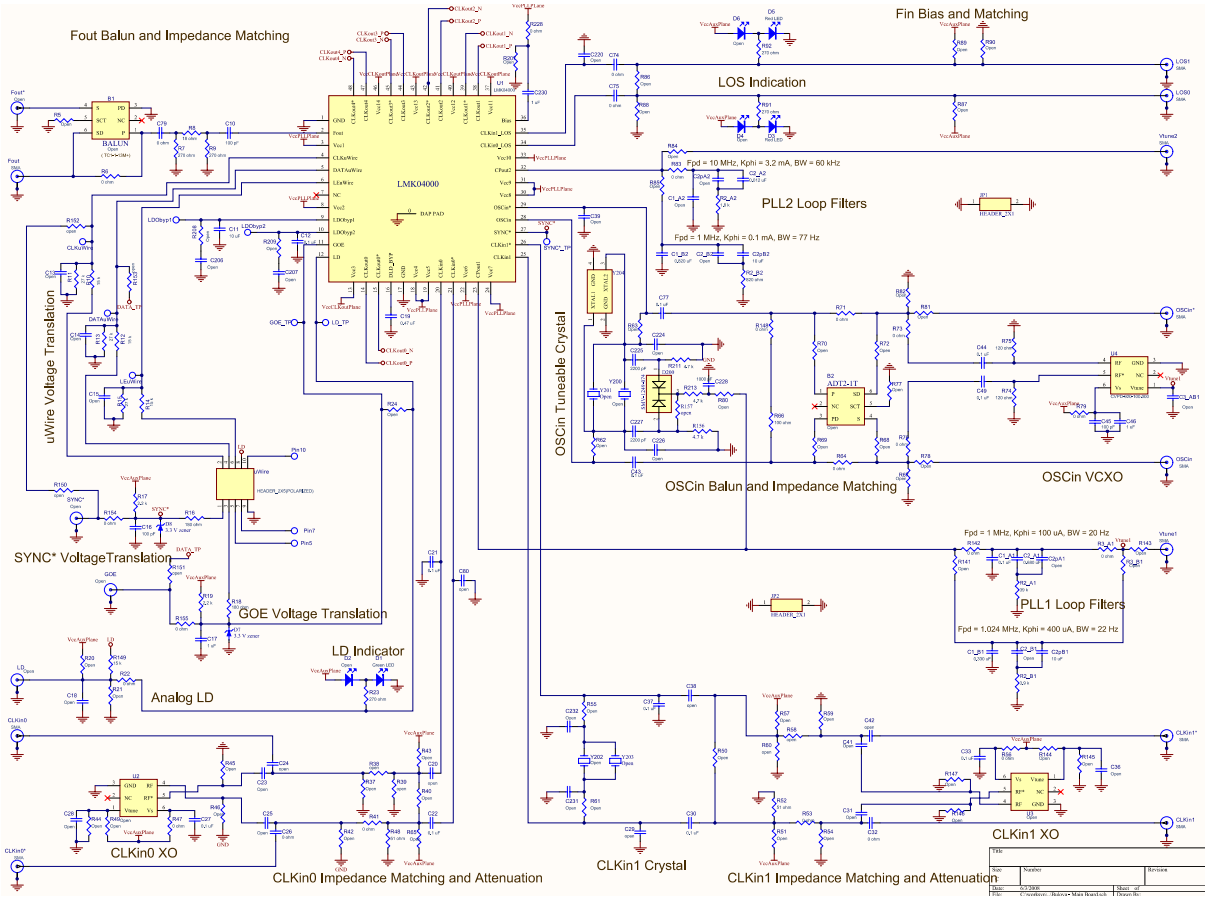


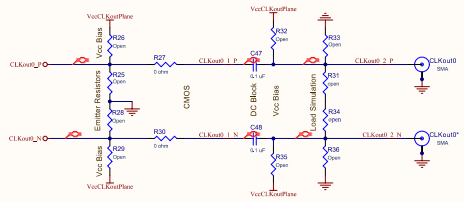
Figure 17. Typical Phase noise, LMK04020, VCXO Option (61.44 MHz). Jitter metrics are for an integration bandwidth of 100 Hz to 20 MHz.

Appendix C: Schematics

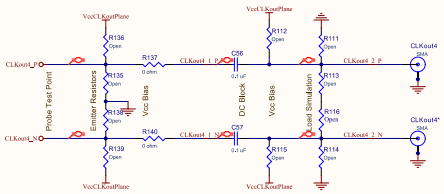




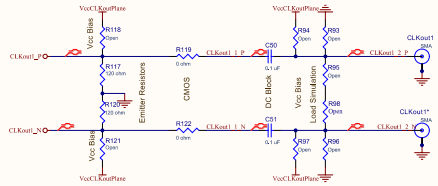
CLKout0 (LVPECL/2VPECL or LVDS)



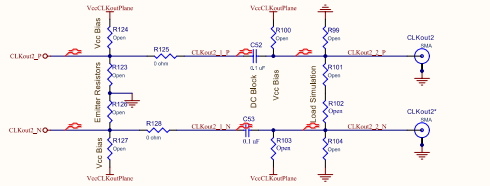
CLKout4 (LVPECL/2VPECL or LVDS)



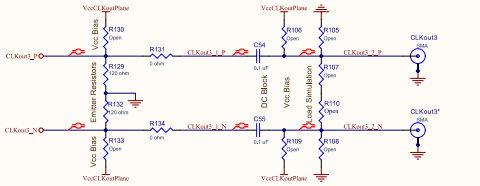
CLKout1 (LVPECL/2VPECL)



CLKout2 (LVPECL/2VPECL or LVCMOS)



CLKout3 (LVPECL/2VPECL or LVCMOS)



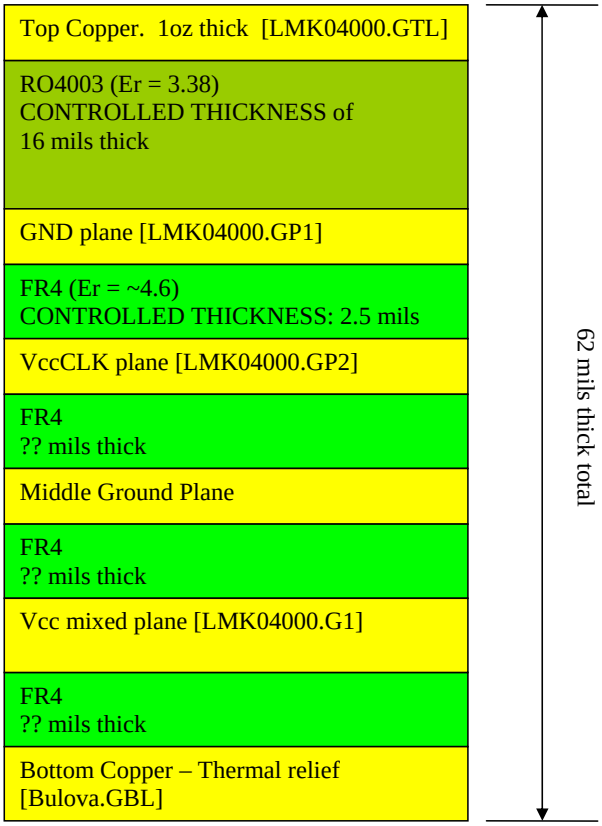
Appendix D: Board Layers Stackup

Layers of the 6 layer evaluation board include:
Blue is dielectrics

- Top layer for high priority high frequency signals
  - 1 oz CU
- RO4003 Dielectric, **16 mils**
- Ground plane
- FR4, **2.5 mils** thick.
- Power plane #1 – VccCLK
- FR4, xx mils
- middle ground plane
- FR4, xx mils
- VccPLL, VccAux
- FR4, xx mils
- Bottom layer copper clad for thermal relief

Top to bottom layer order:

LMK04000.GTL	(1)
LMK04000.GP1	(2) gnd
LMK04000.GP2	(3) vcc
LMK04000.GP3	(4) gnd
LMK04000.G1	(5) vcc
LMK04000.GBL	(6)



Appendix E: Bill of Materials

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
100 pF	Kemet	C0603C101J5GAC	4	C10, C16, C45, C79
100 pF	Kemet	C0603C101J5GAC	14	C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C222, C229
1 nF	Kemet	C0603C102J5GAC	1	C1_B1
1 nF	Kemet	C0603C102J5GAC	1	C228
2.2 nF	Kemet	C0603C222K5RAC	2	C225, C227
5.6 nF	Kemet	C1210C562J1GAC	1	C2pB1
12 nF	Kemet	ECH-U01123JX5	1	C2_A2
0.1 uF	Kemet	C0603C104J3RAC	10	C3, C6, C9, C12, C35, C61, C66, C69, C71, C78
0.1 uF	Kemet	C0603C104J3RAC	27	C19, C20, C21, C24, C26, C27, C30, C32, C33, C37, C42, C43, C44, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C77, C221, C223
100 nF	Kemet	C0603C104J3RAC	1	C1_A1
680 nF	Kemet	C0603C684K8PAC	1	C2_A1
820 nF	Kemet	C0603C824K8PAC	1	C1_B2
1 uF	Kemet	C0603C105K8VAC	17	C2, C5, C8, C17, C34, C46, C58, C59, C60, C63, C64, C67, C68, C70, C72, C73, C76
1 uF	Kemet	C0603C105K8VAC	1	C230
10 uF	Kemet	C0805C106K9PAC	6	C1, C2pB2, C4, C7, C62, C65
10 uF	Kemet	C0805C106K9PAC	1	C11
10 uF	Kemet	C0805C106K9PAC	1	C40
Resistors				
0 ohm	Vishay	CRCW0603000ZRT1	33	C74, C75, R27, R30, R38, R41, R47, R53, R56, R64, R71, R119, R122, R125, R128, R131, R134, R137, R140, R148, R214, R215, R216, R218, R219, R220, R221, R222, R224, R225, R226, R227, R228
0 ohm	Vishay	CRCW0603000ZRT1	13	R1, R2, R3, R3_A1, R22, R73, R76, R79, R83, R142,

				R212, R217, R223
0 ohm	Yageo	RC0805JR-070RL	1	R6
18 ohm	Vishay	CRCW0603180JRT1	1	R8
51 ohm	Vishay/Dale	CRCW060351R0JNEA	2	R39, R52
100 ohm	Vishay	CRCW0603101JRT1	1	R66
120 ohm	Vishay/Dale	CRCW0603120RJNEA	4	R74, R75, R117, R120
180 ohm	Vishay	CRCW0603181JRT1	2	R16, R18
270 ohm	Vishay	CRCW0603271JRT1	2	R7, R9
820 ohm	Vishay	CRCW0603821JRT1	1	R2_B2
1.8 k	Vishay/Dale	CRCW06031K80JNEA	1	R2_A2
2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R17, R19
15 k	Vishay	CRCW0603153JRT1	4	R10, R12, R14, R149
27 k	Vishay	CRCW0603273JRT1	3	R11, R13, R15
39 k	Vishay/Dale	CRCW060339K0JNEA	1	R2_A1
47 k	Vishay/Dale	CRCW060347K0JNEA	2	R211, R213
390 k	Vishay/Dale	CRCW0603390KJNEA	1	R2_B1
Other				
SMV1249	Skyworks	SMV1249-074LF	1	D200
3.3 V zener	Comchip	CZRU52C3V3	2	D7, D8
SMA_FRAME	Printed Circuits Corp.	PCB	1	F1
HEADER_2X3	Comm Con Connectors	HTSM3203-6G2	1	GND_TP
HEADER_2X4	Comm Con Connectors	HTSM3203-8G2	1	Vcc_TP
HEADER_2X5 (POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
Green LED	Lumex	SML-LX2832GC-TR	1	D1
Red LED	Lumex	SML-LX2832IC-TR	2	D3, D5
SMA	Johnson Components	142-0701-851	23	CLKin0, CLKin0*, CLKin1, CLKin1*, CLKout0, CLKout0*, CLKout1, CLKout1*, CLKout2, CLKout2*, CLKout3, CLKout3*, CLKout4, CLKout4*, Fout, LOS0, LOS1, OSCin, OSCin*, Vcc, VccAux, Vtune1, Vtune2
CVPD-920-100.000	Crystek	CVPD-920-100.000	1	U4
0.875" Standoffs	SPC Technology	SPCS-14	4	Standoffs in the four corners (insert from bottom)

Open				
Open	-	603	45	C1_A2, C2_B1, C2_B2, C2pA2, C3_AB1, C13, C14, C15, C18, C28, C36, C201, C204, C220, C224, C226, C231, C232, R3_B1, R4, R5, R20, R21, R23, R24, R44, R49, R78, R80, R81, R84, R85, R141, R143, R144, R145, R200, R201, R202, R203, R204, R205, R206, R208, R210
Open	-	Open	93	C22, C23, C25, C29, C31, C38, C39, C41, R25, R26, R28, R29, R31, R32, R33, R34, R35, R36, R37, R40, R42, R43, R45, R46, R48, R50, R51, R54, R55, R57, R58, R59, R60, R61, R62, R63, R65, R67, R68, R69, R70, R72, R77, R82, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R118, R121, R123, R124, R126, R127, R129, R130, R132, R133, R135, R136, R138, R139, R146, R147, R207, R209
Open	-	805	3	C203, C206, C207
Open	-	Open	4	C2pA1, C200, C202, C205
Open	-	Open	1	B2
Open	-	Open	1	B1
Open	-	Open	2	Y200, Y202
Open	-	Open	3	D2, D4, D6
Open	-	Open	1	U200
Open	-	Open	2	Y201, Y203
Open	-	Open	5	Fout*, GOE, LD, SYNC*, VinLDOByp
Open	-	Open	1	U201
Open	-	Open	2	U1, U2, U3

Appendix F

Typical BALUN Board Frequency Response

The following figure illustrates the typical frequency response of BALUN using either of the Mini-Circuits models listed.

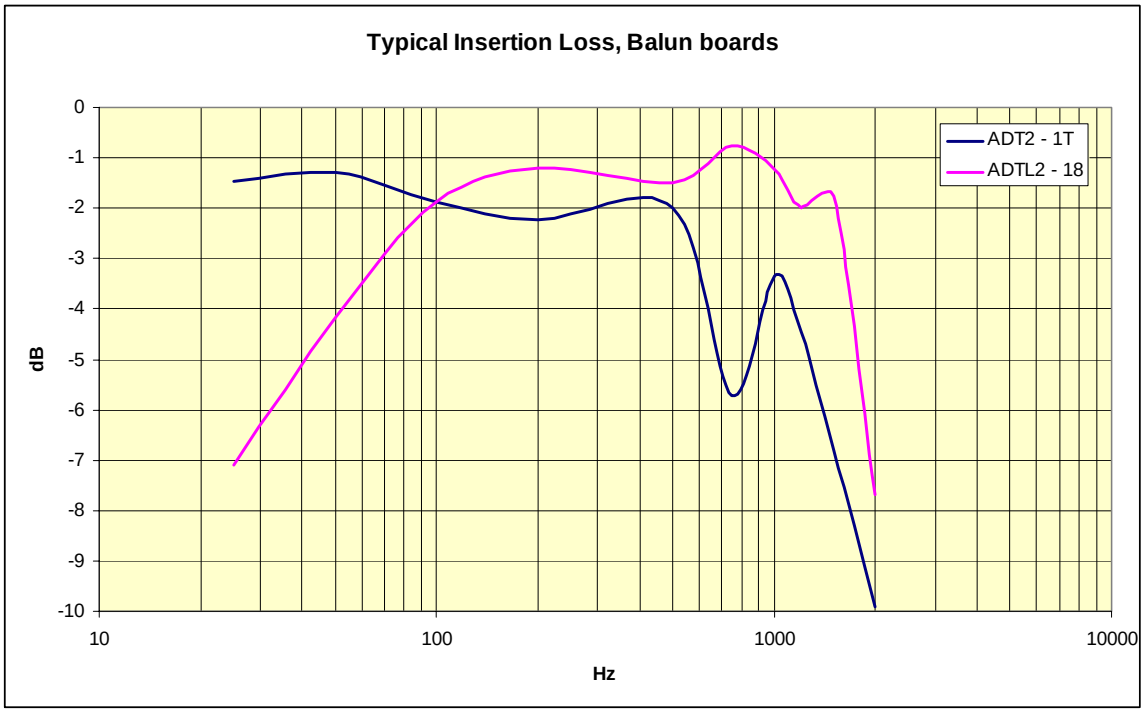


Figure 18. Typical BALUN Frequency Response

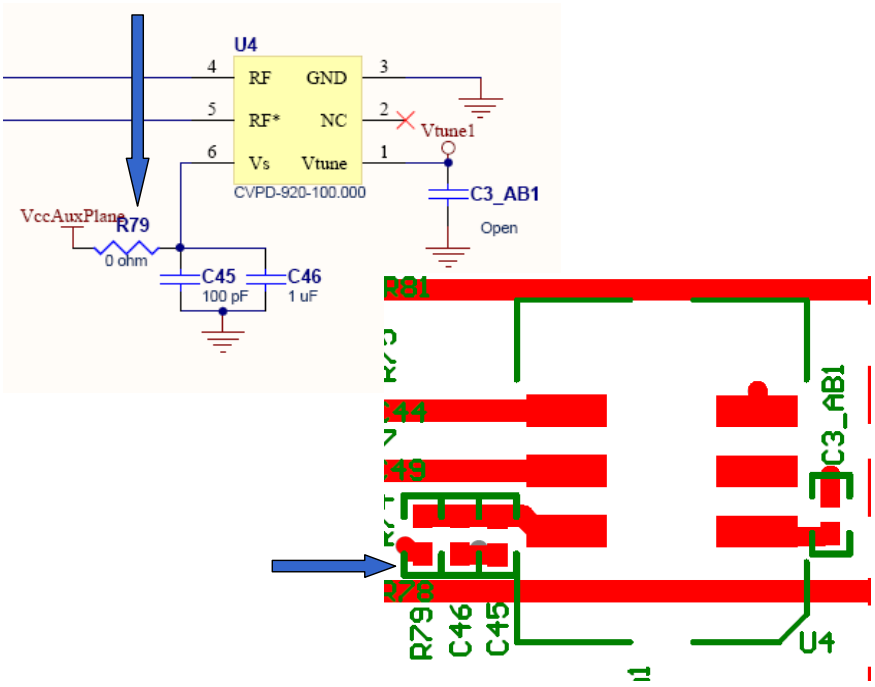
Appendix G

This appendix contains instructions for changing the active on-board oscillator for PLL1.

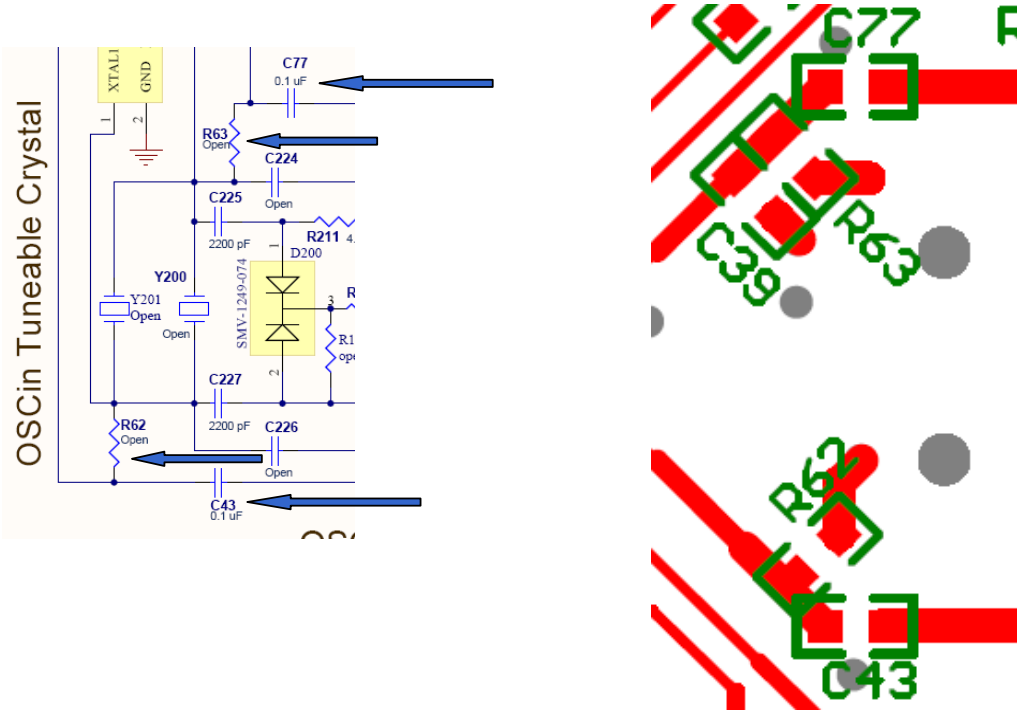
Changing from Crystal Resonator to VCXO

If the board has been setup to use the crystal-based oscillator with PLL1, the crystal may be disabled and the VCXO enabled as described on the following pages:

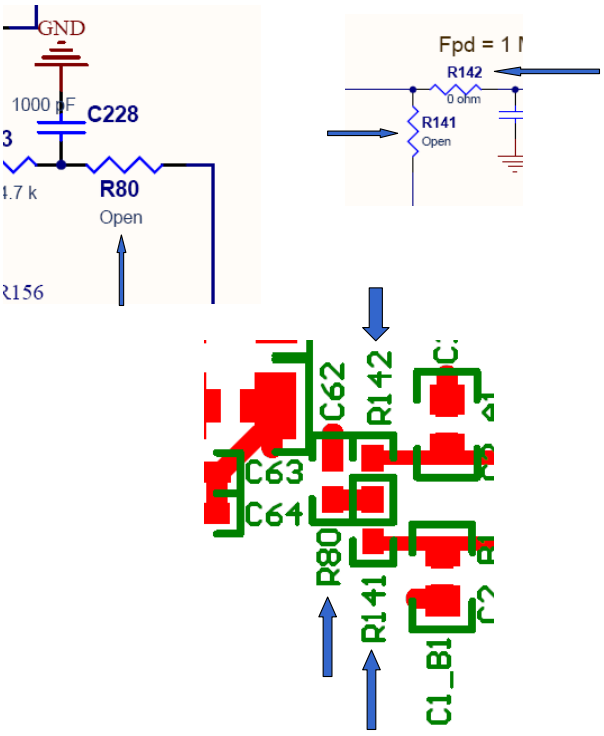
1. Install a zero Ohm resistor in R79 (near the VCXO)



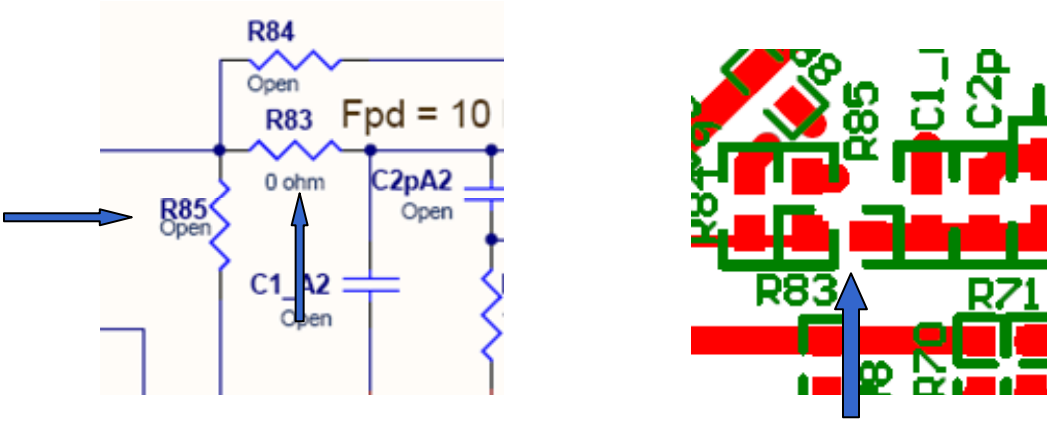
2. Remove resistors R62 and R63 and install 0.1 uF capacitors in C43 and C77.



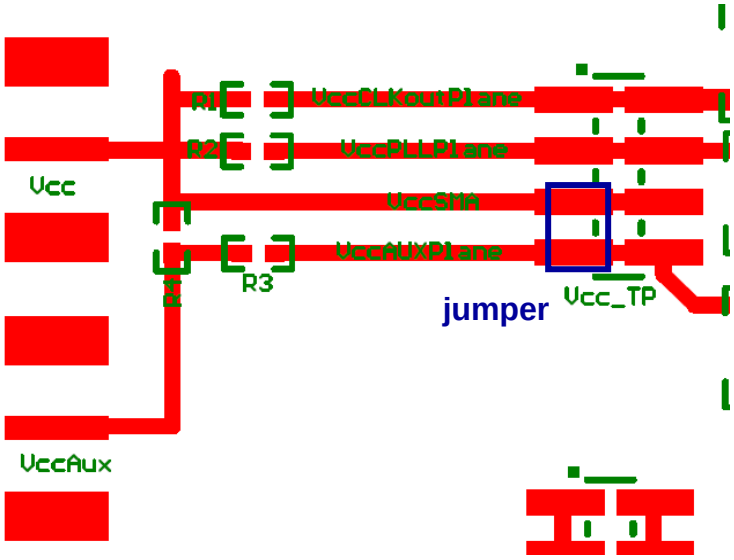
3. Remove resistors R141 and R80. Install a zero Ohm resistor in R142



4. Install a 0 Ohm resistor in R83 and remove the 0 Ohm resistor in R85



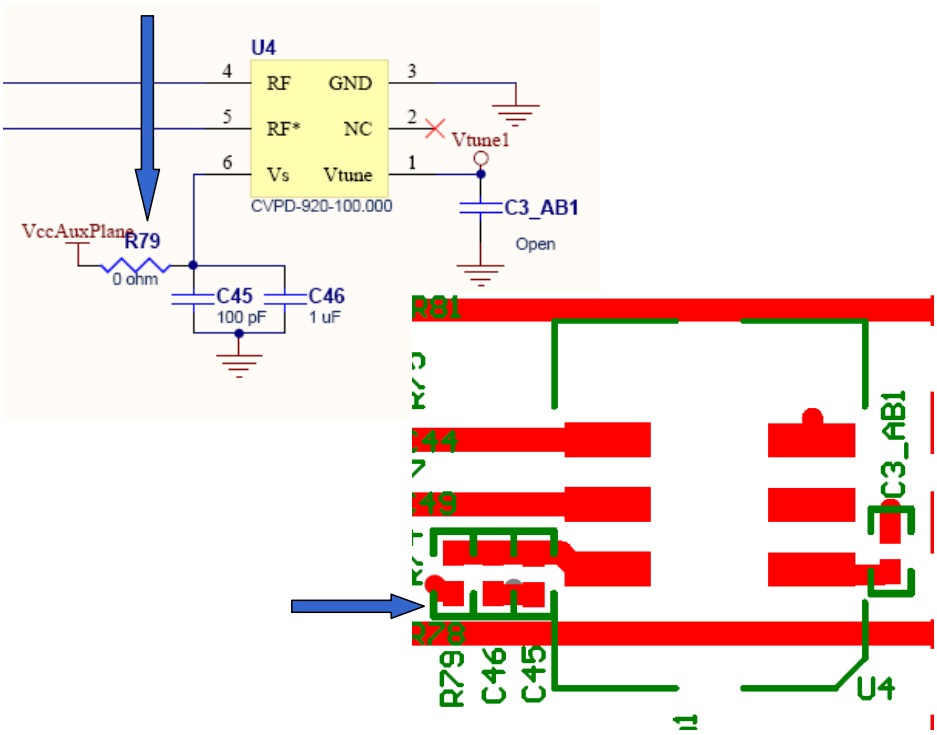
5. Power to the VCXO is provided by placing a jumper on the Vcc_TP header across the traces labeled “VccSMA” and “VccAUXPlane”.



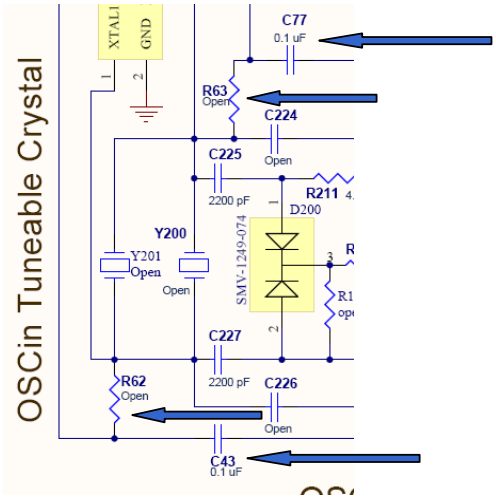
Changing from VCXO to Crystal Resonator

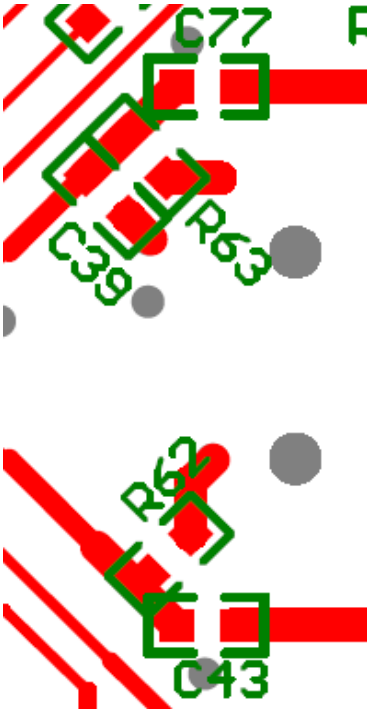
If the board has been setup to use the VCXO for PLL1, the VCXO may be disabled and the crystal enabled as described on the following pages:

1. Remove the zero Ohm resistor R79 (near the VCXO)

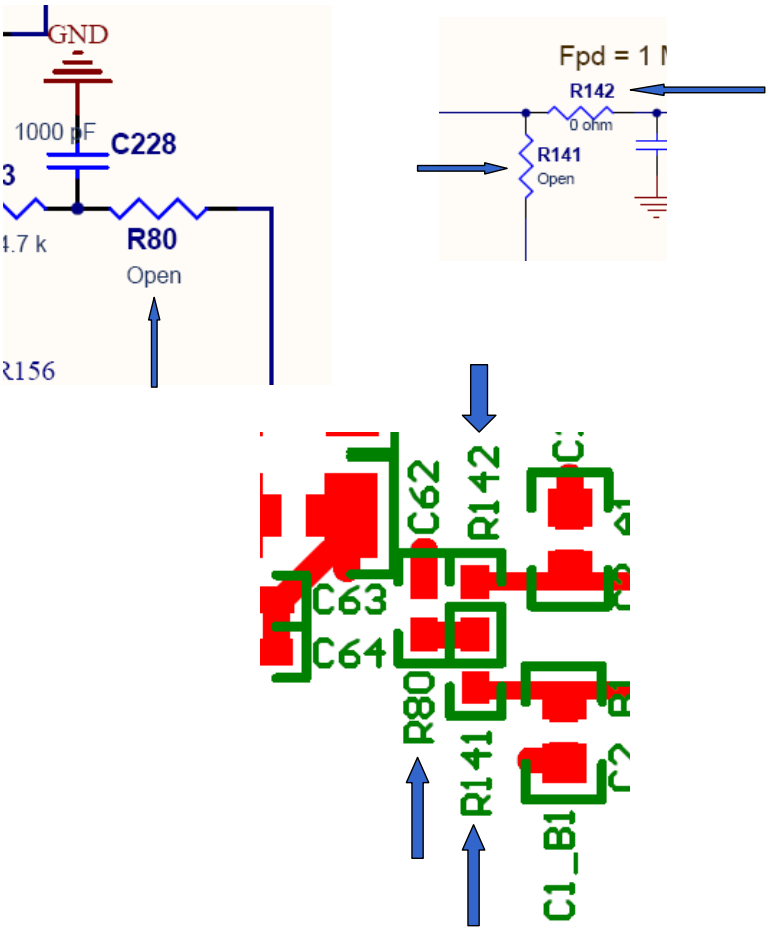


2. Install 0 Ohm resistors R62 and R63 and remove the 0.1 uF capacitors in C43 and C77.

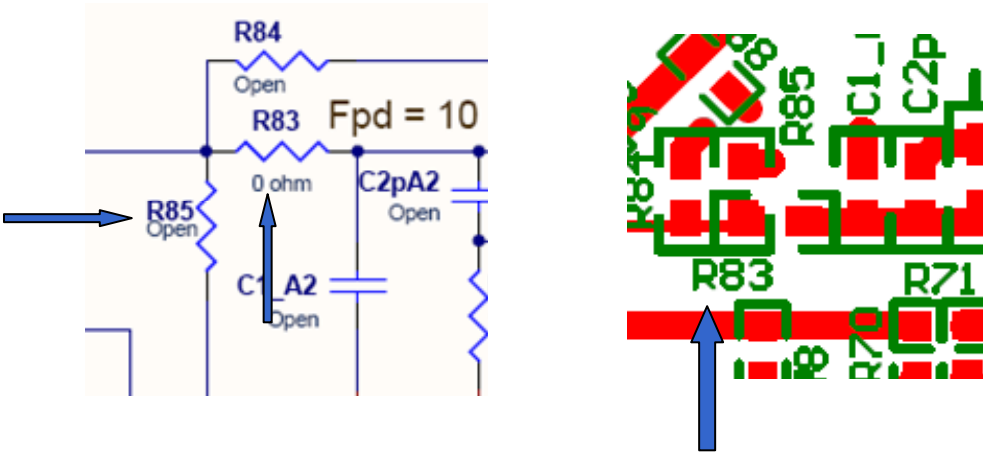




3. Install a 0 Ohm resistor at R141 and R80. Remove the zero Ohm resistor in R142



4. Remove the 0 Ohm resistor installed in R83 and install a 0 Ohm resistor in R85.



5. Disconnect power to the VCXO by removing the jumper on the Vcc_TP header across the traces labeled “VccSMA” and “VccAUXPlane”, if installed.