

# CY3275

Cypress Low Voltage Programmable Powerline Communication Development Kit Guide

Doc. # 001-53657 Rev. \*B

Cypress Semiconductor 198 Champion Court San Jose, CA 95134-1709 Phone (USA): 800.858.1810 Phone (Intnl): 408.943.2600 http://www.cypress.com



#### Copyrights

© Cypress Semiconductor Corporation, 2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATE-RIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

PSoC® is a registered trademark of Cypress Semiconductor Corporation. All products and company names mentioned in this document may be the trademarks of their respective holders.

Purchase of I2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I2C Patent Rights to use these components in an I2C system, provided that the system conforms to the I2C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors.

#### Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Data Sheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

# Contents



1.1     Using the PLC Kit	1. Introdu	uction	n	5
1.2     The Cypress PLC Solution		1.1	Using the PLC Kit	5
1.3     Kit Contents     7       1.4     Document Revision History     8       1.5     Documentation Conventions     8       2. PLC LV Development Board     9       2.1     Features.     9       2.2     PLC Development Board Functional Overview     9       2.2     PLC Development Board Functional Overview     9       2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     A.1.1 Board Overview     19       A.1.1 Board Overview     19     A.1.2 User Interface     20       A.1.4 Power Supply     22     A.2 Layout     23			0	
1.4     Document Revision History     8       1.5     Documentation Conventions     8       2. PLC LV Development Board     9       2.1     Features.     9       2.2     PLC Development Board Functional Overview     9       2.2.1     Operating Conditions:     9       2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit and Receive Coupling Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     A.1.1 Board Overview     19       A.1.2     User Interface     20     20       A.1.3     Transmit and Receive Filter Coupling     21       A.1.4     Power Supply     22       A.2     Layout     23				
1.5     Documentation Conventions     8       2. PLC LV Development Board     9       2.1     Features     9       2.2     PLC Development Board Functional Overview     9       2.1     Operating Conditions:     9       2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     A.1.1 Board Overview     19       A.1.1 Board Overview     19     A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21     A.1.4 Power Supply     22       A.2 Layout     23     23     23     23		-		
2. PLC LV Development Board     9       2.1 Features			•	
2.1     Features.     .9       2.2     PLC Development Board Functional Overview     .9       2.1     Operating Conditions:     .9       2.3     Hardware Description     .10       2.3.1     Power Supply Circuit.     .11       2.3.2     Transmit Amplifier Circuit     .11       2.3.3     Transmit and Receive Coupling Circuit     .11       2.3.4     Development Section     .12       2.3.4.1     Bread Board     .12       2.3.4.2     Development Section     .12       2.3.4.3     Potentiometer and DIP Switches     .15       2.3.5     LCD Daughter Card     .16       2.3.6     Debugger     .16       2.3.7     RS232-COM Port     .17       Appendix     .19     A.1 Schematics     .19       A.1.1 Board Overview     .19     A.1.2 User Interface     .20       A.1.3     Transmit and Receive Filter Coupling     .21     .21       A.14     Power Supply     .22     .22     .22		-		-
2.2PLC Development Board Functional Overview92.2.1Operating Conditions:92.3Hardware Description102.3.1Power Supply Circuit112.3.2Transmit Amplifier Circuit112.3.3Transmit and Receive Coupling Circuit112.3.4Development Section122.3.4.1Bread Board122.3.4.2Development Section122.3.4.3Potentiometer and DIP Switches152.3.5LCD Daughter Card162.3.7RS232-COM Port17Appendix19A.1 Schematics19A.1 Schematics19A.1.2 User Interface20A.1.4Power Supply22A.2 Layout23	2. PLC LV	/ Deve	elopment Board	9
2.2.1     Operating Conditions:     9       2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23		2.1	Features	9
2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23		2.2	PLC Development Board Functional Overview	9
2.3     Hardware Description     10       2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.2.1 Operating Conditions:	9
2.3.1     Power Supply Circuit     11       2.3.2     Transmit Amplifier Circuit     11       2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     A.1 Schematics     19       A.1.1 Board Overview     19     19     A.1.2 User Interface     20       A.1.3     Transmit and Receive Filter Coupling     21     21       A.1.4     Power Supply     22     22       A.2     Layout     23		2.3		
2.3.3     Transmit and Receive Coupling Circuit     11       2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23				
2.3.4     Development Section     12       2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.2 Transmit Amplifier Circuit	11
2.3.4.1     Bread Board     12       2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.3 Transmit and Receive Coupling Circuit	11
2.3.4.2     Development Section     12       2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.4 Development Section	12
2.3.4.3     Potentiometer and DIP Switches     15       2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.4.1 Bread Board	12
2.3.5     LCD Daughter Card     16       2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.4.2 Development Section	12
2.3.6     Debugger     16       2.3.7     RS232-COM Port     17       Appendix     19     19       A.1 Schematics     19       A.1.1 Board Overview     19       A.1.2 User Interface     20       A.1.3 Transmit and Receive Filter Coupling     21       A.1.4 Power Supply     22       A.2 Layout     23			2.3.4.3 Potentiometer and DIP Switches	15
2.3.7 RS232-COM Port.17Appendix19A.1 Schematics19A.1.1 Board Overview19A.1.2 User Interface20A.1.3 Transmit and Receive Filter Coupling21A.1.4 Power Supply22A.2 Layout23			2.3.5 LCD Daughter Card	16
Appendix19A.1 Schematics19A.1.1 Board Overview19A.1.2 User Interface20A.1.3 Transmit and Receive Filter Coupling21A.1.4 Power Supply22A.2 Layout23			2.3.6 Debugger	16
A.1 Schematics			2.3.7 RS232-COM Port	17
A.1.1 Board Overview19A.1.2 User Interface20A.1.3 Transmit and Receive Filter Coupling21A.1.4 Power Supply22A.2 Layout23	Appendix		•	19
A.1.2 User Interface		A.1 Sc	chematics	19
A.1.3 Transmit and Receive Filter Coupling			A.1.1 Board Overview	19
A.1.3 Transmit and Receive Filter Coupling			A.1.2 User Interface	20
A.1.4 Power Supply				
A.2 Layout				
$\pi_{1}$			A.2.1 Top Layer	
A.2.2 Ground Layer				
A.2.3 Power Laver				
A.2.4 Bottom Layer				
A.2.5 Top Silkscreen				
A.2.6 Bottom Silkscreen				
A.3 Bill of Materials		A.3 Bi	ill of Materials	29

Contents







## 1.1 Using the PLC Kit

1.

Introduction

Cypress's Powerline Communication Solution (PLC) makes it possible to transmit command and control data over high voltage and low voltage powerlines. This solution is developed for low bandwidth powerline communication.

The PLC CY3275 Low Voltage (LV) development board allows system design using the ability of the Cypress PLC family of devices to transmit data up to 2400 bps over low voltage (12V to 24V AC/DC) powerlines.

- Chapter 1 provides a brief overview of the Cypress PLC solution. It describes the contents of the development kit and lists special features of the PLC Demonstration kit.
- Chapter 2 gives the functional overview of the PLC Board and describes the operating procedure of the PLC LV board. It provides a high level hardware description of the board.

## 1.2 The Cypress PLC Solution

Powerlines are available everywhere in the world. This makes them one of the most widely available communication mediums for PLC technology. The pervasiveness of powerlines also makes it difficult to predict their characteristics and noise. Because of the variability of powerline quality, implementing robust communication over powerline has been an engineering challenge for years. With this in mind, the Cypress PLC solution is designed to enable secure, reliable, and robust communication over powerlines. The key features of the Cypress PLC solution are:

- An integrated powerline PHY modem with optimized amplifiers that work with rugged high and low voltage powerlines
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement based signaling and multiple retries
- Support for 8-bit packet CRC and 4-bit header CRC for error detection and data packet retransmission
- Carrier Sense Multiple Access (CSMA) scheme that minimizes collisions between packet transmissions on the powerline

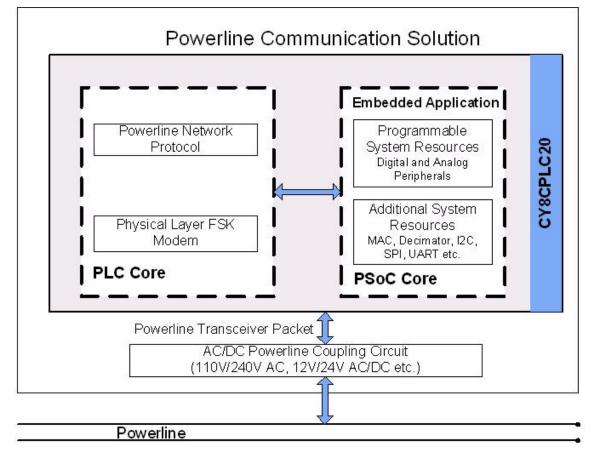
5



The Cypress PLC solution consists of three key elements as shown in Figure 1-1.

- Powerline network protocol layer
- Physical layer FSK modem
- Power Amplification And Coupling Circuits

Figure 1-1. Cypress PLC Solution Block Diagram



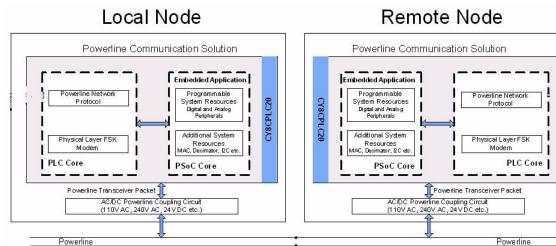
The powerline network protocol layer and the physical layer FSK modem are implemented on the CY8CPLC20 chip. The chip also contains a PSoC core in addition to the PLC core. The power amplification and coupling circuits are built using discrete components.

The network protocol layer allows for the addressing of multiple nodes on the network. This enables point-to-multipoint communication. The protocol layer also provides a defined packet structure for transmitting data packets from one node to the other as well as error detection and packet retransmit functionalities.

A two node system level diagram is shown in Figure 1-2.

6





#### Figure 1-2. PLC System Level Block Diagram - Two Nodes

## 1.3 Kit Contents

The CY3275 PLC LV Development kit contains:

- CY3275 PLC LV development board
- CY3275 Quick start guide
- CD-ROM containing:
  - Packet Test software PLC Control Panel application
  - CY8CPLC20 data sheet
  - □ User guide
  - □ CY3275 Board Altium design project
  - □ CY3275 Board BOM
  - □ Application note Using CY8CPLC20 in Powerline Communication (PLC) Applications
  - CY3275 Board schematics
  - □ CY3275 Board Gerbers
  - PSoC Designer
  - PSoC Programmer
- 12V DC power supply
- MiniProg1 for programming the CY8CPLC20 device
- 25 Jumper wires
- LCD module
- USB-I<sup>2</sup>C Bridge
- Retractable USB cable
- Daisy chain cable



## 1.4 Document Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	8/14/09	IUS	Initial release.
*A	9/3/09	IUS	Rework for external release.
*В	12/10/09	RARP	Content updates

## 1.5 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\cd\icc\
Italics	Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Designer User Guide</i> .
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the <b>File</b> icon and then click <b>Open</b> .
Times New Roman	Displays an equation: 2+2=4
Text in gray boxes	Describes Cautions or unique functionality of the product.

# 2. PLC LV Development Board



This chapter explains the key features of the CY3275 development board.

## 2.1 Features

The Cypress CY3275 LV CY8CPLC20 development board is a versatile tool with these features

- User friendly PLC Control Panel application available on the kit CD-ROM
- Chip power supply derived from 12V to 24V AC/DC
- CY8CPLC20-OCD chip -- 100-pin TQFP on chip debug (OCD) device that allows for the quick design and debug of PLC applications. The CY8CPLC20 100-pin TQFP is available for debug purposes only. For production quantities, CY8CPLC20 is available in 28-pin SSOP and 48-pin QFN packages.
- User configurable general purpose LEDs
- General purpose 8-bit DIP switch
- RJ45 connector to use ICE debugger
- RS232 COM port for serial communication
- Header to attach LCD card
- I<sup>2</sup>C header for communicating to external devices
- ISSP header for programming the CY8CPLC20 chip

## 2.2 PLC Development Board Functional Overview

The PLC development board is designed as a development platform for low bandwidth (up to 2400 bps) powerline communication applications.

The application residing on CY8CPLC20 generates the data. The PLC core encapsulates this data into a PLC network packet. The FSK modem modulates this packet and the coupling circuitry incorporates the resulting sinusoidal waveform onto the existing waveform on the low voltage bus.

#### 2.2.1 Operating Conditions:

- Input Voltage: 12/24V AC/DC
- Input Current: 200 mA/150 mA
- Operating Temperature: 0°C to 40°C
- Operating Humidity Condition: 5% to 95% RH, non-condensing

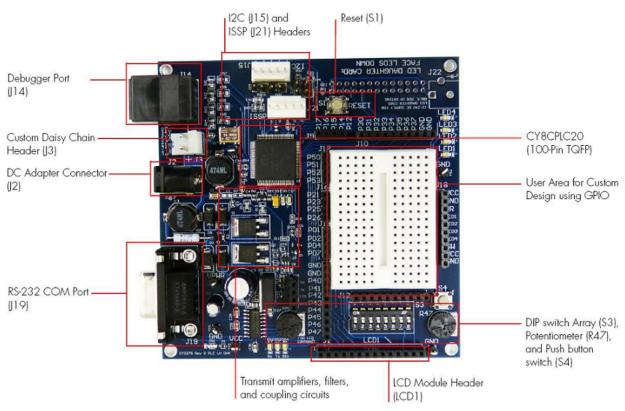


## 2.3 Hardware Description

The programmable low voltage PLC development board is shown in Figure 2-1. The board can be divided into six main sections:

- Power supply circuit to generate 5V
- Transmit amplifier and coupling circuit section
- Development section for user
- LCD module header
- Debugger
- RS232 COM port

#### Figure 2-1. Top View of Cypress Programmable PLC LV Development Board



The communication signal flow on this LV Board is:

*Transmit*: CY8CPLC20 TX pin  $\rightarrow$  Power Amplifier Circuitry  $\rightarrow$  LV Coupling Circuitry  $\rightarrow$  LV Powerline (12V to 24V AC/DC).

*Receive*: LV Powerline (12V to 24V AC/DC)  $\rightarrow$  LV Coupling Circuitry  $\rightarrow$  Passive Low Pass Filtering  $\rightarrow$  Centre Biasing  $\rightarrow$  CY8CPLC20 RX pin. The core of the PLC LV board is the CY8CPLC20 chip.



## 2.3.1 Power Supply Circuit

This section takes the power from the powerline and generates the necessary low DC voltage for the operation of the PLC transceiver and other components on the chip.

Table 2-1. Key Power Supply Circuitry Components

Component	Description	
J2	This is the connector to hook up the wall wart	
U2	5V regulator	
J3	This is a 2 pin header to connect other boards in daisy chain and power them. The cable to do this is provided with the kit. Connect a maximum of five boards in one daisy chain.	
DS1	This is a blue LED which is on when power is supplied to the board	

#### 2.3.2 Transmit Amplifier Circuit

This section takes the output signal from the CY8CPLC20 chip and amplifies the signal for transmission over the powerline.

Table 2-2. Key Transmit Amplifier Components

Component	Description
U3, Q1, Q2	These opamp and high gain transistors are used for power amplification.
Q3	This transistor controls whether transmission is allowed based on the out- put of the TXDISABLE pin

#### 2.3.3 Transmit and Receive Coupling Circuit

This circuit couples the signal from the board on to the powerline. On the receive side, the same circuit couples the carrier on the powerline in to the board rejecting the low frequency content on the powerline.

Table 2-3. Key Transmit and Receive Coupling Components
---

Component	Description
L3	This inductor along with R2 filters out the higher frequencies
L2	This is the inductor which grounds the low frequency signal and forms a high pass with C1 and L1
C6	This is the coupling capacitor that couples the communication signal and rejects the low frequency noise. The voltage rating of this component is an important parameter.

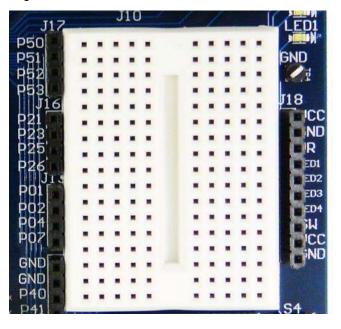


#### 2.3.4 Development Section

#### 2.3.4.1 Bread Board

This section is the area where you prepare your custom design. All GPIO pins excluding those required for PLC communication are routed to this bread board space for access.

Figure 2-2. Bread Board

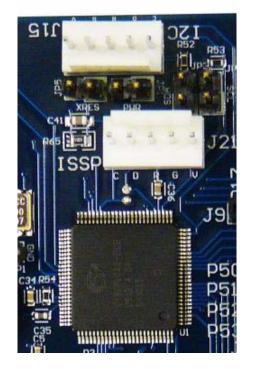


#### 2.3.4.2 Development Section

This section has the CY8CPLC20-OCD chip which has the integrated transmit/receive modem and network protocol. It also has the I2C header to communicate to the external host processor. The ISSP header is provided to program the part. The part also has inbuilt debug support using the RJ45 connector which can be used with the ICE debugger. There are also three dedicated LEDs, which can be used to indicate communication on the powerline: green LED for TX, red LED for RX, and yellow LED for BIU.



## Figure 2-3. I<sup>2</sup>C and ISSP headers





Headers and Jumpers	Description
CY8CPLC20-OCD	This is the Cypress Powerline transceiver chip. It is a 100-pin OCD device.
PWR LED[DS1]	This is a blue LED that glows when the board is powered on.
TX LED[DS3]	This is a green LED that can be used to indicate when the board is transmit- ting data on to the powerline.
RX LED[DS2]	This is a red LED that can be used to indicate when the board is receiving data.
BIU LED[DS4]	This is a yellow LED that can be used to indicate when the transmit fre- quency band is in use.
TP1, TP2, TP3, TP4	Grounded test points to facilitate probing/debugging
S2	Reset switch for resetting the CY8CPLC20-OCD chip
J8	2-pin header for connecting to Vcc and Gnd
LED1-LED4	Headers connected to general purpose configurable LEDs
JP1 (PWR)	Connect this jumper to power an external board from the CY3275. The external board is powered through the V and G pins on the I2C connector (J15).
JP5 (Reset)	The jumper is for enabling the reset of the PLC chip through an external board. Once this jumper has been connected, the external board reset can be connected to the R pin on the I2C header (J15).
JP4 (I2C-SDA)	This is a pull up jumper. While communicating through I2C(J15), one side has to pull up the line. When the jumper is connected, the SDA line will get pulled high. This needs to be done when the user wants the I2C link to be pulled up by CY3275 board. This jumper does not need to be placed if the USB-I2C bridge is used for communication to the host.
JP3 (I2C-SCL)	This is a pull up jumper. While communicating through I2C(J15), one side has to pull up the line. When the jumper is connected, the SCL line will get pulled high. This needs to be done when the user wants the I2C link to be pulled up by CY3275 board. This jumper does not need to be placed if the USB-I2C bridge is used for communication to the host.
P40-P46	Port pins connected to LCD card
P47	Free port pin
P01,P02,P04, P07	Free port pins
P21	Port pin connected to yellow LED for BIU
P23	Port pin connected to Red LED for RX
P25	Port pin connected to Green LED for TX
P26	Free port pin
P17	Port pin connect to SCL for I2C
P15	Port pin connect to SDA for I2C
P16, P12	Free port pins
P30,P31,P32,P33,P34,P35, P36, P37	Free port pins
P50,P51,P52,P53	Free port pins
SW	Header connected to the switch S4. S4 is a general purpose switch
VR	Header connected to the potentiometer

#### Table 2-4. Headers and Jumpers



Headers and Jumpers	Description
	V - Vdd pin: This pin can provide a maximum of 50 mA at 5V to an external board only when the input to the board is 12V. For input voltages greater than 12V do not use this pin to power another board. This pin is only to source the current. DO NOT SUPPLY POWER TO THIS PIN FOR POWERING THE CY8CPLC20 DEVICE. Note that the PWR jumper (JP1) needs to be connected to enable this functionality.
J15	G - Gnd Pin: This pin can provide the ground reference to an external board. This pin connects to the ground pin of the external board.
	D - I2C Data (SDA): This is the data line for the I2C communication. This pin is directly connected to the CY8CPLC20 device
	C - I2C Clock (SCL): This is the clock line for the I2C communication. This pin is directly connected to the CY8CPLC20 device.
	R – Reset: Connecting this pin to an external board enables the CY8CPLC20 chip to be reset by an external board. Note that the RES jumper needs to be connected for enabling this functionality.

#### 2.3.4.3 Potentiometer and DIP Switches

There are 8-bit general purpose dip switches (S3) provided for the user. A general purpose potentiometer (R47) is provided next to the dip switches. This potentiometer can be routed to the chip using the GPIO pins. The second potentiometer (R46) is specifically meant to control the contrast for the LCD daughter card in the LCD1 slot.

#### Figure 2-4. Dip Switches



#### Key components and their use:

Component	Description
S3[7-0]	These dip switches are general purpose and can be routed to any port of the CY8CPLC20 chip.
Potentiometer [R47]	This is a variable resistor that connects to the VR header. It can be used to generate a voltage between +5V and GND.
LCD Contrast[R46]	Adjusting this potentiometer adjusts the contrast on the LCD Daughter Card.



### 2.3.5 LCD Daughter Card

This card is an LCD module easily connected to the board. It is connected and controlled by using the CY8CPLC20 GPIOs.

Figure 2-5. LCD Daughter Card



It is connected to the main board as shown in Figure 2-5.

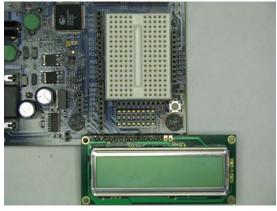
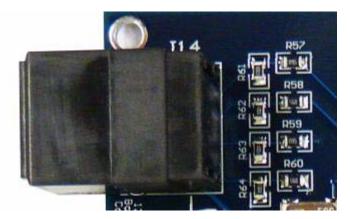


Figure 2-6. LCD Daughter Card Connection

#### 2.3.6 Debugger

The RJ45 ICE Cube Emulation Connector provides a debug interface between the CY8CPLC20-OCD device and the ICE Cube emulation tool using the PSoC Designer software application.

Figure 2-7. RJ45 Connector

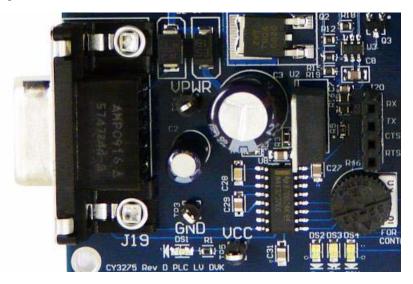




### 2.3.7 RS232-COM Port

The RS232 COM Port can be used with a standard RS232 cable to connect two RS232 capable devices together. The RS232 header (J20) is a four pin header that has connections for the RX, TX, RTS and CTS lines. These need to be wired to port pins to connect the device to the respective pins on the RS232 DB9 port.

Figure 2-8. RS232- COM Port



The controls associated with this are.

Control	Description/Comment
RX	The board receives the RS232 information through this pin
ТХ	The board transmits RS232 information through this pin
RTS	The host asks the chip if it can send information through this pin
CTS	The chip signals that it is ready to accept information through RX

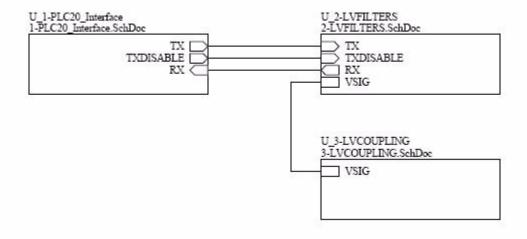


# A. Appendix



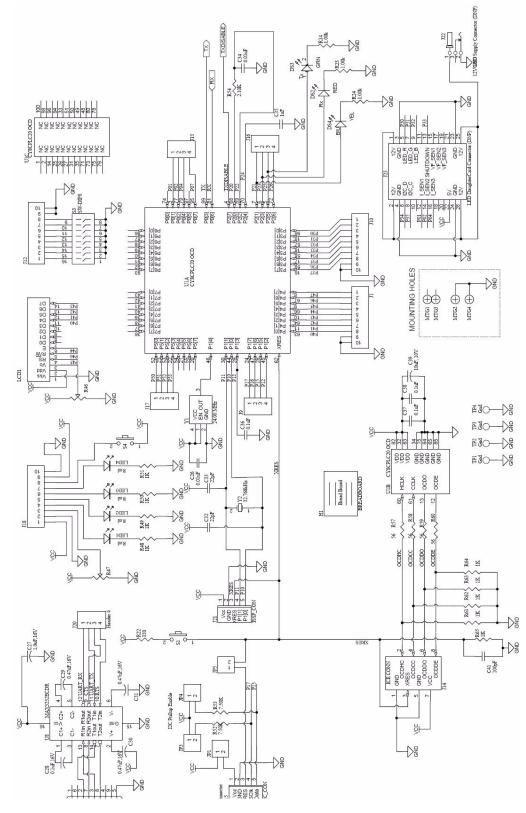
## A.1 Schematics

A.1.1 Board Overview



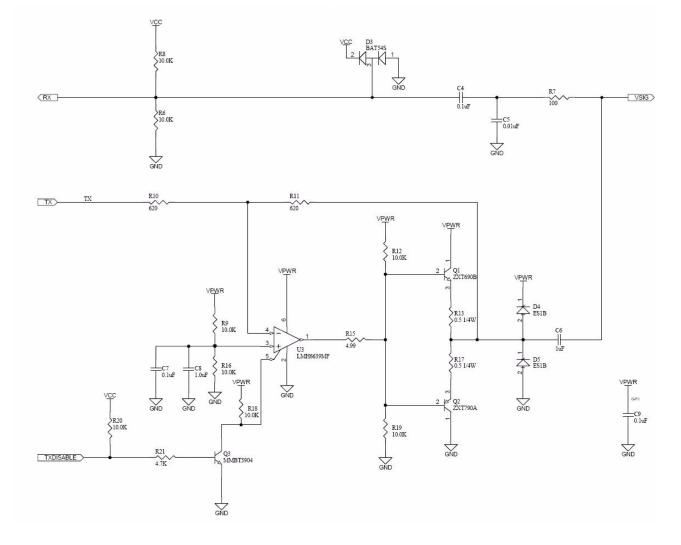


## A.1.2 User Interface



CY3275 Cypress Low Voltage Programmable PLC Development Kit Guide, Doc. # 001-53657 Rev. \*B



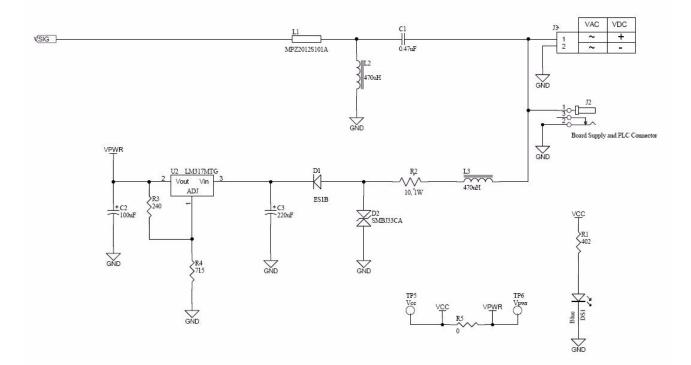


## A.1.3 Transmit and Receive Filter Coupling

21



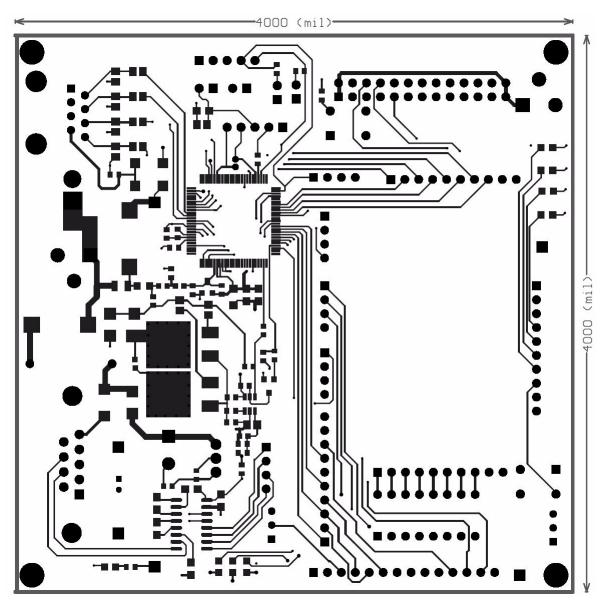
## A.1.4 Power Supply





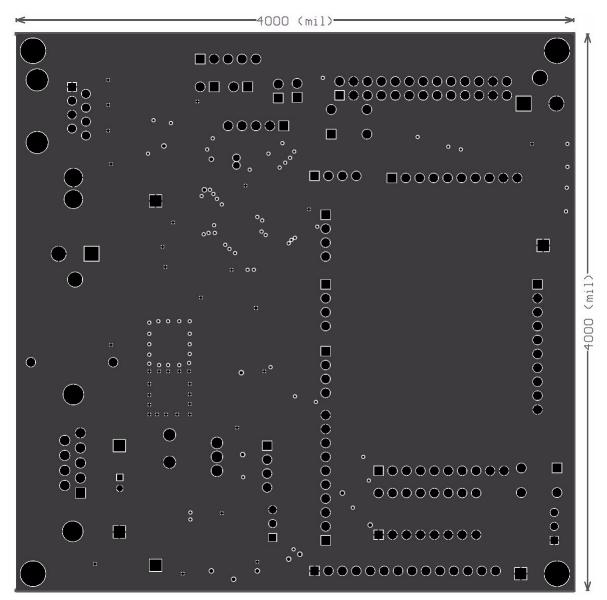
## A.2 Layout

## A.2.1 Top Layer





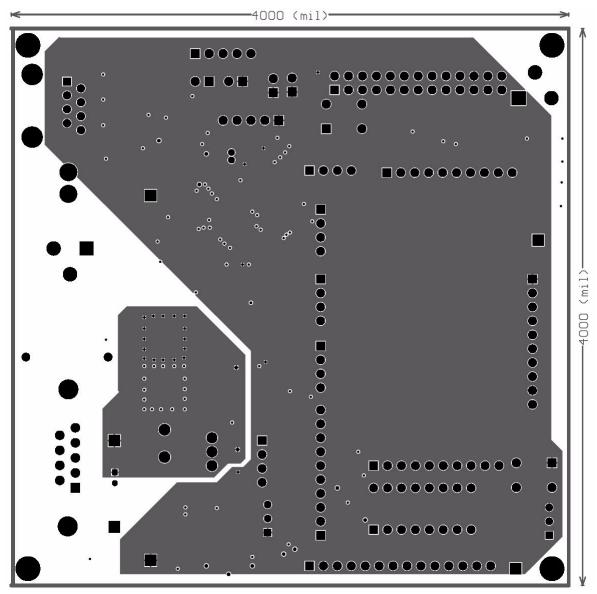
## A.2.2 Ground Layer



24

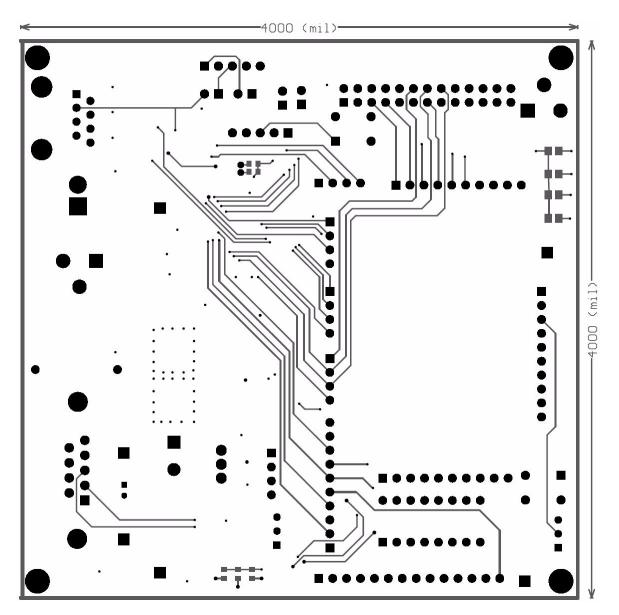


## A.2.3 Power Layer





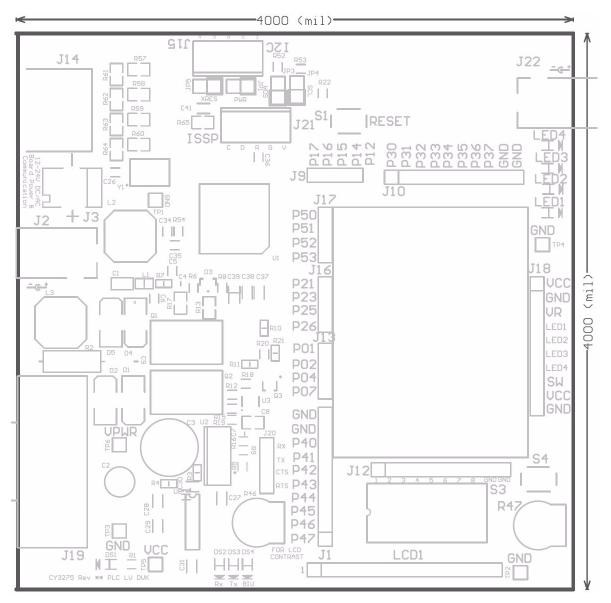
## A.2.4 Bottom Layer



26

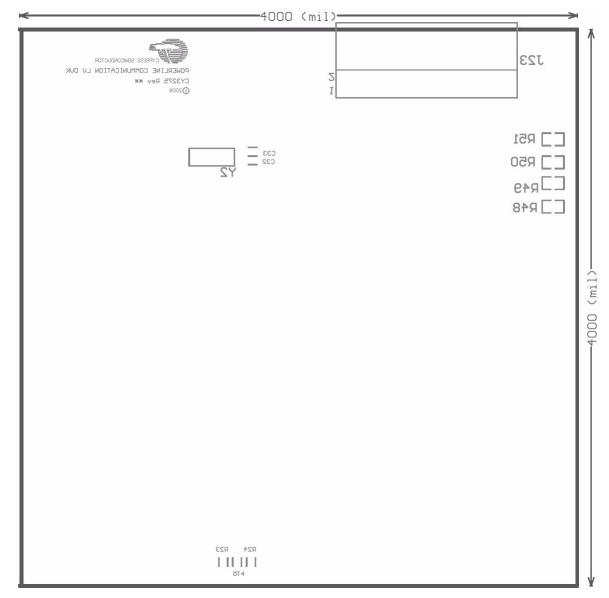


## A.2.5 Top Silkscreen





## A.2.6 Bottom Silkscreen





## A.3 Bill of Materials

Description	Designator	Quan tity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
Capacitor Ceramic 0.47UF 50V X7R 10% 1206	C1	1	0.47uF	ТДК	C3216X7R1H47 4K	445-1380-1-ND
Capacitor 100UF 10V ALUM LYTIC RADIAL	C2	1	100uF	PANASONIC	ECA-1AM101	P5123-ND
Capacitor Electrolytic 220uF 50V	C3	1	220uF	PANASONIC	ECA-1HM221	P5183-ND
Capacitor Ceramic 0.1uF 25V X7R 0603	C4, C7, C9	3	0.1uF	AVX	06033C104JAT2 A	478-3713-1-ND
Capacitor Ceramic 0.01uF 25V C0G 5% 0603	C5	1	0.01uF	ток	C1608C0G1E10 3J	445-2664-1-ND
Capacitor Ceramic 1.0uF 16V X7R 0603	C6, C35	2	1uF	Murata	GRM188R71C10 5KA12D	490-3900-1-ND
Capacitor Ceramic 1UF 50V Y5V 0805	C8	1	1.0uF	Murata	GRM21BF51H10 5ZA12L	490-3903-1-ND
Capacitor Ceramic 0.01uF 25V X7R 0603	C26, C34	2	0.01uF	AVX	06033C103JAT2 A	06033C103JAT 2A-ND
Capacitor 1.0uF, 16V	C27	1	1.0uF,1 6V			PCC1849TR- ND
Capacitor 0.1uF, 16V	C28	1	0.1uF,1 6V			PCC1864TR- ND
Capacitor 0.47uF, 16V	C29, C30, C31	3	0.47uF, 16V			PCC1847TR- ND
Capacitor Ceramic 22pF 100V C0G 0603	C32, C33	2	22pF	Murata	GRM1885C2A22 0JA01D	490-1335-1-ND
Capacitor Ceramic 0.1uF 25V X7R 0603	C36	1	0.1uF	AVX	06033C104JAT2 A	478-3713-1-ND
Capacitor 0.1uF	C37, C38	2	0.1uF			PCC1864TR- ND
Capacitor 10uF,10V	C39	1	10uF,1 0V	Vishay	293D106X9010A 2TE3	718-1121-1-ND
Capacitor 100pF	C41	1	100pF			399-1121-2-ND
Diode Super Fast 100V 1A	D1	1		Diodes Inc.	ES1B-13-F	ES1B-FDICT- ND
Diode TVS 33V 600W BI- DIR SMB	D2	1		Littelfuse	SMBJ33CA	SMBJ33CALFC T-ND
Diode Schottky 40V 0.3A SOT-23	D3	1		ST Micro	BAT54SFILM	497-2522-1-ND
Diode Ultrafast 100V 1A	D4, D5	2		Diodes Inc.	ES1B	ES1B-FDICT- ND

CY3275 Cypress Low Voltage Programmable PLC Development Kit Guide, Doc. # 001-53657 Rev. \*B



Description	Designator	Quan tity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
Blue LED	DS1	1	Blue		SML- E12BC7TT86	511-1589-1-ND
LED Red Clear 0805	DS2	1		Lite-On	LTST- C170KRKT	160-1415-1-ND
LED Green Clear 0805	DS3	1		Lite-On	LTST- C170KGKT	160-1414-1-ND
LED Yellow Clear 0805	DS4	1		Lite-On	LTST- C170KSKT	160-1416-1-ND
3M solderless breadboard super strip	H1	1		Parallax	700-00012	923273-ND
Header, 10-Pin	J1, J10, J12, J18	4	10			929850E-01-36- ND
Power connector	J2	1		CUI Inc	PJ-102A	CP-102A-ND
Power Header, 2-Pin	J3	1		MOLEX	09-65-2028	WM18823-ND
Header, 4-Pin	J9, J13, J17, J20	4	4			929850E-01-36- ND
ICE Connection	J14	1		Тусо	5557785-1	A31457-ND
ISSP Conn	J15	1				WM4203-ND
Header, 4-Pin	J16	1	4			929850E-01-36- ND
Female DB-9	J19	1	DB9-F			A23301-ND
ISSP Conn	J21	1				WM4203-ND
(DO NOT POPULATE) Power Connector Jack 2.1mm PCB	J22					
(DO NOT POPULATE) Right Angle 2X13 header 0.1" Spacing	J23					
Header, 2-Pin, Male	JP1, JP3, JP4, JP5	4	2	Generic Com- ponents		S1011E-36-ND
Ferrite Chip 100 OHM 4A 0805	L1	1		ток	MPZ2012S101A	445-1567-1-ND
Inductor PWR UNSHIELD 470UH SMD	L2, L3	2	470uH	Pulse	P0752.474NLT	553-1071-1-ND
14-Pin header, Female	LCD1	1	14	3M/ESD	929850-01-36- RA	929850E-01-36- ND
Red LED	LED1, LED2, LED3, LED4	4	Red		SML- LXT0805IW-TR	67-1552-2-ND



Description	Designator	Quan tity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
Mounting Holes	MTG1, MTG2, MTG3, MTG4	4				
Transistor NPN 45V 3A	Q1	1		Zetex	ZXT690BKTC	ZXT690BKCT- ND
Transistor PNP 40V 3A	Q2	1		Zetex	ZXT790AKTC	ZXT790AKCT- ND
Transistor NPN SOT-23	Q3	1		Fairchild	MMBT3904LT1	MMBT3904LT1I NCT-ND
Resistor 402 OHM 1/10W 1% 0603 SMD	R1	1	402	Rohm	MCR03EZPFX4 020	RHM402HCT- ND
Resistor 10 OHM 1W 5% METAL OXIDE	R2	1	10 Ohm, 1W	Stackpole	RSMF 1 10 5% R	RSMF110JRCT -ND
Resistor 240 OHM 1/10W 1% 0603 SMD	R3	1	240	Rohm	MCR03EZPFX2 400	RHM240HCT- ND
Resistor 715 OHM 1/10W 1% 0603 SMD	R4	1	715	Rohm	MCR03EZPFX7 150	RHM715HCT- ND
Resistor 0.0 OHM 1/10W 5% 0603 SMD	R5	1	0	Rohm	MCR03EZPJ000	RHM0.0GCT- ND
Resistor 10.0k 1% 1/10W 0603	R6, R8, R9, R12, R16, R18, R19,R20	8	10.0K	Rohm	MCR03EZPFX1 002	RHM10.0KHCT -ND
Resistor 100 OHM 1/10W 1% 0603 SMD	R7	1	100	Rohm	MCR03EZPFX1 000	RHM100HCT- ND
Resistor 620 OHM 1/10W 1% 0603 SMD	R10, R11	2	620	Rohm	MCR03EZPFX6 200	RHM620HCT- ND
Resistor 0.5 1% 1/4W 0805	R13, R17	2	0.5 1/ 4W	Susumu	RL1220S-R50-F	RL12S.50FCT- ND
Resistor 1.00k 1% 1/10W 0603	R14, R23, R24	3	1.00k	Yageo	RC0603FR- 071KL	311- 1.00KHRTR-ND
Resistor 4.99 1% 1/10W 0603	R15	1	4.99	Yageo	RC0603FR- 074R99L	311-4.99HRCT- ND
Resistor 4.70K OHM 1/ 10W 1% 0603 SMD	R21	1	4.7K	Yageo	RC0603FR- 074K7L	311- 4.70KHRCT-ND
Resistor 330 Ohm 1% 1/ 10W 0603	R22	1	330	Rohm	MCR03EZPFX3 300	RHM330HCT- ND
Potentiometer	R46, R47	2		Bourns Inc	3352T-1-103LF	3352T-103LF- ND



Description	Designator	Quan tity	Value	Manufacturer	Manufacturer Part#	Digi-Key#
Resistor 1.0K, SMT	R48, R49, R50, R51, R61, R62, R63, R64, R65	9	1K	Panasonic	ERJ- 6GEYJ102V	P1.0KACT-ND
Resistor 7.50k 1% 1/10W 0603	R52, R53	2	7.50K	Rohm	MCR03EZPFX7 501	RHM7.50KHCT -ND
Resistor 2.10k 1% 1/10W 0603	R54	1	2.10K	Rohm	MCR03EZPFX2 101	RHM2.10KHCT -ND
Resistor 56 Ohm, SMT	R57, R58, R59, R60	4	56			P56ACT-ND
Swtich, SPST	S1, S4	2		Omron	B3F-1022	SW403-ND
4009 Series DIP Switch, Raised actuator	S3	1		ESwitch	KAJ08LAGT	EG4441-ND
Simple Test point	TP1, TP2, TP3, TP4	4				5006K-ND
Simple Test point	TP5	1				5006K-ND
Simple Test point	TP6	1				5006K-ND
CY8CPLC20 OCD Part	U1	1		Cypress	CY8CPLC20- OCD	
Voltage Regulator 5 Volt	U2	1		ST Micro	LM317MTG	LM317MTGOS- ND
Op-Amp 190MHz	U3	1		National Semi- conductor	LMH6639MF/ NOPB	LMH6639MFCT -ND
RS-232 tranceiver (1.0uF Caps)	U8	1			MAX3232ECDR	296-19851-2- ND
Oscillator	Y1	1	24.00 MHz	Crystek	C3290-24.000	C3290-24.000- ND
	Y1 (2nd source)			Citizen	CSX750FCC24. 000M-UT	300-7214-2-ND
Crystal 32.768kHz 12.5pF	Y2	1	32.768 kHz	ECS Inc.	ECS-3X8X	X1123-ND
LCD Module	LCD1	1		Cypress Semi- conductor	1187-00003	