UM0819
User manual

Getting started with STEVAL-PCC010V1, ST802RT1 TX mode Ethernet PHY demonstration kit

1 Introduction

The STEVAL-PCC010V1 demonstration kit was designed to evaluate the ST802RT1 TX mode. This device is a Fast Ethernet physical layer (PHY) interface which supports 100 Base-TX and 10 Base-T applications. The PHY provides a Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for easy attachment to a 10/100 Media Access Controllers (MAC). The demonstration board features jumpers, test points and connectors to test the ST802RT1 TX mode Ethernet PHY.
To quickly evaluate the microcontroller and physical layer, the device can be connected to the STM32F107 controller demonstration board through an additional header connector. The controller board is preprogrammed with a web server demonstration application. The STM32F107 controller demonstration board is part of the STEVAL-PCC010V1 package delivery.
The board can be equipped with a dedicated digital connector compatible to the Spirent® Communications SmartBits 200/2000 (SMB-200/ SMB-2000) analysis system.

Figure 1. ST802RT1 TX mode Ethernet PHY demonstration board - top view

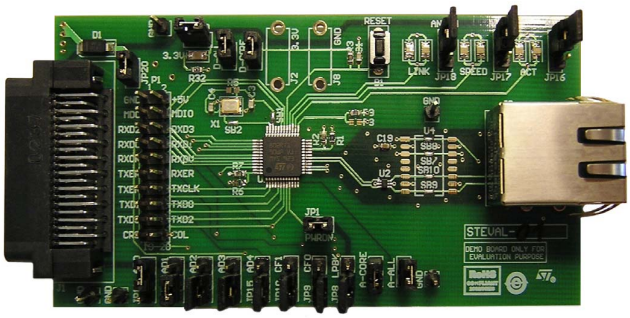
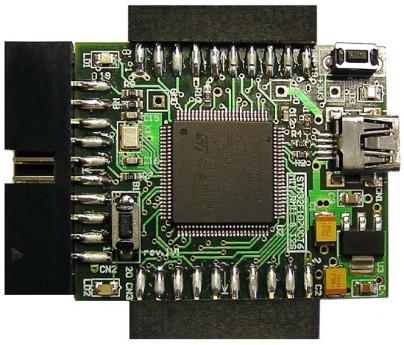


Figure 2. STM32F107 controller demonstration board - top view



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2 Boards key features

2.1 ST802RT1 TX mode Ethernet PHY demonstration board

- ST802RT1 TX mode Fast Ethernet physical layer transceiver
- On-board 3.3 V LDO regulator
- On-board 25 MHz crystal
- 12 jumpers for boot-strap configuration (MII address, auto-negotiation, loopback, power-down, MII/RMII configuration)
- Several GND test points and jumpers for power consumption measurement
- Connectors
  - 20-pin full pitch header connector for debug purposes (compatible to the STM32F107 controller board)
  - 40-pin connector compatible to the Spirent Communications SmartBits 200/2000 (SMB-200/ SMB-2000) analysis system (not assembled)
  - RJ45 connector with embedded transformer

2.2 STM32F107 controller demonstration board

- STM32F107 connectivity line Cortex™-M3 based microcontroller with embedded Ethernet MAC
- On-board 3.3 V LDO regulator
- On-board 25 MHz crystal
- Reset button, power LED, general-purpose button and two LEDs
- Connectors
  - 20-pin full pitch header connector for debug purposes and compatibility to the ST802RT1 TX mode demonstration board
  - 20-pin JTAG connector
  - Additional general-purpose 20-pin full pitch header connector
  - USB device connector (+5 V power supply)

3 General system description

The STEVAL-PCC010V1 ST802RT1 TX mode Ethernet PHY demonstration kit consists of two boards. The ST802RT1 TX mode demonstration board was designed to evaluate the chip. It therefore allows to easily select the PHY boot options, to evaluate the PHY boot options, to evaluate the power consumption of the chip and to attach the device to the professional test equipment.

In addition, the STM32F107 controller demonstration board can extend the ST802RT1 TX mode demonstration board with STM32™ microcontroller and its embedded MAC. This allows to quickly evaluate application on the embedded microcontroller and the Ethernet PHY. By default, the controller board is preprogrammed with a web-server application for demonstration purposes.

Figure 3. ST802RT1 TX mode Ethernet PHY demonstration kit

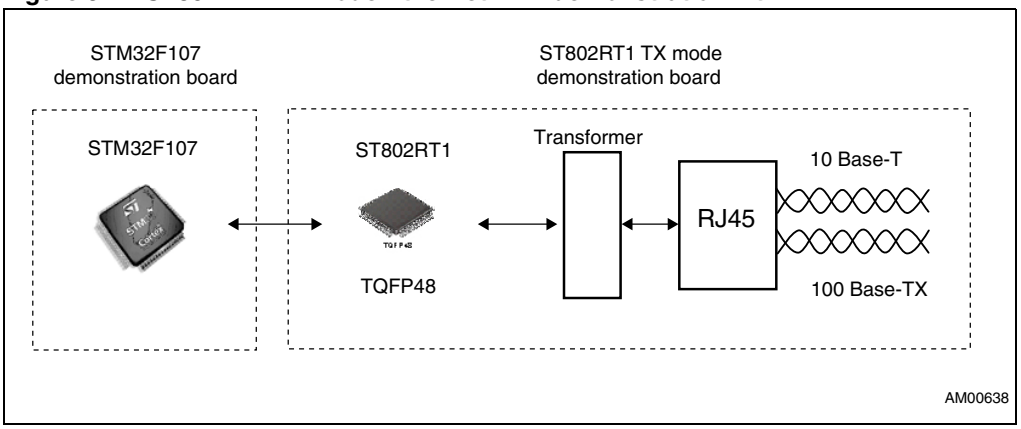


Figure 3 shows the ST802RT1 TX mode Ethernet PHY demonstration kit. It consists of two boards: the ST802RT1 TX mode Ethernet PHY demonstration board, and the STM32F107 controller demonstration board connected through the MII/RMII connector.

4 Getting started

This section briefly describes how to start using the STEVAL-PCC010V1 ST802RT1 TX mode Ethernet PHY demonstration kit. To use this demonstration kit you must install a web browser on your computer.

4.1 Package contents

The ST802RT1 TX mode Ethernet PHY demonstration kit includes the following items:

Hardware content

- One ST802RT1 TX mode Ethernet PHY demonstration board
- One STM32F107 controller demonstration board

Software content

- Web server - demonstration software based on uIP TCP/IP stack

Documentation

- STM32F107xx datasheet, ST802RT1 product documentation
- This user manual

4.2 How to run the demonstration software

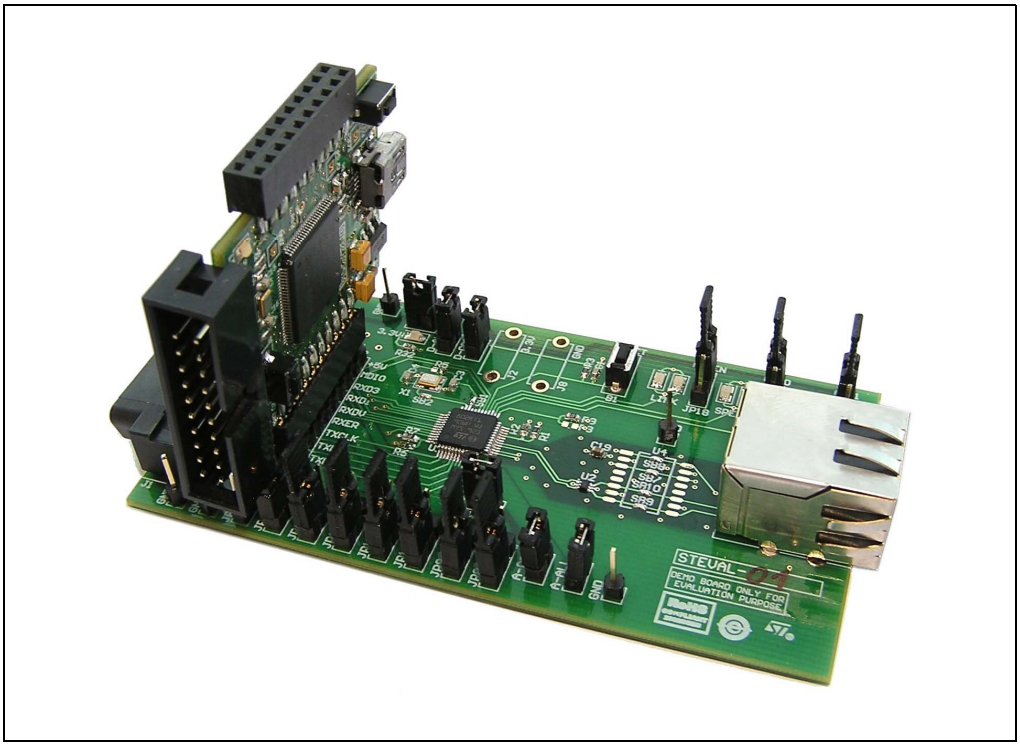
This section describes the demonstration software delivered with the ST802RT1 TX mode Ethernet PHY demonstration kit. The software implements a simple web server based on uIP TCP/IP stack. The web server consists of three pages displaying general information about the STM32 and ST802RT1 TX mode, allowing to control LEDs on the STM32F107 controller board and finally showing the content of the ST802RT1 TX mode registers.

To run the demonstration software, you need a demonstration kit, an Ethernet cable, and a PC with a web browser.

Follow the steps below:

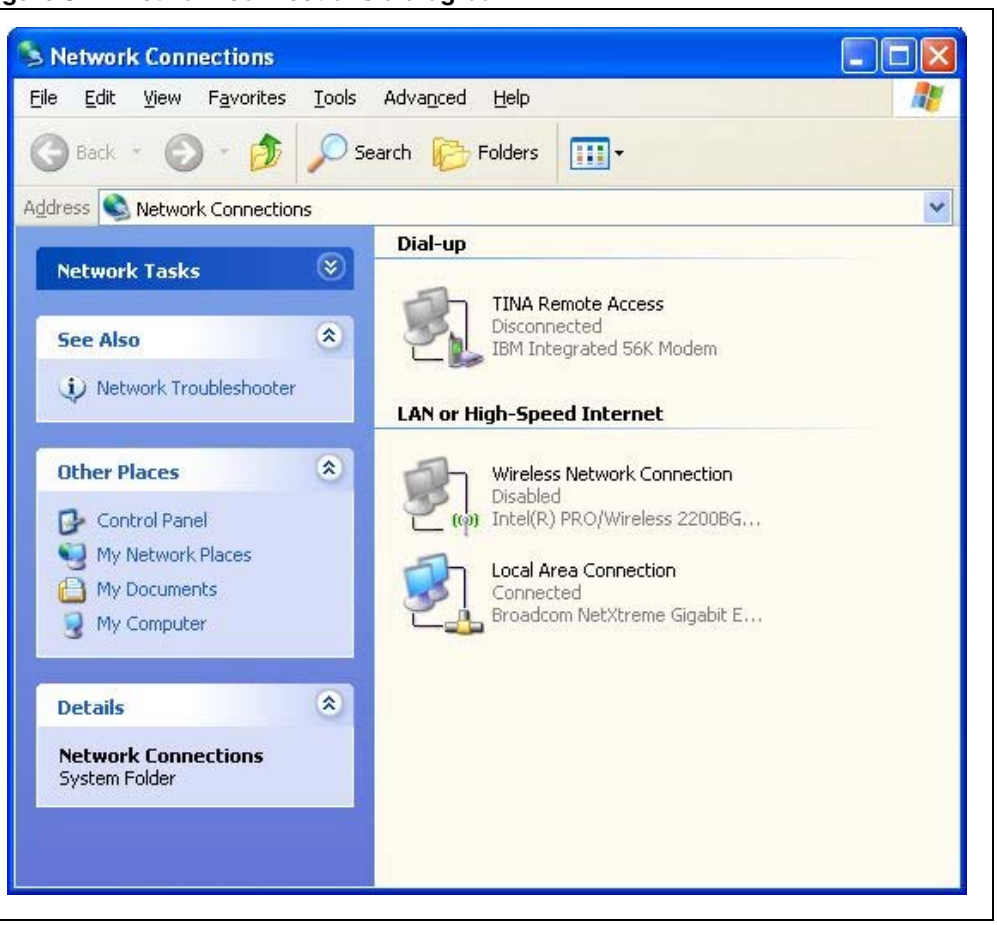
1. Connect the boards delivered in the package as shown on the *Figure 4*.

Figure 4. ST802RT1 TX mode demonstration board connected to STM32F107 demonstration board



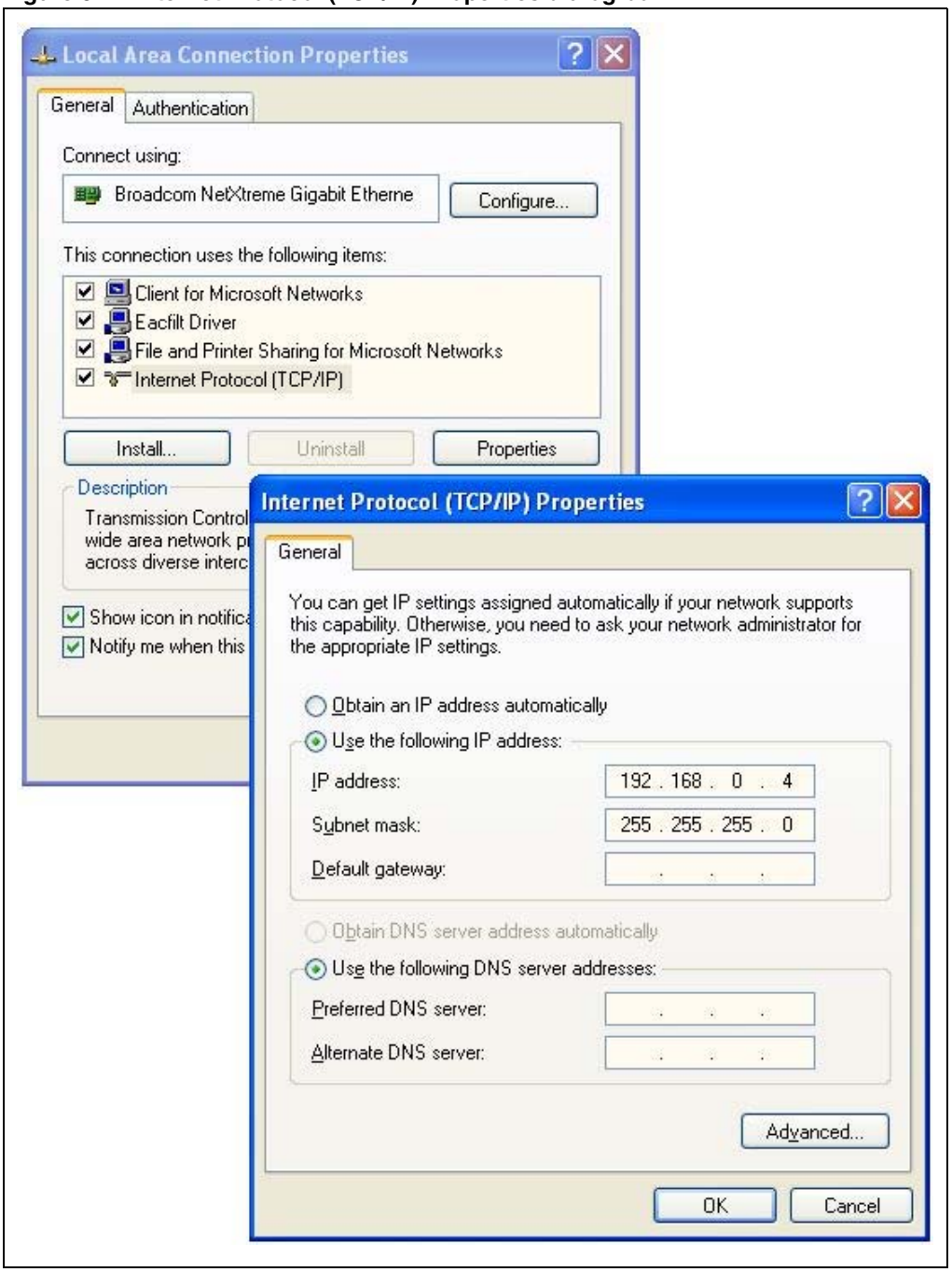
2. Setup properly jumpers on the ST802RT1 TX mode Ethernet PHY demonstration board. The software does not change any settings of the PHY; it reads the settings from the PHY instead. See *Section 6.1* for more details about board setup.
3. Connect ST802RT1 TX mode Ethernet PHY board to STM32F107 controller board.
4. Connect Ethernet cable to the ST802RT1 TX mode Ethernet PHY board on one side and to the PC on the other side.
5. Flash the demonstration software into the Flash memory of the STM32F107 MCU.
6. Configure your PC. The following description is valid for Windows® XP; nevertheless it is easy to setup any other operating system in a similar way.
   a) Setup network settings: in Control Panel - Network Connections right click your network card and open Properties.

Figure 5. Network connections dialog box



b) Select IP protocol properties: select Internet Protocol (TCP/IP) and click Properties.

Figure 6. Internet Protocol (TCP/IP) Properties dialog box

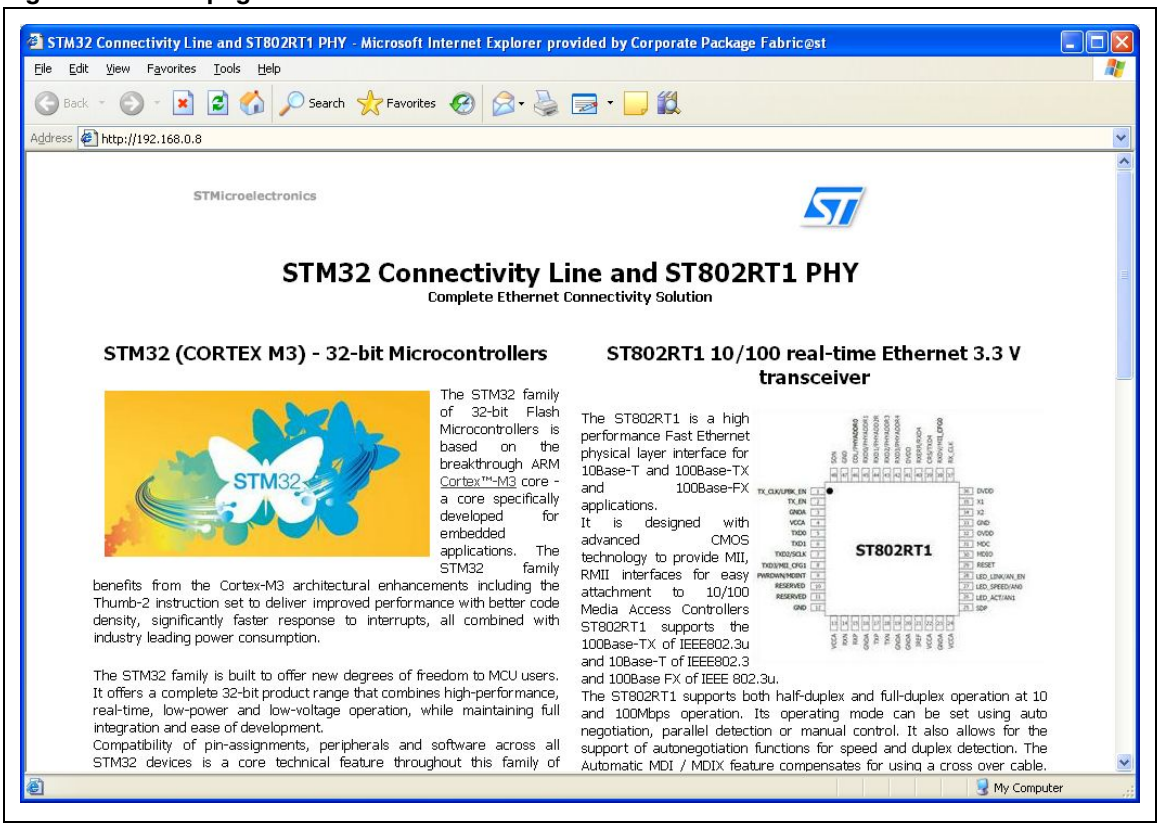


c) Change you IP settings to:
IP address: 192.168.0.4
Subnet mask: 255.255.255.0

d) Disable firewall(s) running on your PC.

7. Run your web browser and open page http://192.168.0.8. You should be able to see the first page of the web server running on the demonstration kit.

Figure 7. First page of the web server demonstration software

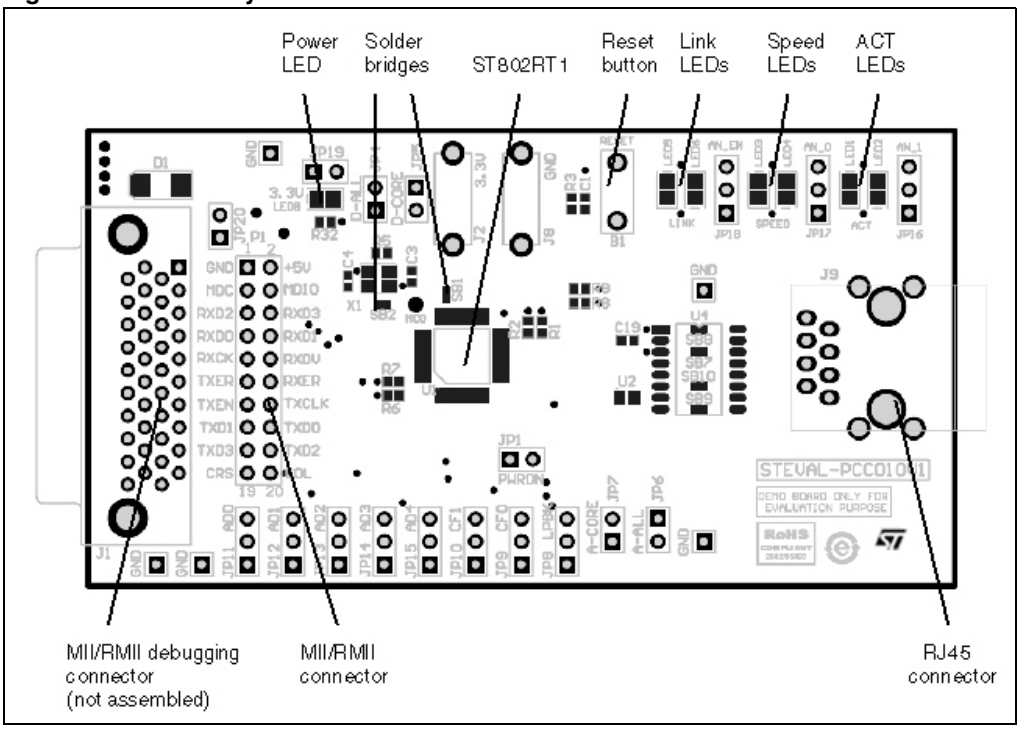


8. You can also ping to the board using ping command on your PC.

5 Boards layout

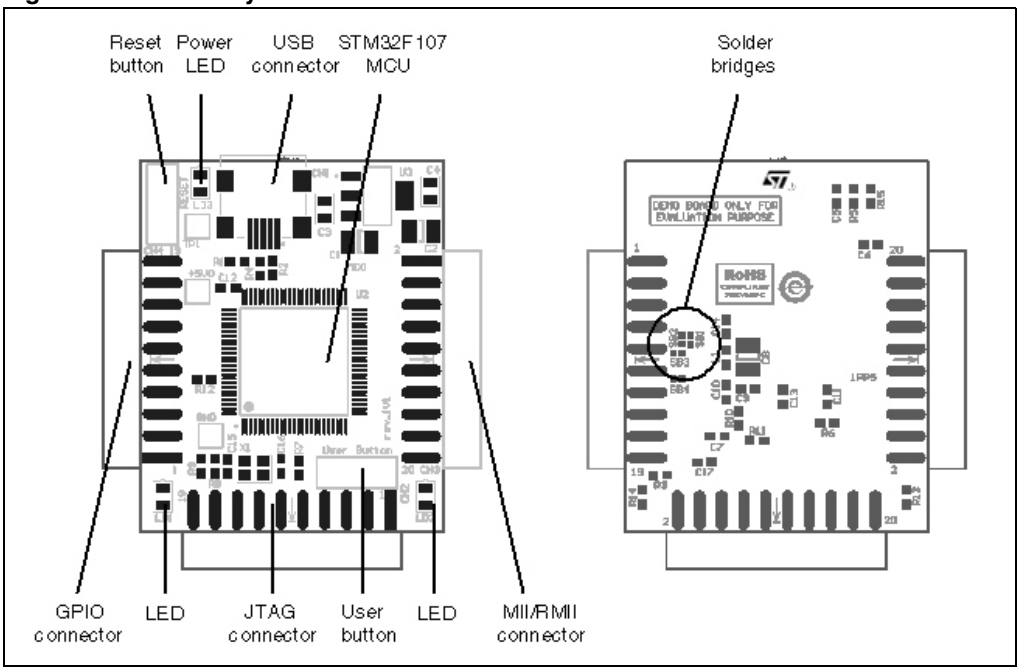
5.1 Board layout - ST802RT1 TX mode Ethernet PHY demonstration board

Figure 8. Board layout - ST802RT1 TX mode Ethernet PHY demonstration board



5.2 Board layout - STM32F107 controller demonstration board

Figure 9. Board layout - STM32F107 controller demonstration board



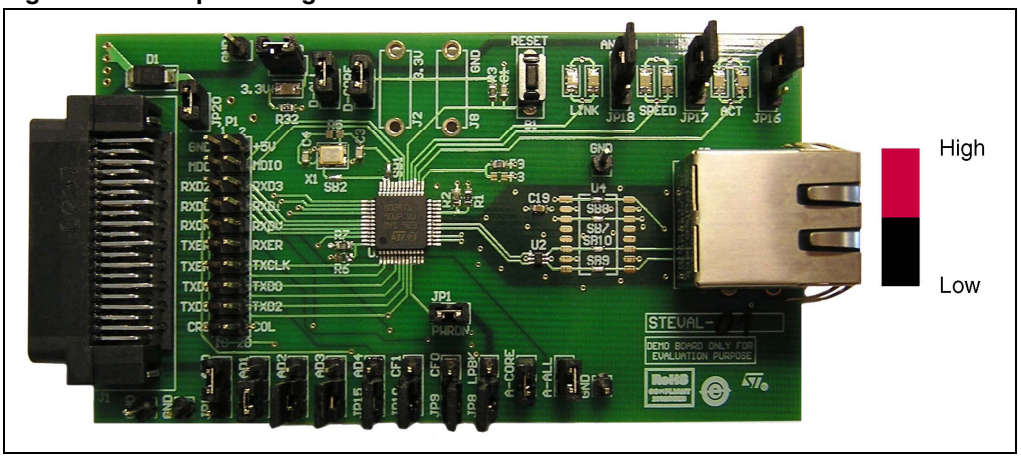
6 Configuration and functionality

This section describes the functions and configuration of STM802RT1A Ethernet PHY demonstration board and STM32F107 controller demonstration board.

6.1 Configuration and functionality- ST802RT1 TX mode Ethernet PHY demonstration board

In this chapter jumper “high” means that the jumper is placed in the position closer to the top edge of the board and “low” means that the jumper is placed in the position closer to the bottom edge of the board as shown by *Figure 10*.

Figure 10. Jumper configuration



6.1.1 Boot strap options

The ST802RT1 TX mode PHY uses many of the functional pins as strap options. The values of these pins are sampled during hardware reset and power up. They are used to strap signals on the device into specific modes of operation. The ST802RT1 TX mode provides a simple strap option to automatically configure the device to operate in the modes requiring no device register configuration. All strap pins have a weak internal pull-ups or pull-downs. To change the default strap value, the strap pins should be connected directly to V_{CC} or GND with an external 2.2 kΩ resistor. The software reset and power-down through the power-down pin cannot be used to change the strap configuration.

Auto-negotiation

Auto-negotiation is performed as part of the initial set-up of the link. It allows the PHYs connected to the cable to exchange their key features (speed, PHY type, half or full duplex) and automatically select the link communication mode. If auto-negotiation is disabled the chip stays at the speed that is selected by strap pins. If the partner PHY speed is the same, the link ON state is signaled otherwise no link state is signaled.

Table 1. Auto-negotiation jumper settings(1)

Jumper	Description	Default configuration
JP16	AN_1	High
JP17	AN_0	High
JP18	AN_EN - Auto-negotiation enable; when “high” - auto-negotiation enabled, when “low” - auto-negotiation disabled	High

1. See functionality of AN_xxx pins in the ST802RT1 product documentation.

PHY MII address

The MDIO/MDC serial management interface is used to access the internal registers of the PHY. The Ethernet MAC that is connected to the PHY must know the appropriate PHY address for successful communication. Special case is the PHY address 0x00. If this address is used as the bootstrap address during the reset, the 00000 value is latched into the internal receive mode control register RN14 (0x14h) but the PHY goes also to the isolation mode. It is possible to change the PHY address by writing the RN14 register later when application is already running.

Table 2. PHY MII address jumper settings

Jumper	Description	Default configuration
JP11	MII address 0	High
JP12	MII address 1	Low
JP13	MII address 2	Low
JP14	MII address 3	Low
JP15	MII address 4	Low

Power-down

This pin is an active low input of the PHY and should be asserted low to put the device in a power-down mode. During the power-down mode, TXP/TXN outputs and all LED outputs are 3-stated, and the MII interface is isolated. The power-down functionality is also achievable by software by asserting bit 11 of register RN00.

Table 3. Power-down jumper settings

Jumper	Description	Default configuration
JP1	Power-down, if fitted - PHY works normally; if not fitted - PHY is in power-down mode	Fitted

Loopback

Local loopback passes data internally from the transmitting to the receiving serial analog logic. There are two ways to enter the internal loopback mode, either writing RN00 register, bit 14 (MDIO/MDC) or by using boot strap LPBK pin (V_{DD} - enabled, GND - disabled, through 2.2 kΩ resistor).

Table 4. Loopback jumper setting

Jumper	Description	Default configuration
JP8	LPBK - loopback; “high” - internal loopback selected (mainly for debug purposes); “low” - normal operation	Low

MII/RMII mode selection

A strapping option allows setting the operating mode of the MAC data interface. Default operation (no pull-ups) enable normal MII mode of operation. Strapping CF0 high will cause the device to be in RMII.

Table 5. MII/RMII jumper settings

Jumper	Description	Default configuration
JP9	CF0 - MAC data interface selection	Low
JP10	CF1 - MAC data interface selection	Low

Table 6. MII/RMII interface selection

	CF0 (JP9)	CF1 (JP10)
MII	Low	X
RMII	High	Low

6.1.2 Solder bridges

The SB1 and SB2 solder bridges are used to connect 25MHz crystal X1 to the ST802RT1 TX mode PHY. They can be removed to disconnect the crystal when external clock signal on test point MCO is used as the input clock.

6.1.3 RESET button

The RESET button resets the ST802RT1 TX mode PHY to its initial state.

6.1.4 LEDs

By default the LEDs have the following functionality:

Table 7. LEDs functionality - alternative 1

LED	Description	Details
LED1	BLINK for activity	JP16 is low
LED2	BLINK for activity	JP16 is high
LED3	ON for 100 Mb / OFF for 10 Mb	JP17 is low
LED4	ON for 100 Mb / OFF for 10 Mb	JP17 is high
LED5	ON for link up / OFF for link down	JP18 is low
LED6	ON for link up / OFF for link down	JP18 is high

Alternatively it is possible to change the meaning of LED1 - LED6 by writing the PHY register RN1B [0d27, 0x1B]:

Table 8. LEDs functionality - alternative 2

LED	Description	Details
LED1	ON for full duplex, BLINK for collision	JP16 is low
LED2	ON for full duplex, BLINK for collision	JP16 is high
LED3	ON for 100 Mb / OFF for 10 Mb	JP17 is low
LED4	ON for 100 Mb / OFF for 10 Mb	JP17 is high
LED5	ON for link up and BLINK for activity / OFF for link down	JP18 is low
LED6	ON for link up and BLINK for activity / OFF for link down	JP18 is high
LED8	Is used for indicating that the board is powered	—

6.1.5 Test point MCO

The test point MCO can be used to connect external clock signal to clock input of the STM802RT1A PHY in MII mode. Note that the 25 MHz crystal X1 has to be disconnected from the ST802RT1 TX mode PHY by removing solder bridges SB1 and SB2 before connecting any external signal to the test point.

6.2 Configuration and functionality - STM32F107 controller demonstration board

6.2.1 MII/RMII configuration

The STM32F107 controller demonstration board can be configured to communicate with Ethernet PHY using either MII or RMII interface. The configuration is done using three solder bridges SB1, SB2 and SB3.

Table 9. MII/RMII interface selection by solder bridges SB1, SB2 and SB3

	SB1	SB2	SB3
MII	Remove	Remove	Fit
RMII	Fit	Fit	Remove

In MII mode, the ST802RT1 TX mode Ethernet PHY demonstration board can be clocked either from its on-board 25 MHz crystal oscillator or by the 25 MHz clock signal output - MCO from the STM32F107 controller demonstration board, see *Section 6.1.5* and *6.2.4*. Both MCO pins (test points) must be interconnected by an additional wire.

In RMII mode, the ST802RT1 TX mode Ethernet PHY demonstration board is clocked from the 50 MHz clock signal output delivered from the STM32F107 controller demonstration board.

6.2.2 Buttons

There are two buttons on the STM32F107 controller demonstration board. The RESET button resets the STM32F107 MCU to its initial state. The B1 general purpose button is connected to PA4-pin of STM32F107 MCU and is active low.

6.2.3 LEDs

There are three LEDs on the STM32F107 controller demonstration board. LD1 and LD2 are general purpose LEDs connected to PC13 and PC14-pins of the STM32F107 MCU. LD3 is used for indicating that the board is powered.

6.2.4 Test point MCO

There is MCO (Main Clock Output) clock signal of STM32 available on this test point which can be used as input clock source of the ST802RT1 TX mode PHY.

7 Connectors

7.1 Connectors of the ST802RT1 TX mode Ethernet PHY demonstration board

7.1.1 MII/RMII debugging connector J1

Figure 11. MII/RMII debugging connector J1

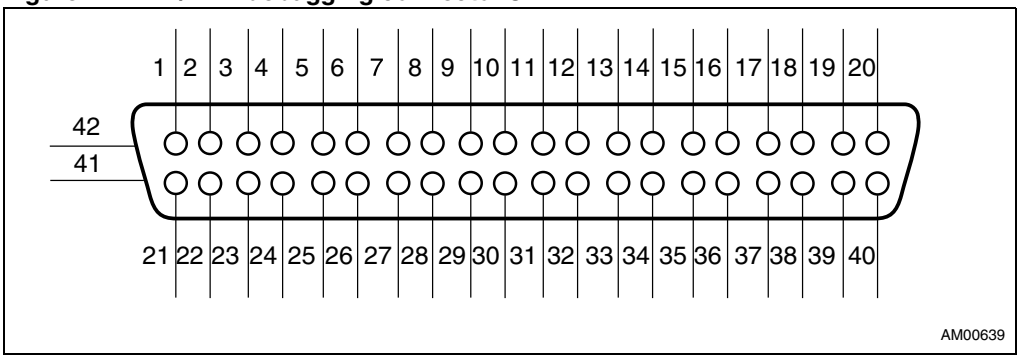


Table 10. MII/RMII debugging connector J1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	12	TXCLK	23	GND	34	GND
2	MDIO	13	TXEN	24	GND	35	GND
3	MDC	14	TXD_0	25	GND	36	GND
4	RXD_3	15	TXD_1	26	GND	37	GND
5	RXD_2	16	TXD_2	27	GND	38	GND
6	RXD_1	17	TXD_3	28	GND	39	GND
7	RXD_0	18	COL	29	GND	40	Not connected
8	RXDV	19	CRS	30	GND	41	GND
9	RXCLK	20	Not connected	31	GND	42	GND
10	RXER	21	+5 V	32	GND		
11	TXER	22	GND	33	GND		

7.1.2 MII/RMII connector P1

Figure 12. MII/RMII connector P1

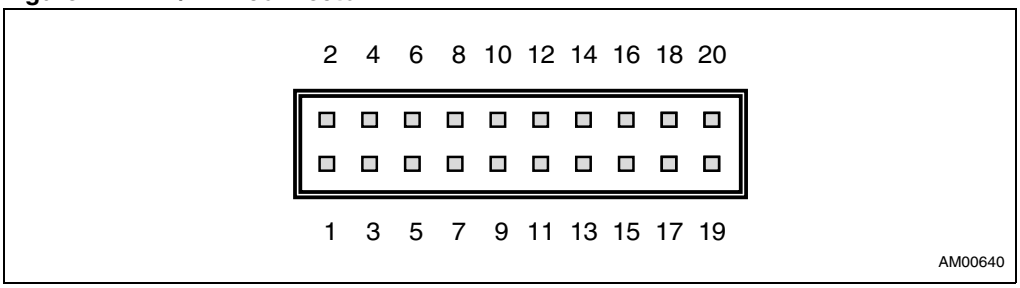


Table 11. MII/RMII connector P1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	RXD3	11	TXER	16	TXD0
2	+5 V	7	RXD0	12	RXER	17	TXD3
3	MDC	8	RXD1	13	TXEN	18	TXD2
4	MDIO	9	RXCLK	14	TXCLK	19	CRS
5	RXD2	10	RXDV	15	TXD1	20	COL

7.1.3 RJ45 connector J9

Figure 13. Ethernet RJ45 connector J9 - front view

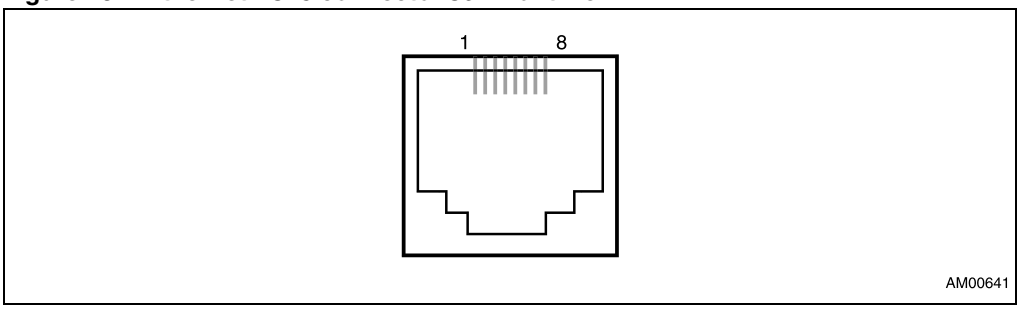


Table 12. RJ45 connector J9

Pin	Description	Pin	Description
1	TxData+	2	TxData–
3	RxData+	4	NC
5	NC	6	RxData–
7	NC	8	NC

7.2 Connectors of the STM32F107 controller board

7.2.1 USB connector CN1

Figure 14. USB connector CN1

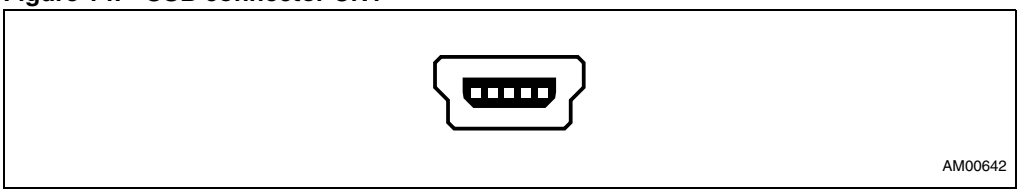


Table 13. USB connector CN1

Pin	Signal	Pin	Signal
1	V_{BUS}	4	ID
2	D–	5	GND
3	D+	6	SH

7.2.2 JTAG connector CN2

The 20-pin connector (CN2) provides the JTAG interface. This interface is primarily used for communicating with a PC using suitable USB/JTAG converter box such as J-Link from IAR Systems™ or R-Link from Raisonance, etc. There exists a wide choice of development tools on the market supporting microcontroller Flash memory programming and application debugging.

Figure 15. JTAG connector CN2

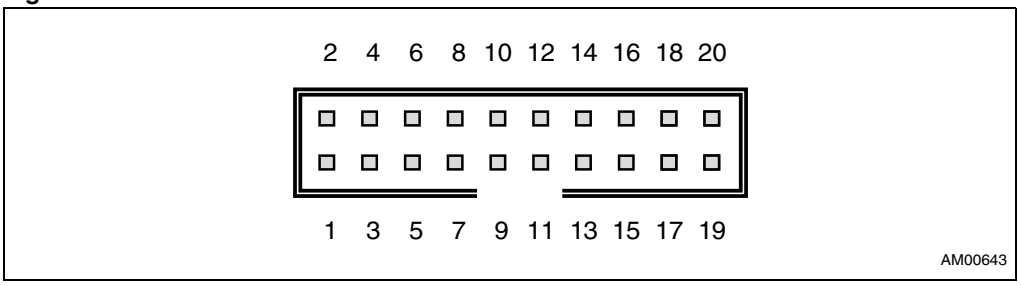
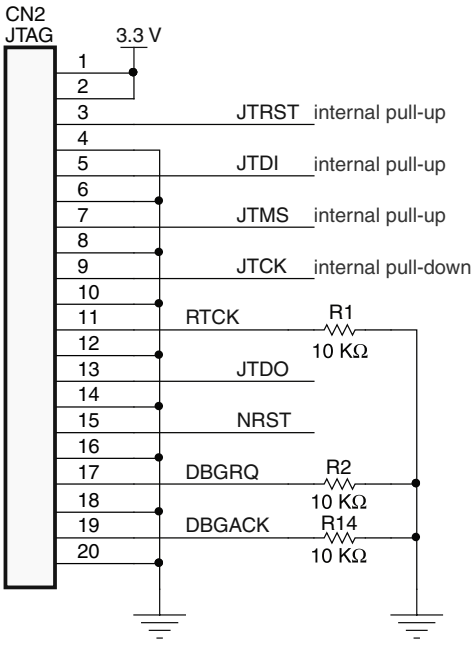


Table 14. JTAG connector CN2

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	3.3 V DC	6	GND	11	RTCK connected to GND by R1 (10 kΩ)	16	GND
2	3.3 V DC	7	JTMS	12	GND	17	DBGRQ connected to GND by R2 (10 kΩ)
3	JTRST	8	GND	13	JTDO	18	GND
4	GND	9	JTCK	14	GND	19	DBGACK connected to GND by R14 (10 kΩ)
5	JTDI	10	GND	15	NRST	20	GND

Figure 16. JTAG connector CN2 - schematic



7.2.3 MII/RMII connector CN3

Figure 17. MII/RMII connector CN3

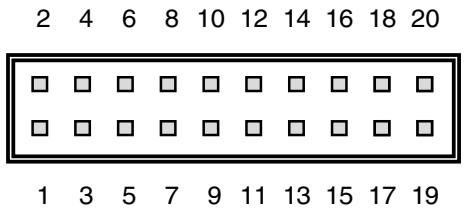


Table 15. MII/RMII connector CN3

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	RXD3	11	TXER	16	TXD0
2	+5 V	7	RXD0	12	RXER	17	TXD3
3	MDC	8	RXD1	13	TXEN	18	TXD2
4	MDIO	9	RXCLK	14	TXCLK	19	CRS
5	RXD2	10	RXDV	15	TXD1	20	COL

7.2.4 GPIO connector CN4

Figure 18. GPIO connector CN4

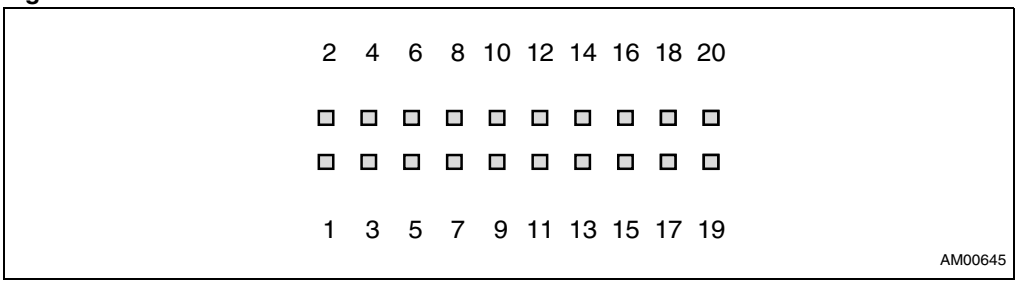


Table 16. GPIO connector CN4

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	PD3	11	PD4	16	PE0
2	+5 V	7	+3.3 V	12	PC12	17	PD7
3	PA6	8	PA15	13	PD5	18	PE1
4	PD2	9	GND	14	PC7	19	GND
5	PA5	10	PC10	15	PD6	20	+3.3 V

8 List of transformers and RJ45 connectors with embedded transformers with turn ratio 1.414:1

HALO Electronics, Inc.

www.haloelectronics.com

- HFJ11-2477E-L12RL (RJ45 with integrated transformer)
- TG110-S177N2RL (transformer)

Pulse

www.pulseeng.com

- J00-0086NL (RJ45 with integrated transformer)
- H1300NL (transformer)

EPCOS

www.epcos.com

- B78477P1001A314 (RJ45 with integrated transformer)

YUAN DEAN SCIENTIFIC CO., LTD.

www.yds.com.tw

- 49F-12171GYDXNL (RJ45 with integrated transformer)

Appendix A ST802RT1 TX mode Ethernet PHY demonstration board - BOM

Table 17. Bill of material ST802RT1 TX mode

Designator	Qty.	Description	Value	Order	Not assembled
B1	1	Push button (DT2112C)	RESET	GM Electronic®: 630-121 Farnell: 9471898	
C1, C2	2	Capacitor	10 nF	Farnell: 1709948	
C3, C4	2	Capacitor	12 pF	Farnell: 1462447	
C5, C6, C7, C9, C10, C11, C14, C15, C17, C18, C19	11	Capacitor	100 nF	Farnell: 4532004	C10, C17
C8, C12	2	Capacitor	1 µF / X5R Murata Manufacturing Co., Ltd. GRM188R60J105KA01	Murata: GRM188R60J105KA01 Farnell: 1710296	
C13, C16	2	Polarized capacitor	10 µF / tantalum	Farnell: 1213794	
D1	1	Schottky diode	STPS160A / STPS2L40U	STMicroelectronics™: STPS2L40U	
J1	1	Plug assembly, 40-pin connector	Connector 40	Tyco Electronics: 174218-2; Fujitsu: FCN-238P040-G/F	J1
J2, J8	2	1-pin header, 2 mm banana receptacle	2MM_REC		J2, J8
J3, J4, J5, J6, J7	5	1-pin header	GND	Farnell: 1593411	
J9	1	RJ45 Ethernet connector with integrated magnetic	RJ-45	Pulse: J00-0086NL	
JP1, JP4, JP5, JP6, JP7, JP19, JP20	7	2-pin jumper wire	Jumper	Farnell: 1593411	
JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18	11	3-pin jumper wire	Jumper3	Farnell: 1593412	
L1, L2	2	Ferrite bead	NFE31PT222Z1E9L Murata	Farnell: 9528172	
LED1, LED2	2	LED	Yellow	Farnell: 1226420	
LED3, LED4, LED8	3	LED	Red	Farnell: 1226392	
LED5, LED6	2	LED	Green	Farnell: 1226373	

Table 17. Bill of material ST802RT1 TX mode (continued)

Designator	Qty.	Description	Value	Order	Not assembled
P1	1	Header, 20-pin, dual row	Header 10 x 2	Farnell: 1593446	
R1	1	Resistor	5.6 KΩ	Farnell: 1514773	
R2	1	Resistor	91 KΩ	Farnell: 1646361	
R3, R4	2	Resistor	10 KΩ	Farnell: 1601277	
R5	1	Resistor	1 MΩ NA	Farnell: 1631320	R5
R6, R8	2	Resistor	750 Ω	Farnell: 1399909	R6, R8
R7, R9	2	Resistor	1.2 KΩ	Farnell: 1632396	
R17, R18, R19, R20, R21, R22, R23, R24	8	Resistor	2. 2 KΩ	Farnell: 1632417	
R25	1	Resistor	330 Ω	Farnell: 1646224	
R26, R28, R30	3	Resistor	2 KΩ	Farnell: 1632414	
R27, R32	2	Resistor	470 Ω	Farnell: 9367659	
R29	1	Resistor	220 Ω	Farnell: 1646159	
R31, R33, R34, R35	4	Resistor	75 Ω	Farnell: 9331549	R31, R33, R34, R35
SB1, SB2, SB3, SB4, SB5, SB6, SB7, SB8, SB9, SB10	10	Soldering bridge	Soldbridge		SB4, SB5
U1	1	10 / 100 Fast Ethernet 3.3 V transceiver	ST802RT1 TX mode	ST: ST802RT1 TX mode	
U2, U5	2	ESD protection, DALC208SC6	DVIULC6-2P6	ST: DVIULC6-2P6	
U3	1		LD1117S33	ST: LD1117S33	
U4	1	H1300 Ethernet transformer	H1300 (pulse)		
X1	1	Epson® Crystal: FA-238	25 MHz	Farnell: 1712818	

Appendix B STM32F107 controller demonstration board - BOM

Table 18. Bill of material STM32F107

Designator	Qty.	Description	Value	Order	Not assembled
C1, C2, C8	3	Polarized capacitor (surface mount)	10 µF / 6.3 V	Farnell: 1213794	
C3, C4	2	Capacitor	100 nF_0805	Farnell: 1414664	
C6, C17	2	Capacitor	100 nF_0603	Farnell: 4532004	
C5, C7, C9, C10, C11, C12, C13, C14	8	Capacitor	10 nF	Farnell: 1709948	
C15, C16	2	Capacitor	12 pF	Farnell: 1462447	
CN1	1	Molex® - 675031020 - socket, USB, MINI-B, SMT, W/PEGS	USB_1X90A	Farnell: 1125348	
CN2	1	Header, 20-pin, dual row, with key	JTAG	Farnell: 1099258	
CN3	1	Socket, 20-pin, dual row, side mounting	Socket 10x2, BL820GD	Farnell: 1593494 GME:832-009	
CN4	1	Socket, 20-pin, dual row, side mounting	Socket 10x2, BL820GD	Farnell: 1593494 GME: 832-009	
L1	1	Inductor, BLM18BA05OSN1D	BEAD	Farnell: 1515680	
LD1	1	Typical red, green, yellow, amber GaAs LED	Yellow	Farnell: 1226420	
LD2	1	Typical red, green, yellow, amber GaAs LED	Green	Farnell: 1226373	
LD3	1	Typical red, green, yellow, amber GaAs LED	Red	Farnell: 1226392	
R1	1	Resistor	1. 5 kΩ_0603	Farnell: 1632406	
R2, R4	2	Resistor	22 Ω_0603	Farnell: 1692521	
R3, R6, R7, R8, R9, R12	6	Resistor	10 kΩ_0603	Farnell: 1601277	
R5	1	Resistor	1 MΩ_0603	Farnell: 1631320	R5
R10	1	Resistor	47 Ω_0603	Farnell: 1646283	
R11	1	Resistor	0 Ω_0603	Farnell: 1573911	
R13	1	Resistor	330 Ω	Farnell: 1646224	

Table 18. Bill of material STM32F107 (continued)

Designator	Qty.	Description	Value	Order	Not assembled
R15	1	Resistor	470 Ω	Farnell: 9367659	
R14	1	Resistor	220 Ω	Farnell: 1646159	
RESET1	1	Switch	Reset	GME: 630-121 Farnell: 9471898	
RESET2	1	Switch	B1	GME: 630-121 Farnell: 9471898	
U2	1	MCU	STM32F107_256K	ST: STM32F107	
U3	1	Low drop voltage regulator	LD1117S33	ST: LD1117S33	
X1	1	Epson Crystal: FA-238	25 MHz	Farnell: 1712818	
SB1, SB2, SB3, SB4	4	Solder bridge			SB1, SB2

Appendix C ST802RT1 TX mode Ethernet PHY demonstration board - schematic

Figure 19. ST802RT1 TX mode Ethernet PHY demonstration board - schematic - part 1

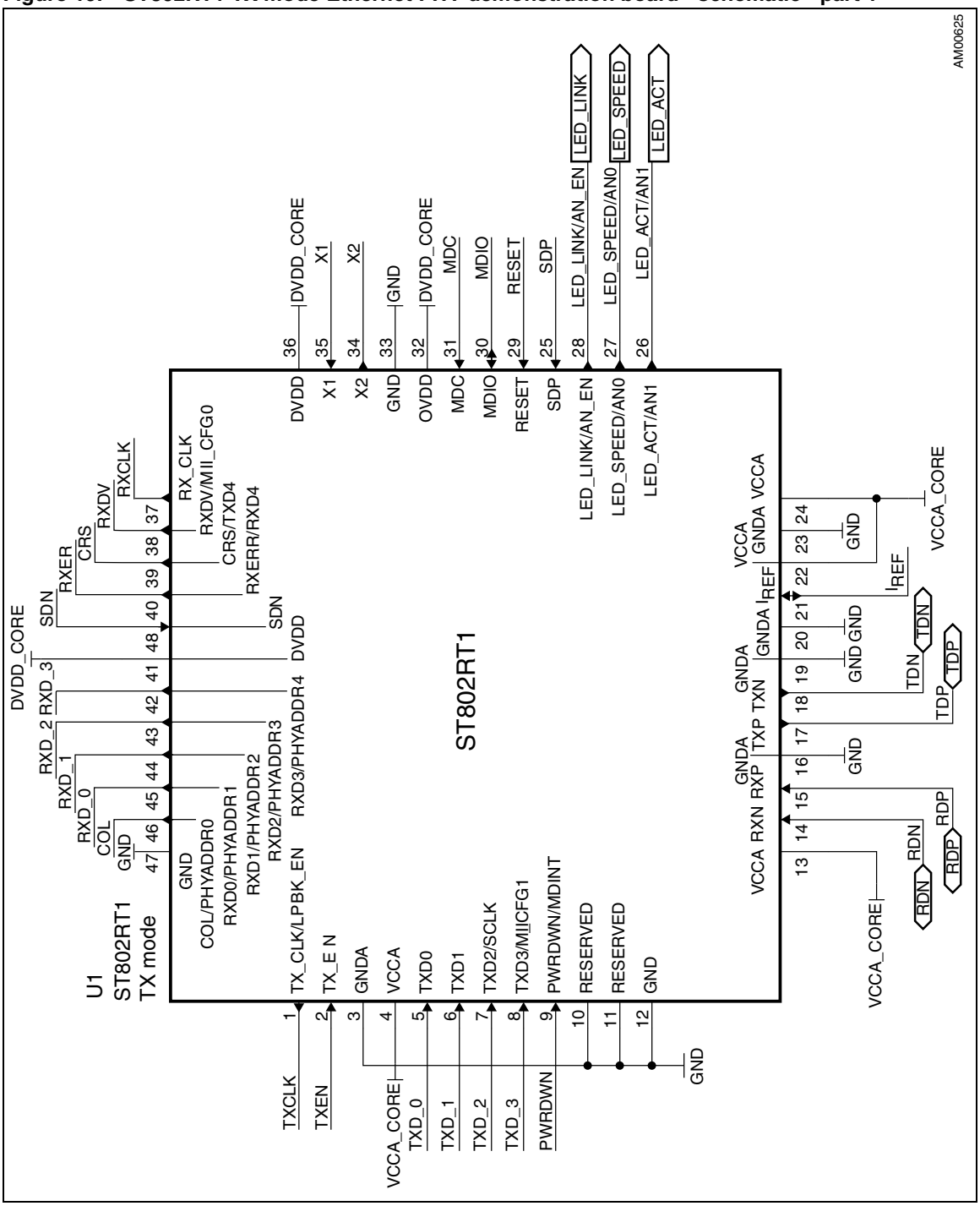


Figure 20. ST802RT1 TX mode Ethernet PHY demonstration board - schematic - part 2

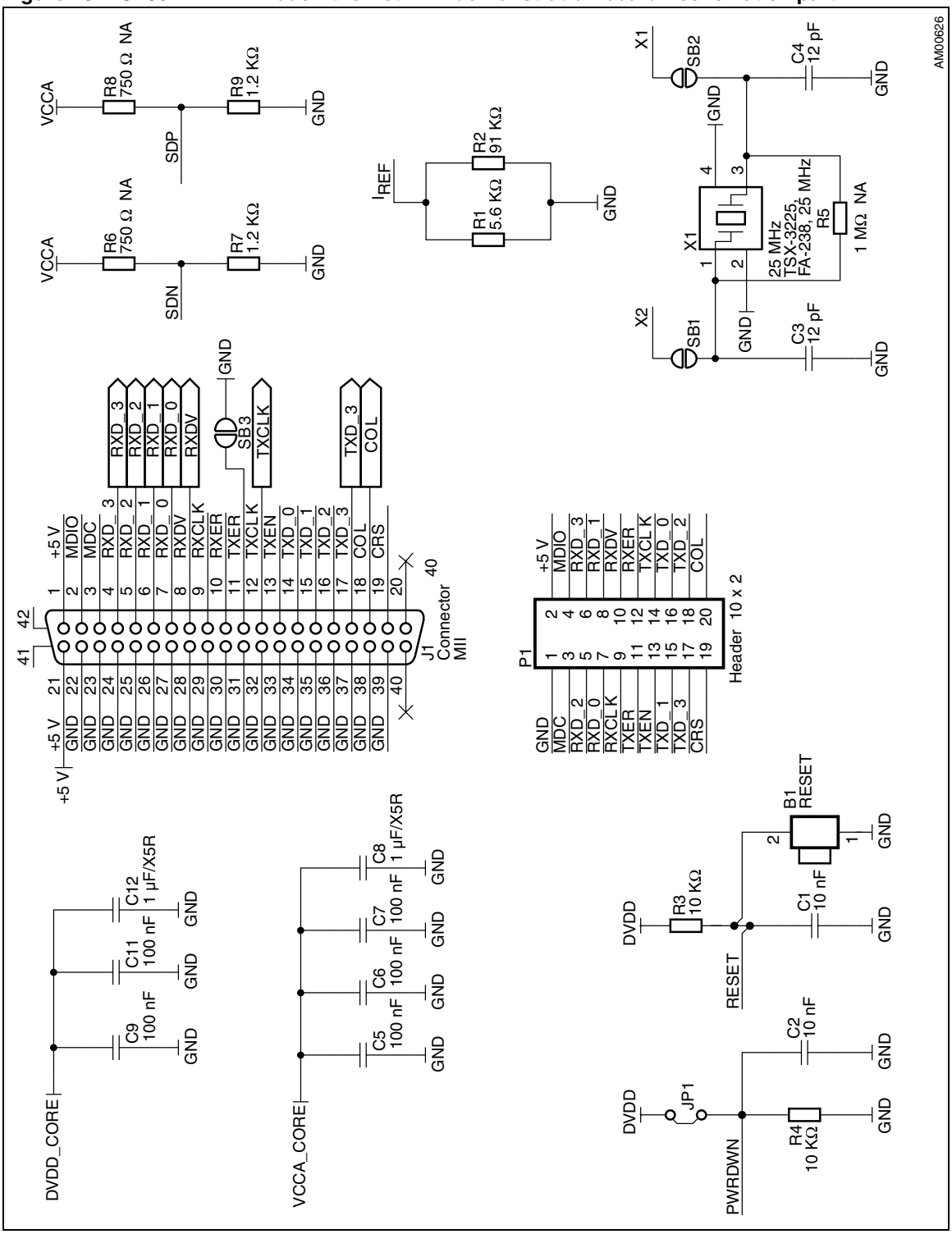


Figure 21. ST802RT1 TX mode Ethernet PHY demonstration board - schematic - part 3

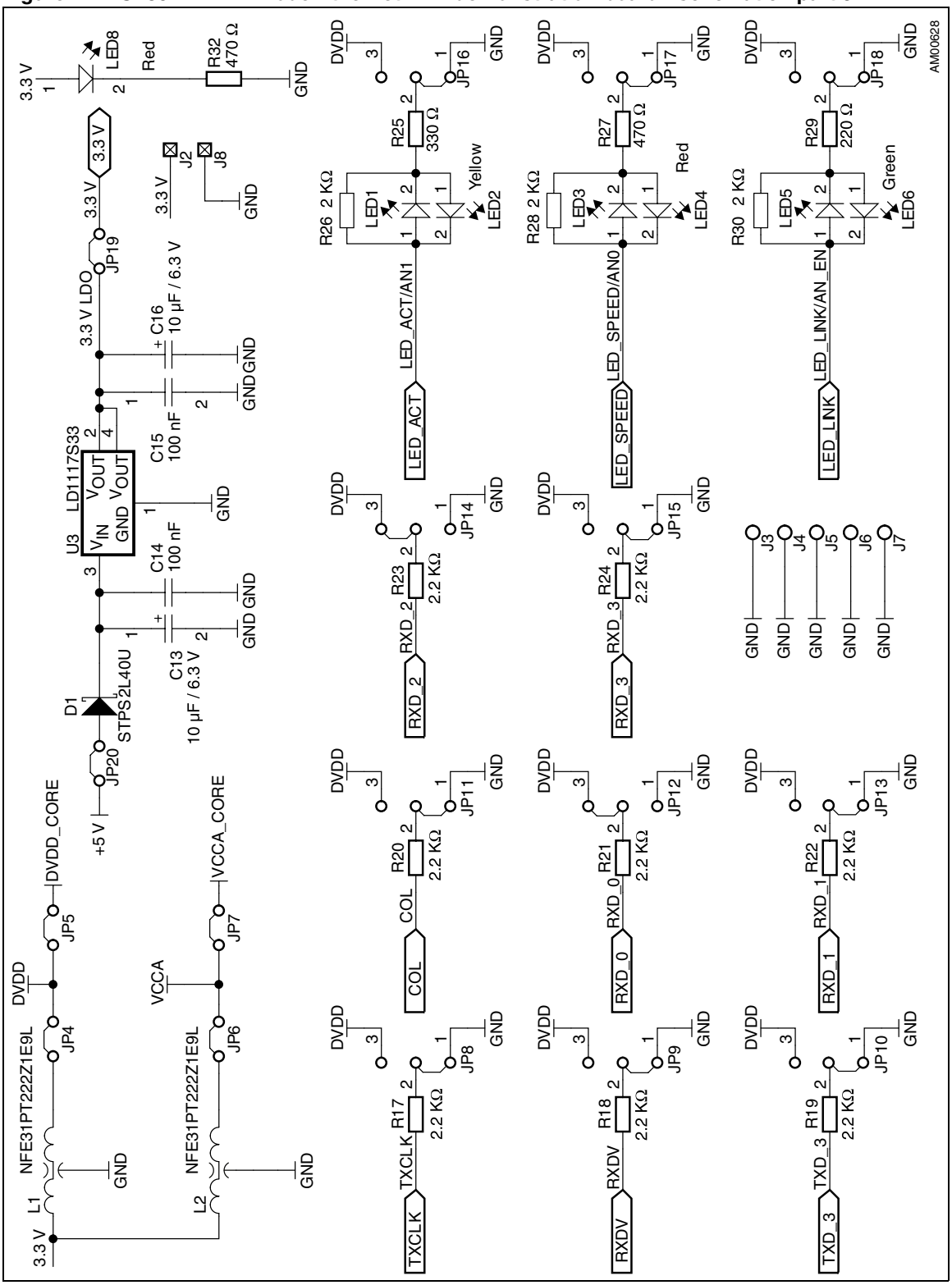
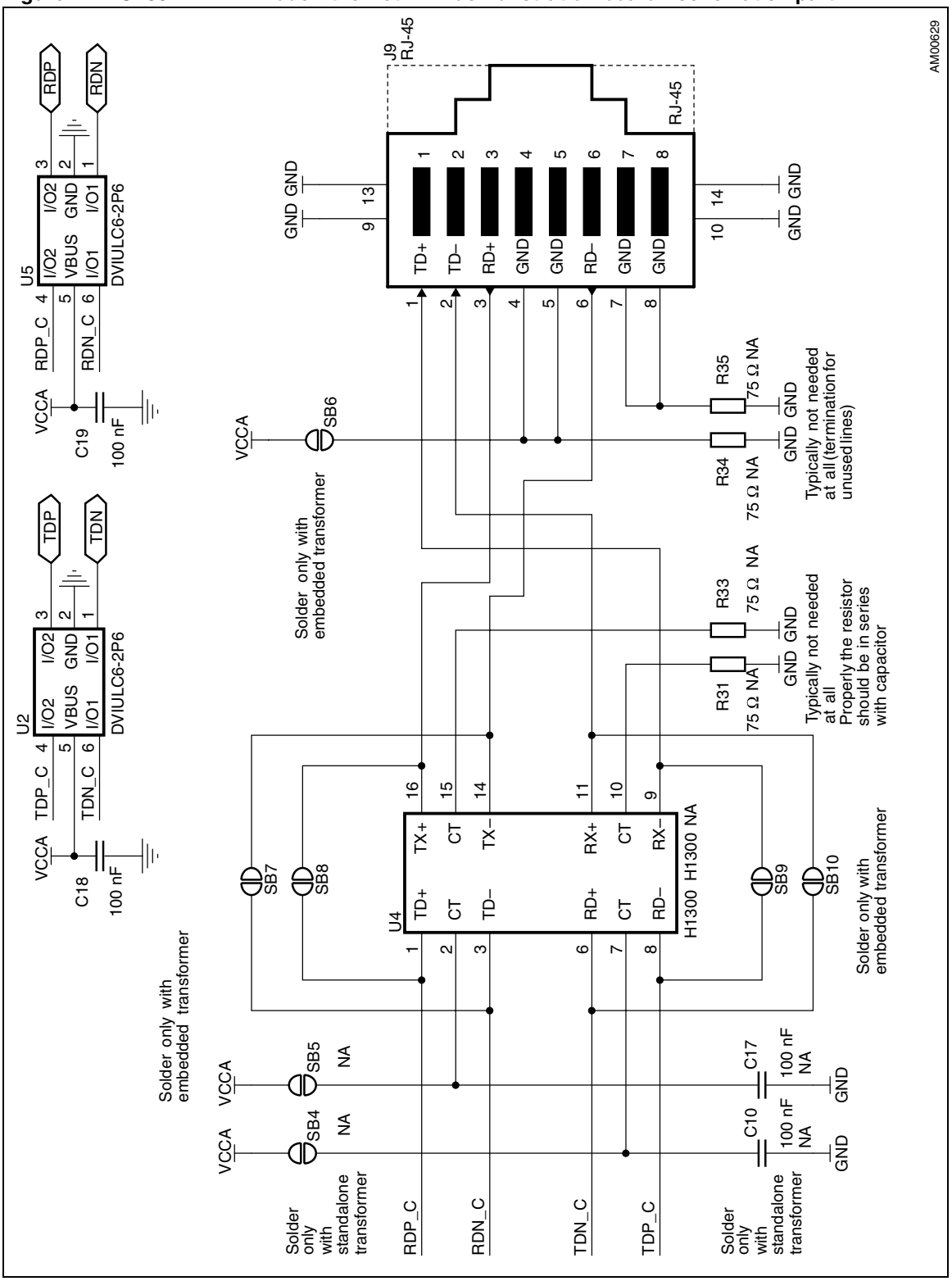


Figure 22. ST802RT1 TX mode Ethernet PHY demonstration board - schematic - part 4



Appendix D STM32F107 controller demonstration board - schematic

Figure 23. STM32F107 controller demonstration board - schematic - part 1

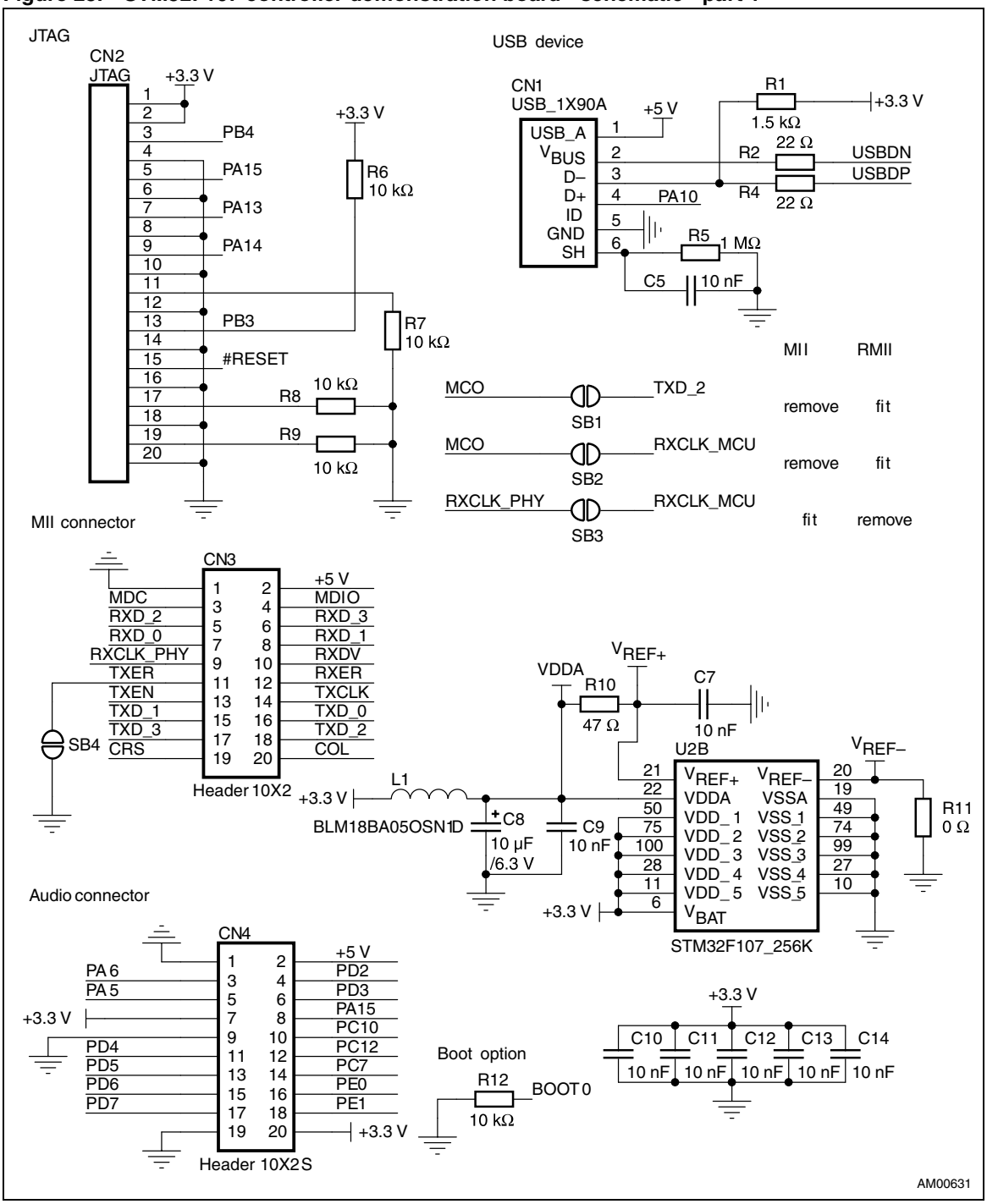
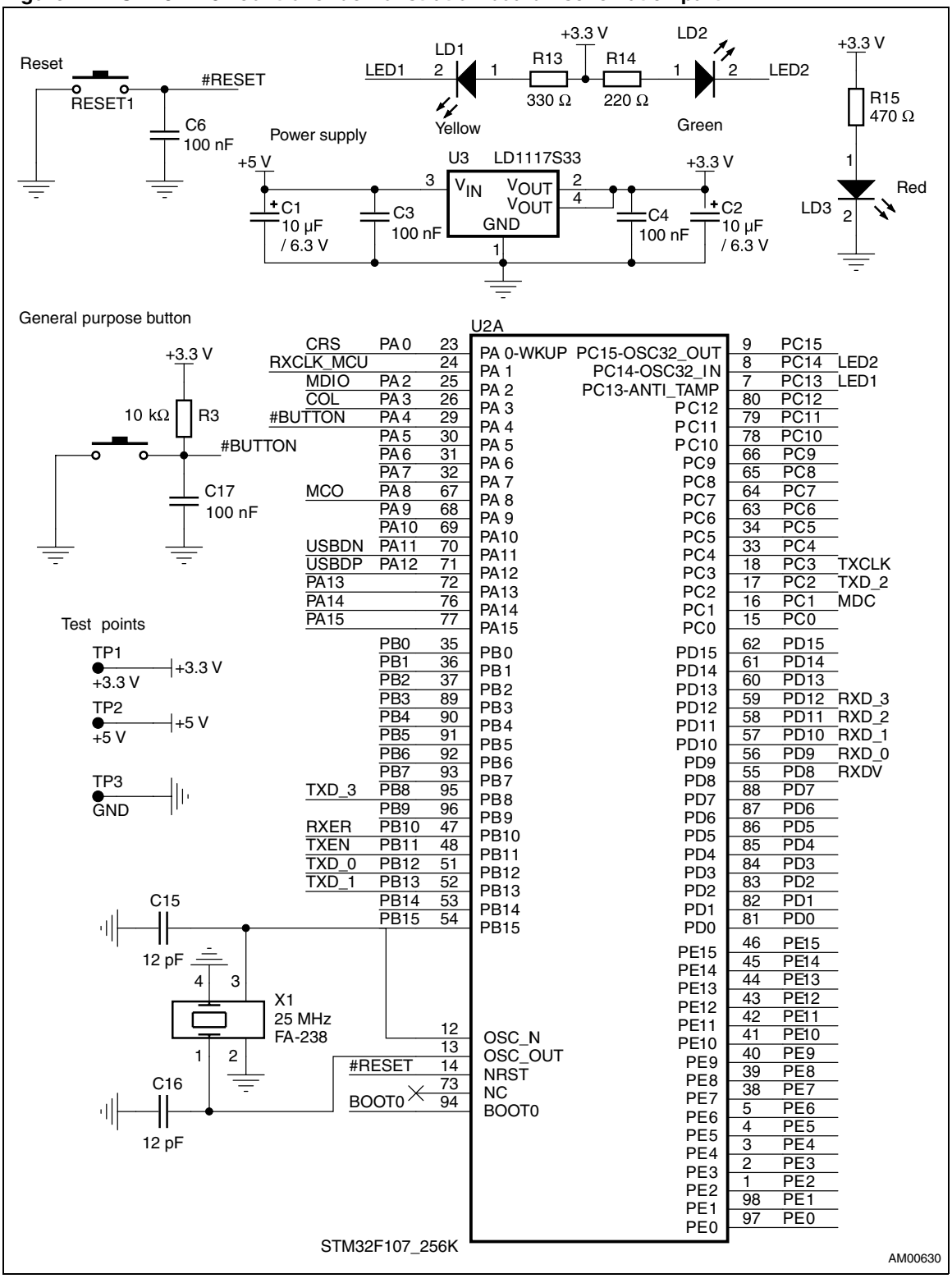


Figure 24. STM32F107 controller demonstration board - schematic - part 2



Revision history

Table 19. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release.
07-May-2010	2	Added *Section 8*.

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