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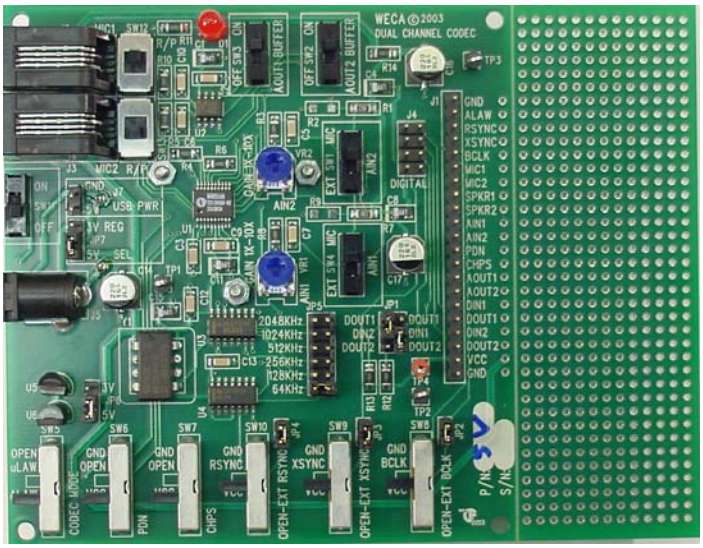
Winbond W682x10
Dual Channel CODEC
Evaluation System User Guide



W682x10DK Evaluation Board Rev 1.06

1 Overview

1.1 Introduction

The dual channel W682310 and W682510 (hereafter referred to as W682x10) are members of the W68XXXX family of PCM CODECs. The dual voice band CODEC complies with the ITU-T G.712 industry telecom specifications. The W682x10 also includes a complete μ-Law and A-Law compander. The μ-Law and A-Law companders comply with the ITU-T G.711 specifications. The board supports 64 kHz, 128 kHz, 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz clock rates.

1.2 General Description

Winbond's W682x10DK Evaluation/Development System is a Stand-alone unit that serves as an easy-to-use demonstration board as well as a powerful evaluation system. All the functions of the W682x10 PCM CODEC are selectable in real time to allow complete evaluation of this IC for an end application. The board includes connectors allowing easy connection to external hardware for use as a development tool.

1.3 W682x10DK Features

- Easy to use (a stand-alone evaluation system)
- Single 9 VDC power supply
- Prototype area for application development
- Header with all digital and analog signals on the chip brought out for access
- Additional connector with the digital signals for easy data extraction
- Two RJ9 handset jacks
- Switch between μ-Law and A-Law
- Switch between serial and parallel mode
- Simple interfacing to external hardware
- Headers for interconnecting digital signals
- Switches to select handset microphone polarity

1.4 Reference Documents

Please refer to the W682310 and W682510 data sheets for detailed specifications of our dual channel CODECs at www.winbond-usa.com/products/codecs/

1.5 Pin name cross reference

The W682x10 CODECS are Oki compatible, this table is a pin name cross reference.

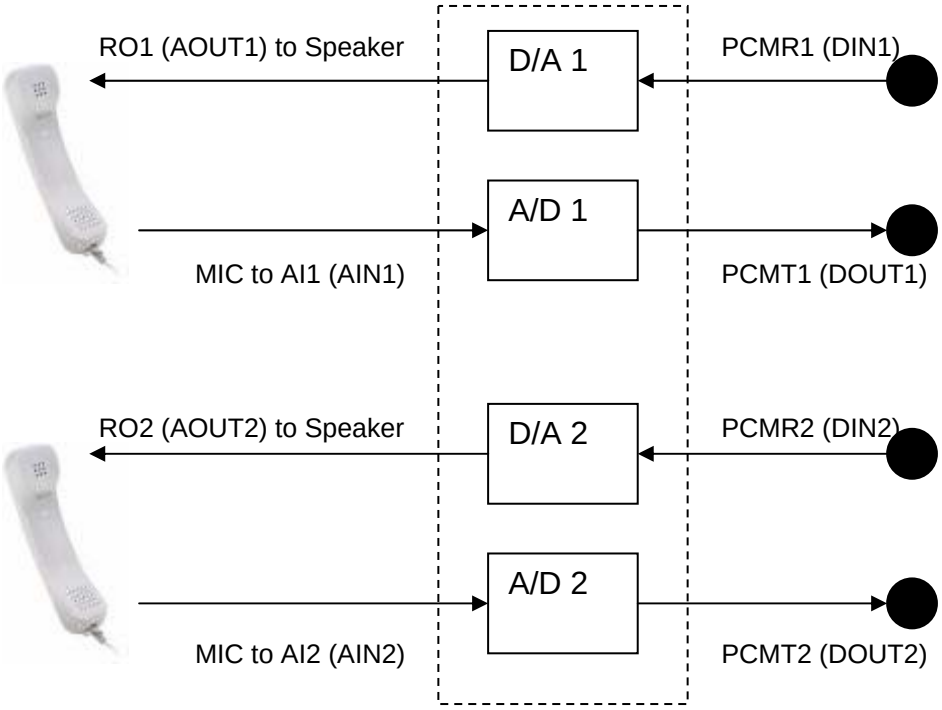
Pin nr	Winbond	Oki
1	VREF	SGC
2	RO2	AOUT2
3	RO1	AOUT1
4	PUI	PDN
5	PCMMS	CHPS
6	VDD	VDD
7	VSSD	DG
8	FSR	RSYNC
9	PCMR2	DIN2
10	PCMR1	DIN1

Pin nr	Winbond	Oki
11	AI2	AIN2
12	AO2-	GSX2
13	AO1-	GSX1
14	AI1	AIN1
15	U/A LAW	ALAW
16	VSSA	AG
17	BCLK	BCLK
18	FST	XSYNC
19	PCMT2	DOUT2
20	PCMT1	DOUT1

2 Hardware

2.1 CODEC block description

The W682x10 CODEC is a dual channel CODEC that consists of two A/D converters (AI1-2) and two D/A converters (RO1-2) as shown below.



2.2 Parallel and Serial mode operation

The W682x10 allows two types of data interfaces, parallel or serial. Parallel mode uses A/D 1 and A/D 2 to convert analog data to two separate digital bit streams on PCMT1 and PCMT2 respectively. D/A1 and D/A2 convert incoming digital data from PCMR1 and PCMR2 for analog output to RO1 and RO2. This mode interfaces easily to circuits that require two separate PCM interfaces.

Serial mode takes the input from AI1 and AI2 and multiplexes the output on PCMT1. The first 8 bits are channel 1 and the second set of 8 bits are channel 2. The digital signal coming in on PCMR2 is time division multiplexed and the two channels split to RO1 and RO2 respectively. This mode works well with single PCM interface systems such as PBX multiplexers.

To set up the handsets to communicate over parallel and serial mode, connect the digital channels as follows:

Parallel mode (In same time slot)

- Set SW7 to VCC position to set CHPS to VCC
- Connect DIN1 to DOUT2 (PCMR1 to PCMT2)
- Connect DIN2 to DOUT1 (PCMR2 to PCMT1)

Serial mode (Not in same time slot)

- Set SW7 to GND position to set CHPS to GND
- Connect DIN2 to DOUT1 (PCMR2 to PCMT1)
- Leave other digital pins unconnected

2.3 Power

There are three ways of supplying power to the board:

- 9 V battery
- 9 VDC at 500 mA power supply
- Header J7 for 5 VDC (in USB application)

The jumper JP6 selects whether a 5V or 3V regulator is used. Connecting J13 to a 5 VDC supply drives the circuits on the board directly or through the 3V regulator selected by jumper JP7.
Do not change these jumpers, as they have been set according to the CODEC device on the board.

2.4 Bit Clock and Frame Sync

A 2.048 MHz TTL oscillator generates the allowable bit clock frequencies from 64 kHz up to 2.048 MHz. The bit clock is selectable through jumper JP5. The Frame Sync signal is 8 kHz with a 50% duty cycle.

2.5 Analog Audio Circuits

The CODEC supports variable input gain (<10X). This gain can be manually set for each channel with variable resistors VR1 (channel 1) and VR2 (channel2). The CODEC itself does not support handset operation so analog circuits for microphone bias (no AGC) are required. A unity gain output amplifier drives the handset speakers.
For optimal sound quality, adjust VR1 and VR2 individually to provide approximately 2.4 Vp-p (W6825010) or 1.0 Vp-p (W682310) at the AI1 and AI2 pins from the source. The source can be either a microphone or an external input

2.6 Prototyping Area

All CODEC I/O pins are connected to the prototyping area for easy connection of additional hardware. The switches and jumpers that disconnect the signals generated on the CODEC board will simplify connection of external circuits.

2.7 Telephone handset microphone setup

Two switches (SW12 and SW13) toggle between the two common types of handsets available. Switching will reverse the polarity of the microphone connectors. If two handsets are used and the handsets are not transmitting audio, try the other position of the switches to ensure the correct microphone polarity is used.

2.8 Default switch and jumper settings

The default settings in the following table will enable operation of the board in parallel PCM mode, a-Law and two handsets communicating with each other using the on board clock generator

2.8.1 Signal Switches

Switch	*Description*	*Default Setting*
SW1	Connect/disconnect channel 2 handset and MIC bias circuit	MIC
SW2	Connect/disconnect channel 2 analog output buffer	ON
SW3	Connect/disconnect channel 1 analog output buffer	ON
SW4	Connect/disconnect channel 1 handset and MIC bias circuit	MIC
SW5	Set ALAW pin to GND, VCC or external control	ALAW
SW6	Set PDN pin to GND, VCC or external control	VCC
SW7	Set CHPS pin to GND, VCC or external control	VCC
SW8	Set BCLK to GND, VCC or on board bit clock (remove JP2 for external control)	BCLK
SW9	Set XSYNC to GND, VCC or on board frame sync (remove JP3 for external control)	XSYNC
SW10	Set RSYNC to GND, VCC or on board frame sync (remove JP4 for external control)	RSYNC
SW11	Power switch	ON
SW12	MIC1 Handset microphone line switch	
SW13	MIC2 Handset microphone line switch	

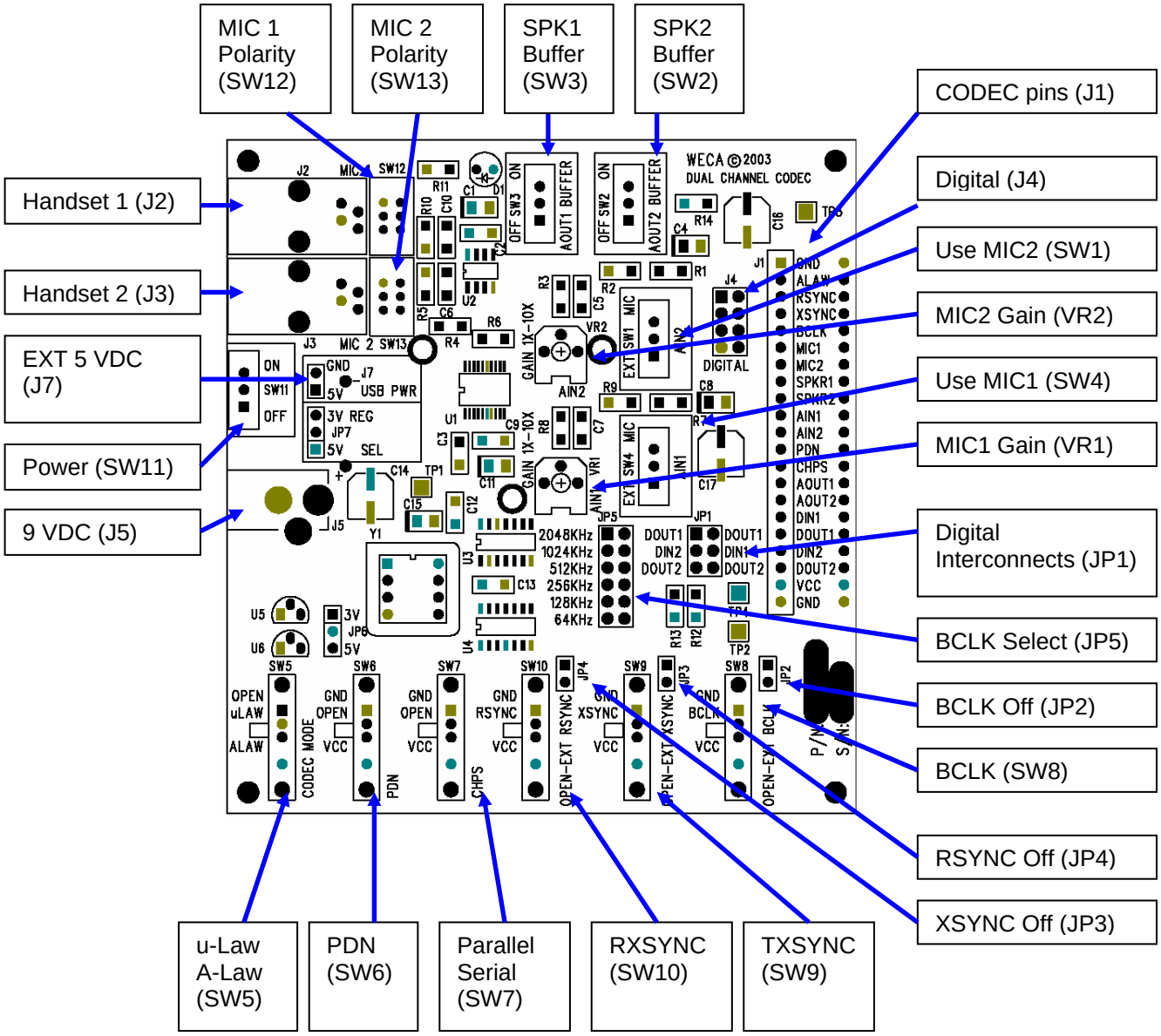
2.8.2 Jumpers

2.8.2.1.1.1 Jumper	*Description*	*Default Setting*
JP1	Connect digital inputs and outputs as desired	DOUT1 to DIN2, (PCMT1 to PCMR2) DOUT2 to DIN1 (PCMT2 to PCMR1)
JP2	Disable on board bit clock when removed	Installed
JP3	Disable on board TXSYNC when removed	Installed
JP4	Disable on board RXSYNC when removed	Installed
JP5	Bit Clock Select - selects the Bit Clock frequencies from 2.048MHz to 64KHz	64kHz
JP6	3V or 5V operation	
JP7	External 5V power generates 5V or 3V	

2.8.3 Connectors

2.8.3.1.1.1 Connector	*Description*
J1	Header providing access to all CODEC signals
J2	Handset connected to analog input and output channel 1
J3	Handset connected to analog input and output channel 2
J4	Digital CODEC signals for external interfacing
J5	9 VDC power supply input
J6	9 V Battery
J7	Header for external 5V input (USB)

2.8.4 Location of switches, jumpers and connectors



3 Operating Modes

The two handsets can be connected using either parallel or serial modes for simple verification of digital multiplexing modes. SW6 sets the mode and the jumper on J3 selects the digital signals to interconnect.

3.1 Two handsets in parallel PCM mode (same time slot)

- Set SW2 and SW3 in the 'ON' position. This enables the analog output buffer.
- Set SW6 in the 'VCC' position to take the chip out of standby.
- Set SW7 in the 'VCC' position to select parallel mode.
- Set SW8, SW9 and SW10 in the BCLK, XSYNC and RSYNC positions.
- Set SW1 and SW4 in the 'MIC' position to enable the handset microphone.
- Set the JP1 jumpers to connect DIN1 to DOUT2 and DIN2 to DOUT1.

3.2 Two handsets in serial PCM mode (adjacent time slot)

- Set SW2 and SW3 in the 'ON' position. This enables the analog output buffer.
- Set SW6 in the 'VCC' position to take the chip out of standby.
- Set SW7 in the 'GND' position to select serial mode.
- Set SW8, SW9 and SW10 in the BCLK, XSYNC and RSYNC positions.
- Set SW1 and SW4 in the 'MIC' position to enable the handset microphone.
- Set the JP1 jumpers to connect DIN1 to DOUT2 and DIN2 to DOUT1.

Note: this mode provides sidetone in the handset and no handset to handset communication

3.3 Using external bit clock and frame sync

- Set SW6 in the 'VCC' position to take the chip out of standby.
- Set SW7 to select parallel or serial mode as desired.
- Set JP1 jumpers as appropriate.
- Disconnect JP2, JP3 and JP4. This disconnects the on board clock generator from the CODEC.
- Connect the external clock to header pins BCLK, RSYNC and XSYNC respectively.

3.4 Using external analog audio generator

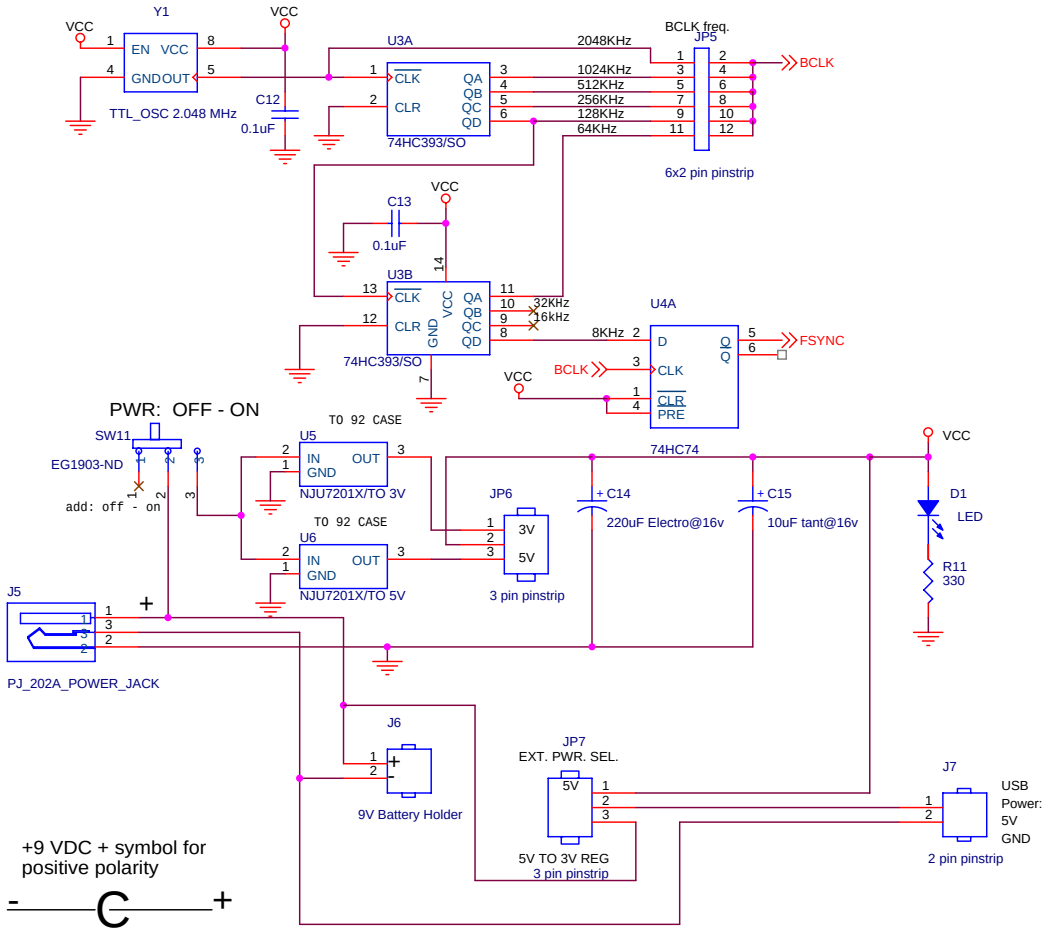
- Set SW6 in the 'VCC' position to take the chip out of standby.
- Set SW7 to select parallel or serial mode as desired.
- Set JP1 jumpers as appropriate.
- Set SW8, SW9 and SW10 in the BCLK, XSYNC and RSYNC positions.
- Set SW1 and SW4 in the 'EXT' position to disable the handset microphone.
- (Optional) Set SW2 and SW3 in the 'ON' position. This enables the analog output buffer.
- Connect AI1 and AI2 on header J1 and connect the ground reference to AGND.

3.5 Digital Audio connector

To allow easy connection of external digital audio capturing and processing, a header has been dedicated to all digital pins and the clock signals. Enable or disable the internal clocks as required and ensure the JP1 jumpers are not interfering with the external digital interface.

4 Schematics

4.1 Clock and power circuits



4.2 CODEC and analog circuits