AN3065
Application note

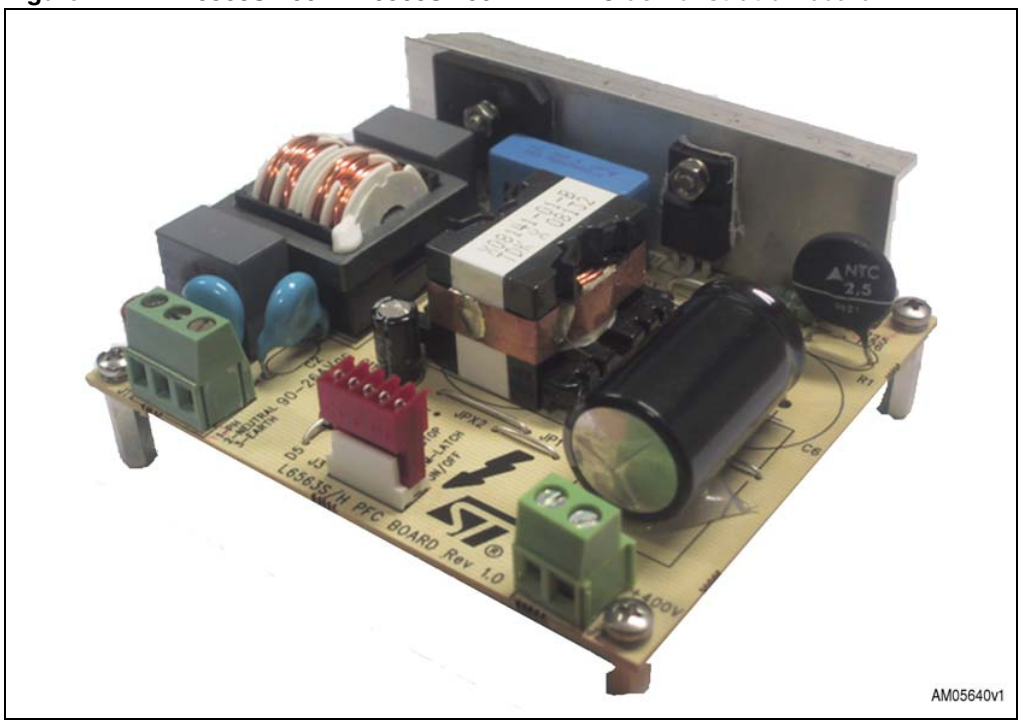
100 W transition-mode PFC pre-regulator with the L6563S

Introduction

This application note describes a demonstration board based on the transition-mode PFC controller L6563S and presents the results of its bench demonstration. The board implements a 100 W, wide-range mains input, PFC pre-conditioner suitable for ballast, adapters, flatscreen displays, and all SMPS having to meet the IEC61000-3-2 or the JEITA-MITI regulation.

The L6563S is a current-mode PFC controller operating in transition mode (TM) and implementing an internal high-voltage startup circuitry.

Figure 1. EVL6563S-100W: L6563S 100W TM PFC demonstration board



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1 Main characteristics and circuit description

The main characteristics of the SMPS are listed below:

- Line voltage range: 90 to 265 Vac
- Minimum line frequency (f_L): 47 Hz
- Regulated output voltage: 400 V
- Rated output power: 100 W
- Maximum $2f_L$ output voltage ripple: 20 V pk-pk
- Hold-up time: 10 ms (V_{DROP} after hold-up time: 300 V)
- Minimum switching frequency: 40 kHz
- Minimum estimated efficiency: 92% (at Vin = 90 Vac, Pout = 100 W)
- Maximum ambient temperature: 50 °C
- PCB type and size: single side, 35 µm, CEM-1, 90 x 83 mm

This demonstration board implements a power factor correction (PFC) pre-regulator,100 W continuous power, on a regulated 400 V rail from a wide-range mains voltage and provides for the reduction of the mains harmonics, allowing to meet the European EN61000-3-2 or the Japanese JEITA-MITI standard. The regulated output voltage is typically the input for the cascaded isolated DC-DC converter that provides the output rails required by the load.

The board is designed to allow full-load operation in still air.

The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D1. It is completed by the coil L2, the diode D3 and the capacitor C6. The boost switch is represented by the power MOSFET Q1. The NTC R1 limits the inrush current at switch-on. It has been connected on the DC rail, in series to the output electrolytic capacitor, in order to improve the efficiency during low line operation because the RMS current flowing into the output stage is lower than current flowing into the input one at the same input voltage, thus increasing efficiency. The board is equipped with an input EMI filter necessary to filter the commutation noise coming from the boost stage.

At startup the L6563S is powered by the capacitor C11 that is charged via the resistors R7 and R16. Then the L2 secondary winding and the charge pump circuit (C7, R4, D4 and D5) generate the Vcc voltage powering the L6563S during normal operation. The L2 secondary winding is also connected to the L6563S pin #11 (ZCD) through the resistor R5. Its purpose is supply the information that L2 has demagnetized, needed by the internal logic for triggering a new switching cycle.

The divider R9, R12, R17 and R19 provides the L6563S multiplier with the information of the instantaneous mains voltage that is used to modulate the peak current of the boost.

The resistors R2, R8, R10 with R13 and R14 are dedicated to sense the output voltage and feed back to the L6563S the information necessary to regulate the output voltage. The components C9, R18 and C8 constitute the error amplifier compensation network necessary to keep the required loop stability.

The peak current is sensed by resistors R25 and R26 in series to the MOSFET and signal is fed into pin #4 (CS) of the L6563S via the filter composed of R24 and C15.

C13, R27 and R32 connected to pin #5 (V_{FF}) complete an internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage signal at this pin, a DC level equal to the peak voltage on pin #3 (MULT), is fed to a second input to the multiplier for the

$1/V^2$ function necessary to compensate the control loop gain dependence on the mains voltage. Additionally, pin #10 (RUN) is connected to pin# 5 (V_{FF}) through a resistor divider R27 and R32, providing a voltage threshold for brownout protection (AC mains undervoltage). A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The L6563S restarts as the voltage at the pin rises above 0.88 V.

The divider R3, R6, R11 and R15 provides the L6563S pin #7 (PFC_OK) with the information regarding the output voltage level. It is required by the L6563S output voltage monitoring and disables functions used for PFC protection purposes.

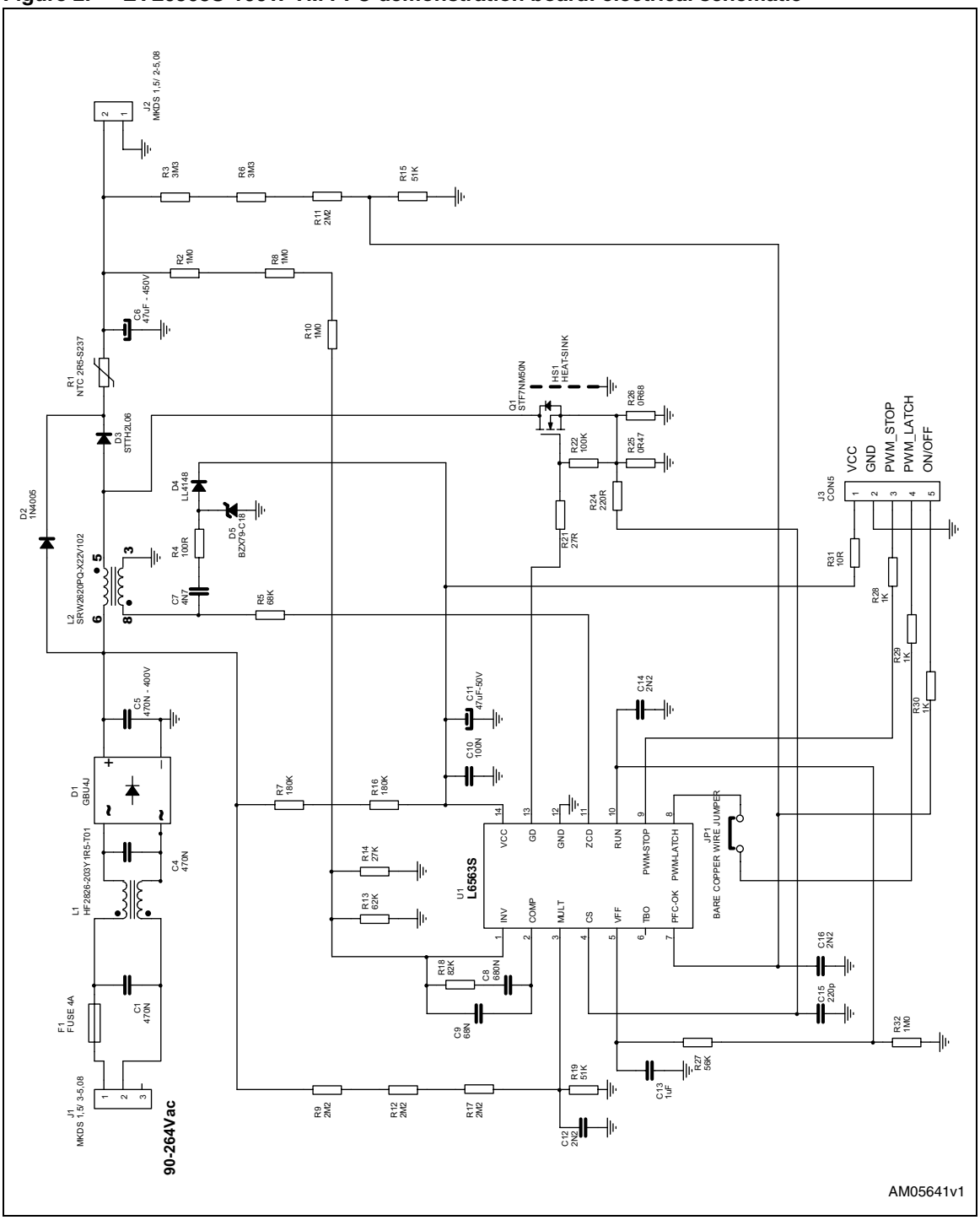
If the voltage on pin #7 exceeds 2.5 V, the IC stops switching and restarts as the voltage on the pin falls below 2.4 V implementing the so-called dynamic OVP, which prevents an excessive output voltage in case of transients, because of the slow response of the error amplifier. However, if contemporaneously the voltage of the INV pin falls below 1.66 V (typ.), a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling Vcc, bringing its value lower than 6 V before rising up to the turn-on threshold.

Additionally If the voltage on pin #7 (PFC_OK) is tied below 0.23 V, the L6563S is shut down. To restart operation of the L6563S the voltage on pin #7 (PFC_OK) has to increase above 0.27 V. This function can be used as a remote on/off control input.

To allow interfacing of the board with a D2D converter, the connector J3 allows powering the L6563S with an external Vcc and also manages failure or abnormal conditions via the pins PWM_LATCH and PWM_STOP. The L6563S can be also disabled or enabled to manage properly light load or failure by the D2D via the PFC_OK pin (#7), available at pin #5 of J3 (ON/OFF). For further details please see *Section 4.7*.

2 Electrical diagram

Figure 2. EVL6563S-100W TM PFC demonstration board: electrical schematic



3 Bill of material

Table 1. EVL6563S-100W TM PFC demonstration board bill of material

Des.	Part type/part value	Case/package	Description	Supplier
C1	470N	DWG	X2 - FLM CAP - R46-I 3470--M1-	ARCOTRONICS
C4	470N	DWG	X2 - FLM CAP - R46-I 3470--M1-	ARCOTRONICS
C2	2N2	DWG	Y1 - SAFETY CAP. DE1E3KX222M	muRata
C3	2N2	DWG	Y1 - SAFETY CAP. DE1E3KX222M	muRata
C5	470N - 400 V	DWG	400V - FLM CAP - B32653A4474	EPCOS
C6	47 µF - 450 V	Dia. 18 x 31.5 mm	450 V - ALUMINIUM ELCAP - ED SERIES - 105°C	NIPPON-CHEMICON
C7	4N7	1206	100 V CERCAP - general purpose	AVX
C8	680N	1206	25 V CERCAP - general purpose	AVX
C9	68N	0805	50 V CERCAP - general purpose	AVX
C10	100N	1206	50 V CERCAP - general purpose	AVX
C11	47 µF-50 V	Dia. 5 x 10 mm	50 V - aluminium ELCAP - YXF series - 105°C	Rubycon
C12	2N2	1206	50 V CERCAP - general purpose	AVX
C16	2N2	1206	50 V CERCAP - general purpose	AVX
C13	1 µF	0805	25 V CERCAP - general purpose	AVX
C14	2N2	0805	50 V CERCAP - general purpose	AVX
C15	220 pF	0805	50 V CERCAP - general purpose	AVX
D1	GBU4J	STYLE GBU	Single phase bridge rectifier	VISHAY
D2	1N4005	DO - 41	Rectifier - general purpose	VISHAY
D3	STTH2L06	DO - 41	Ultrafast high-voltage rectifier	STMicroelectronics
D4	LL4148	MINIMELF	High-speed signal diode	VISHAY
D5	BZX79-C18	DO - 35	Zener diode	VISHAY
D6	N.M.	MINIMELF	Not mounted	

Table 1. EVL6563S-100W TM PFC demonstration board bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
F1	FUSE 4 A	DWG	Fuse T4A - time delay	Wichmann
HS1	HEAT-SINK	DWG	Heatsink for D1& Q1	
JP1	WIRE JUMPER		Bare copper wire jumper	
JP2	N.M.		NOT MOUNTED	
J1	MKDS 1,5/ 3-5,08	DWG	PCB term. block, screw conn., pitch 5 mm - 3 W	PHOENIX CONTACT
J2	MKDS 1,5/ 2-5,08	DWG	PCB term. block, screw conn., pitch 5 mm - 2 W	PHOENIX CONTACT
J3	CON5		PCB term. block, pitch 2.5 mm - 5 W	MOLEX
L1	HF2826-203Y1R5-T01	DWG	Input EMI filter - 20 mH-1.5 A	TDK
L2	SRW2620PQ-X22V102	DWG	PFC inductor - 0.52 mH (X08141-01-B)	TDK
Q1	STF7NM50N	TO-220FP	N-Channel power MOSFET	STMicroelectronics
R1	NTC 2R5-S237	DWG	NTC RESISTOR P/N B57237S0259M000	EPCOS
R2	1M0	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R8	1M0	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R10	1M0	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R3	3M3	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R6	3M3	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R4	100 Ω	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R5	68 kΩ	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R7	180 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R16	180 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R9	2M2	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R11	2M2	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R12	2M2	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R17	2M2	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R13	62 kΩ	0805	SMD standard film RES - 1/8 W - 1% - 100 ppm/°C	VISHAY

Table 1. EVL6563S-100W TM PFC demonstration board bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
R14	27 kΩ	0805	SMD standard film RES - 1/8 W - 1% - 100 ppm/°C	VISHAY
R15	51 kΩ	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R18	82 kΩ	0805	SMD standard film RES - 1/8 W - 5% - 250 ppm/°C	VISHAY
R19	51 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R20	N.M.	0805	Not mounted	
R21	27 Ω	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R22	100 kΩ	0805	SMD standard film res - 1/8 W - 5% - 250 ppm/°C	VISHAY
R23	N.M.	0805		VISHAY
R24	220 Ω	PTH	SFR25 axial stand. film RES - 0.4W - 5% - 250 ppm/°C	VISHAY
R25	0.47 Ω	PTH	SFR25 axial stand. film RES - 0.4W - 5% - 250 ppm/°C	VISHAY
R26	0.68 Ω	PTH	SFR25 axial stand. film RES - 0.4 W - 5% - 250 ppm/°C	VISHAY
R27	56 kΩ	1206	SMD standard film RES - 1/4 W - 1% - 100 ppm/°C	VISHAY
R28	1 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R29	1 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R30	1 kΩ	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R31	10 Ω	1206	SMD standard film RES - 1/4 W - 5% - 250 ppm/°C	VISHAY
R32	1M0	0805	SMD standard film RES - 1/8 W - 1% - 250 ppm/°C	VISHAY
U1	L6563S	SO-14	Enhanced transition-mode PFC controller	STMicroelectronics

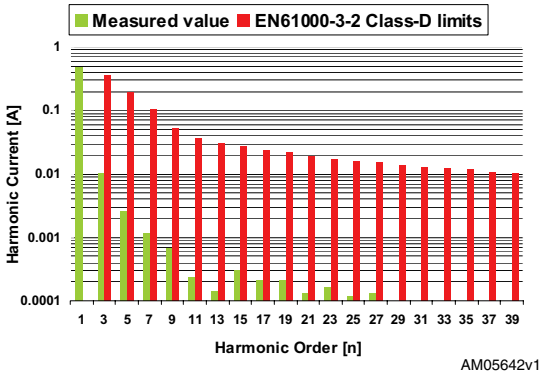
4 Test results and significant waveforms

4.1 Harmonic content measurement

One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D, at full load at both the nominal input voltage mains.

The circuit is able to reduce the harmonics well below the limits of both regulations from full load down (measurements are shown in *Figure 3* and *4*) to light load. Please note that all measures and waveforms have been done using a Pi-filter for filtering the noise coming from the circuit, using a 20 mH common-mode choke and two 470NF-X2 filter capacitors.

Figure 3. EVL6563S-100W TM PFC: compliance to EN61000-3-2 standard



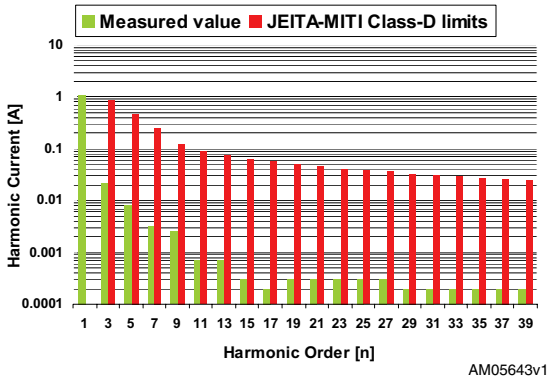
Vin = 230 Vac - 50 Hz

Pout = 100 W

THD = 2.31 %

PF = 0.982

Figure 4. EVL6563S-100W TM PFC: compliance to JEITA-MITI standard



Vin = 100 Vac - 50 Hz

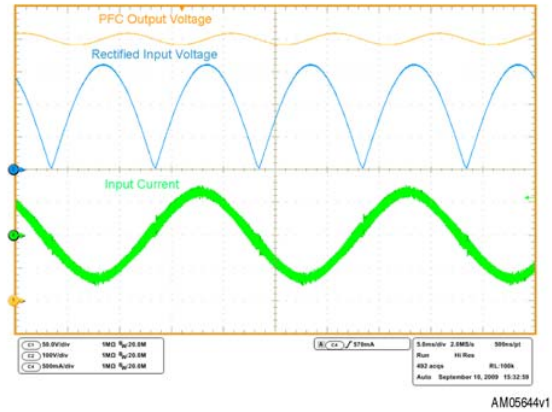
Pout = 100 W

THD = 2.30 %

PF = 0.999

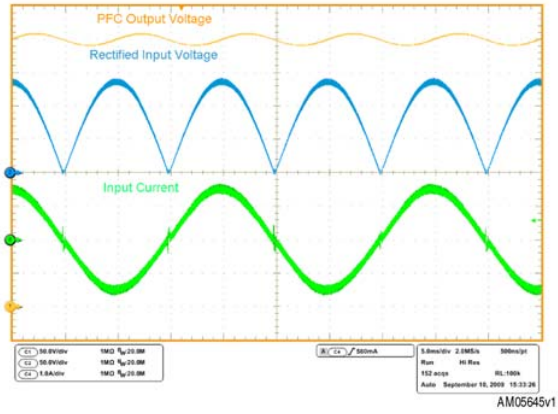
For user reference, waveforms of the input current and voltage at the nominal input voltage mains and nominal load conditions are shown in *Figure 5* and *6*.

Figure 5. EVL6563S-100W TM PFC: input current waveform at 230 V, 50 Hz, 100 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

Figure 6. EVL6563S-100W TM PFC: input current waveform at 100 V, 50 Hz, 100 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

The power factor (PF) and the total harmonic distortion (THD) have been measured too and the results are shown in *Figure 7* and *8*. As visible, the PF remains close to unity throughout the input voltage mains and the total harmonic distortion is very low.

Figure 7. EVL6563S-100W TM PFC: power factor vs. output power

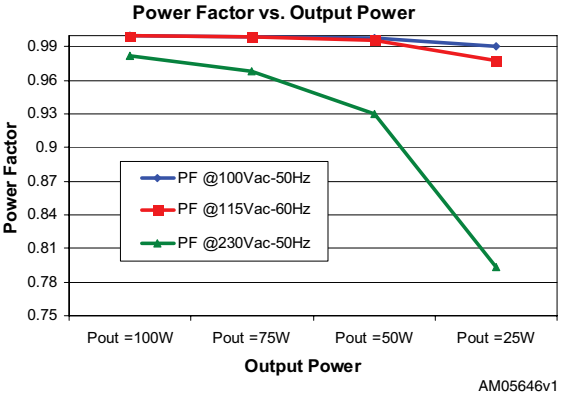
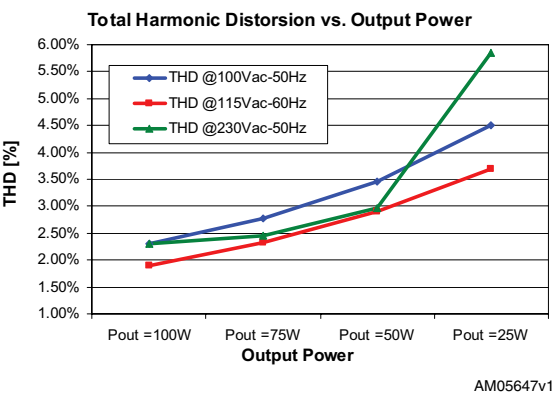


Figure 8. EVL6563S-100W TM PFC: THD vs. output power



The measured efficiency shown in *Figure 9*, measured according to the ES-2 requirements, is very good at all load and line conditions. At full load it is always higher than 93%, making this design suitable for high efficiency power supplies. The average efficiency, calculated according to the ES-2 requirements, at different nominal mains voltages is shown in *Figure 10*.

Figure 9. EVL6563S-100W TM PFC: efficiency vs. output power

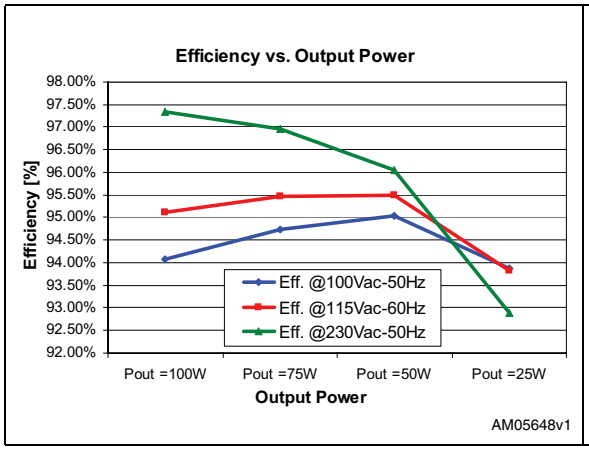


Figure 10. EVL6563S-100W TM PFC: average efficiency acc. to ES-2

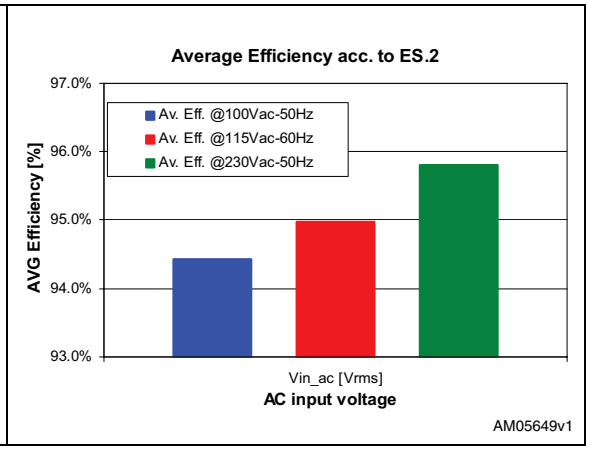
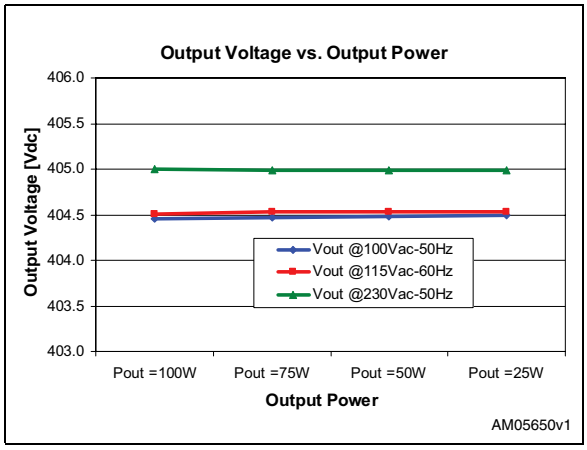


Figure 11. EVL6563S-100W TM PFC: static Vout regulation vs. output power



The measured output voltage at different line and static load conditions is shown in *Figure 11*. As visible, the voltage is very stable over the entire input voltage and output load range.

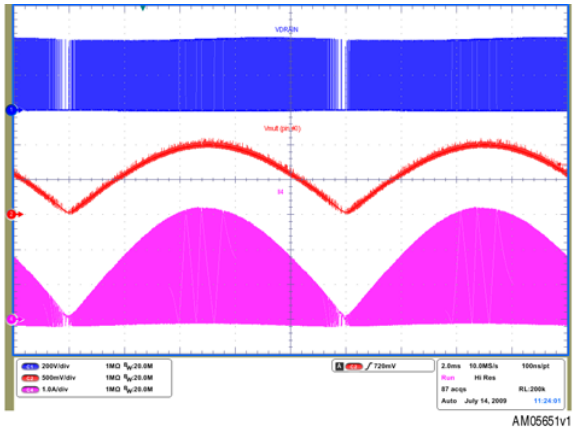
4.2 Inductor current in TM and L6563S THD optimizer

The following figures show the waveforms relevant to the inductor current at different voltage mains. As visible in *Figure 12* and *13* the peak inductor current waveform over a line half-period follows the MULT (pin #3) at both input mains voltages and therefore the line current

is in phase with the input AC voltage, giving low distortion of the current waveform and high power factor. On both the drain voltage traces, close to the zero-crossing points of the sine wave, it is possible to note the action of the THD optimizer embedded in the L6563S. It is a circuit that minimizes the conduction dead-angle of the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the THD (total harmonic distortion) of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore the offset is modulated by the voltage on the V_{FF} pin so as to have little offset at low line, where energy transfer at zero-crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

To obtain maximum benefit from the THD optimizer circuit, the high-frequency filter capacitors after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself, thus reducing the effectiveness of the optimizer circuit.

Figure 12. EVL6563H 100W TM PFC: Vds and inductor current at 100 Vac, 50 Hz, full load



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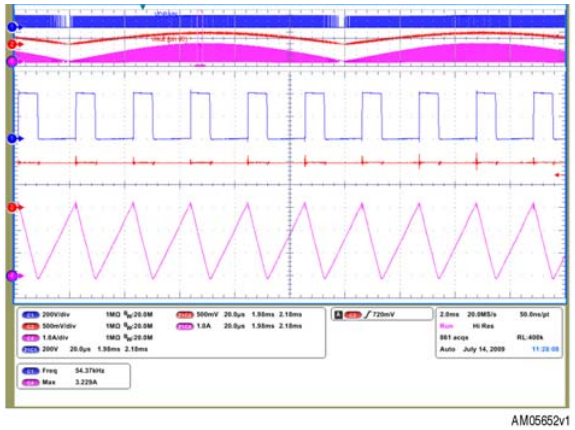
CH1: Q1 drain voltage
CH2: MULT voltage - Pin #3
CH4: L2 inductor current

Figure 13. EVL6563H 100W TM PFC: Vds and inductor current at 100 Vac, 50 Hz, full load (detail)



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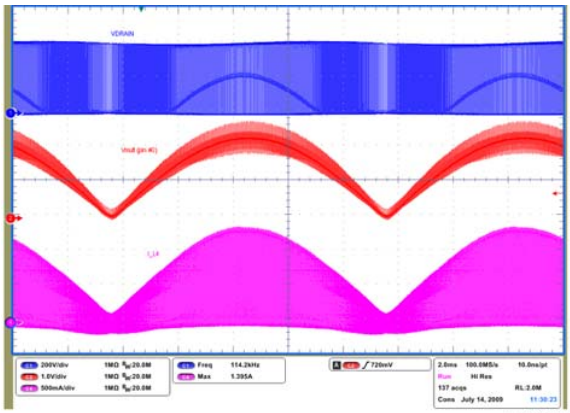
CH4: Q1 drain voltage
CH2: MULT voltage - pin #3
CH1: L2 inductor current

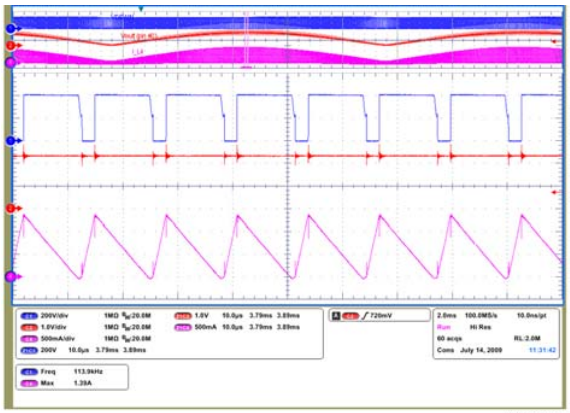
In *Figure 13* and *15* the detail of the waveforms at switching frequency allows measuring the operating frequency and the current peak at top of the input sine wave during operation at 100 Vac and 230 Vac. The multiplier waveform has been captured as a reference.

Figure 14. EVL6563H 100W TM PFC: Vds and inductor current at 230 Vac, 50 Hz, full load



CH4: Q1 drain voltage
CH2: MULT voltage - pin #3
CH1: L2 inductor current

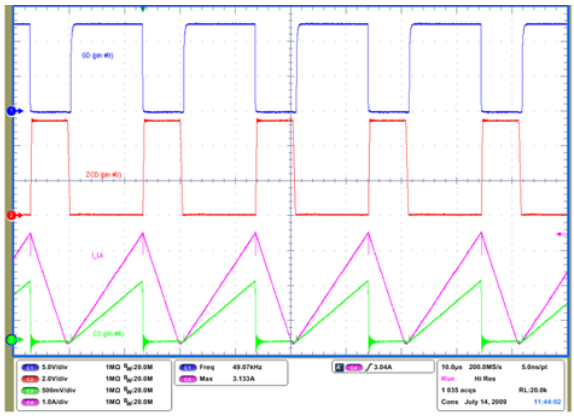
Figure 15. EVL6563H 100W TM PFC: Vds and inductor current at 230 Vac, 50 Hz, full load (detail)



CH4: Q1 drain voltage
CH2: MULT voltage - pin #3
CH1: L2 inductor current

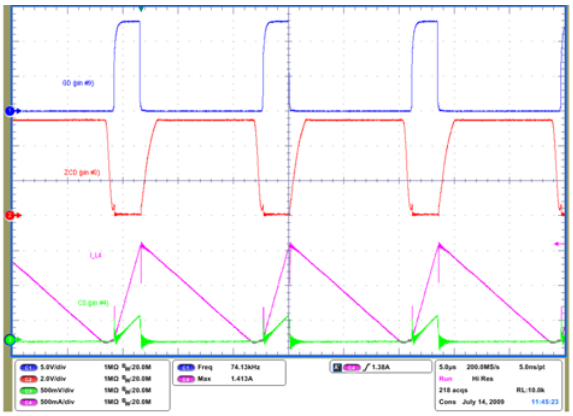
In *Figure 16* and *17* the detail of the waveforms at switching frequency shows the operation of transition-mode control. Once the inductor has transferred all the stored energy, a falling edge on the ZCD pin (pin #11) is detected and it will trigger a new on-time by setting the gate drive high. As soon as the current signal on the CS pin (pin #4) reaches the level programmed by the internal multiplier circuitry according to the input mains instantaneous voltage and the error amplifier output level, the gate drive is set low and MOSFET conduction is stopped. A following off-time will transfer the energy stored in the inductor into the output capacitor and to the load. At the end of the current conduction a new demagnetization will be detected by the ZCD that will provide for a new on-time of the MOSFET.

Figure 16. EVL6563S-100W TM PFC: Vds and inductor current at 100 Vac, 50 Hz, full load



CH1: GD - pin #13
CH2: ZCD - pin #11
CH3: CS - pin #4
CH4: L2 inductor current

Figure 17. EVL6563S-100W TM PFC: Vds and inductor current at 230 Vac, 50 Hz, full load



CH1: GD - pin #13
CH2: ZCD - pin #11
CH3: CS - pin #4
CH4: L2 inductor current

4.3 Voltage feed-forward and brownout function

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage as well as the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get f_c = 20 Hz at 264 Vac means having $f_c \approx$ 4 Hz at 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. A fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feed-forward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way, a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles, the amplitude of the multiplier output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

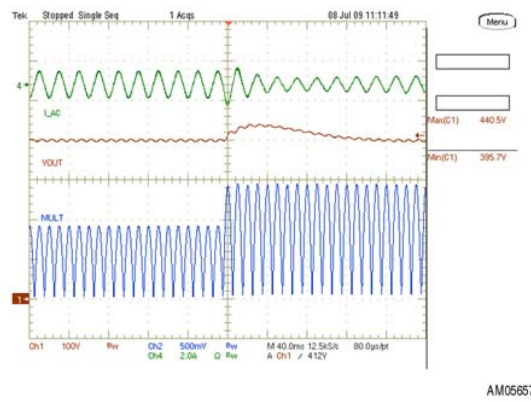
Actually, with other PFCs embedding the voltage feed-forward, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated will be affected by a considerable amount of

ripple at twice the mains frequency that will cause distortion of the current reference (resulting in high THD and poor PF). If it is too large, there will be a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6563S implements an innovative voltage feed-forward which, with a technique that overcomes this time constant trade-off issue whichever voltage change occurs (both surges and drops) on the mains. A capacitor C_{FF} (C13) and a resistor R_{FF} (R27 + R32), both connected to the V_{FF} (pin #5), complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin #3). In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode. In case of line voltage drop, an internal "mains drop" detector enables a low impedance switch which suddenly discharges C_{FF} avoiding a long settling time before reaching the new voltage level. Consequently, an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the preregulator's output like in systems with no feed-forward compensation.

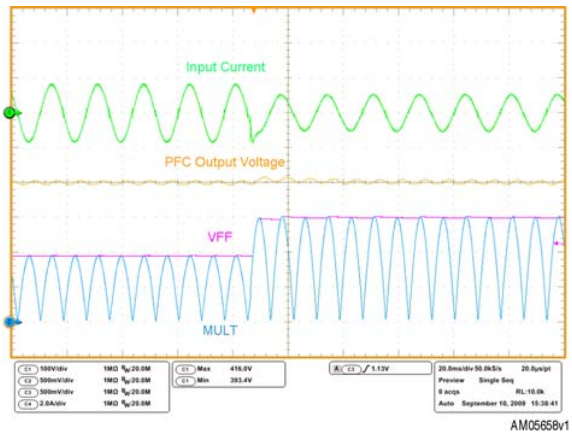
In *Figure 19* we find the behavior of the EVL6563S-100W demonstration board in case of an input voltage surge from 90 to 140 Vac. As shown, it is evident that the V_{FF} function provides for the stability of the output voltage which is not affected by the input voltage surge. In fact, thanks to the V_{FF} function, the compensation of the input voltage variation is very fast and the output voltage remains stable at its nominal value. The opposite is confirmed in *Figure 18* where the behavior of a PFC using the L6562A and delivering same output power is shown. The controller cannot compensate a mains surge and the output voltage stability is guaranteed by the feedback loop only. Unfortunately, as previously stated, its bandwidth is narrow and thus the output voltage has a significant deviation from the nominal value. The circuit has the same behavior in case of a mains surge at any input voltage, and it is also not affected if the input mains surge happens at any point along the input sine wave.

Figure 18. L6562A input mains surge 90 Vac to 140 Vac, no V_{FF} input



CH1: Vout
CH2: MULT (pin #3)
CH4: I_AC

Figure 19. EVL6563S-100W TM PFC: input mains surge 90 Vac to 140 Vac

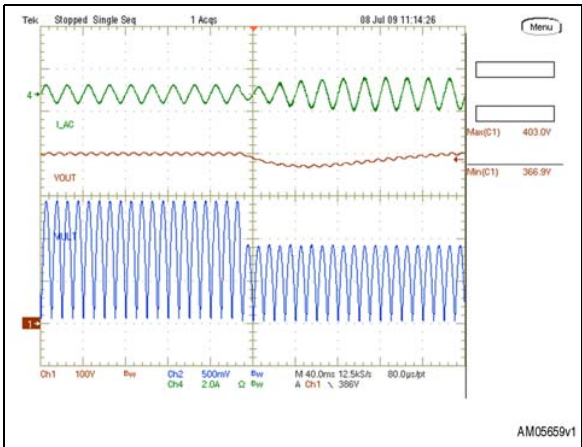


CH1: Vout
CH2: MULT (pin #3)
CH3: V_{FF} (pin #5)
CH4: I_AC

Figure 21 shows the circuit behavior in case of a mains dip. As previously described, the internal circuitry has detected the decreasing of the mains voltage and it has activated the C_{FF} internal fast discharge. As visible, in that case the output voltage changes but in few mains cycles it comes back to the nominal value. The situation is different if we check the performance of a controller without the V_{FF} function. *Figure 20* shows the behavior of a PFC using the L6562A delivering similar output power. In case of a mains dip from 140 Vac to 90 Vac, the output voltage variation is not very different, but the output voltage requires a longer time to restore the original value.

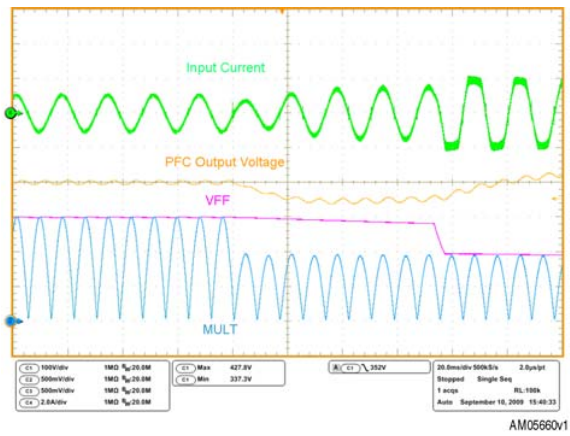
Testing with a wider voltage variation (e.g. 265 Vac to 90 Vac), the output voltage variation of a PFC without the voltage feed-forward fast discharge is emphasized even more.

Figure 20. L6562A input mains dip 140 Vac to 90 Vac, no V_{FF} input



CH1: Vout
CH2: MULT (pin #3)
CH4: I_AC

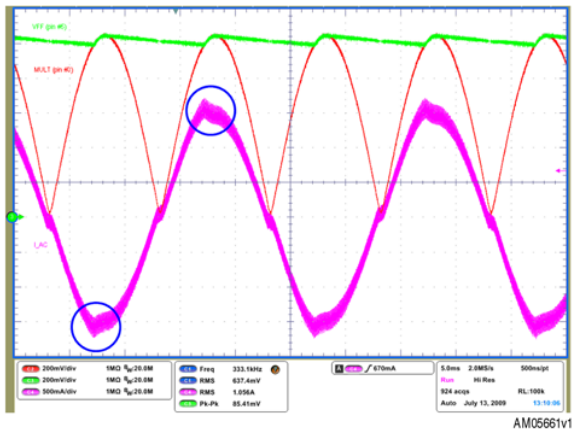
Figure 21. EVL6563S-100W TM PFC: input mains dip 140 Vac to 90 Vac



CH1: Vout
CH2: MULT (pin #3)
CH3: V_{FF} (pin #5)
CH4: I_AC

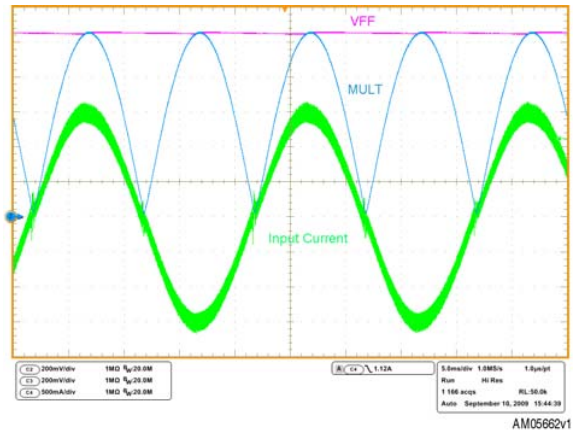
Comparing *Figure 22* and *23* we can see that the input current of the latter has a better shape and the 3rd harmonic current distortion is not noticeable. This demonstrates the benefits of the new voltage feed-forward circuit integrated in the L6563S. Allowing a fast response to mains disturbances but using a quite long V_{FF} time constant provides also very low THD and high PF at same time as confirmed by the measurements below.

Figure 22. L6563: input current at 100 Vac, 50 Hz, C_{FF}=0.47 µF, R_{FF}=390 kΩ



THD = 5.15%, 3RD harmonic = 43 mA
CH2: MULT (pin #3)
CH3: V_{FF} (pin #5)
CH4: I_AC

Figure 23. EVL6563S-100W TM PFC: input current at 100 Vac, 50 Hz, C_{FF}=1 µF, R_{FF}=1 MΩ

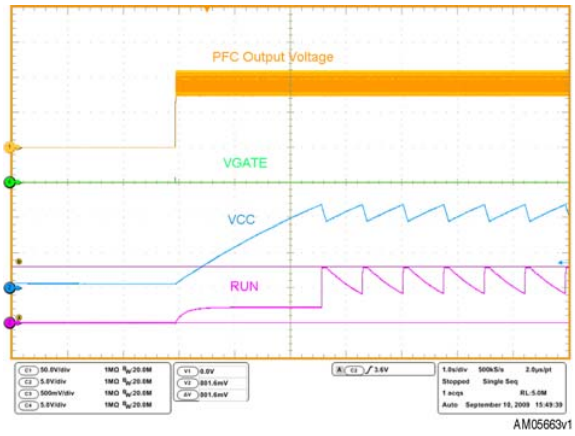


THD = 2.30%, 3RD harmonic = 25.8 mA
CH2: MULT (pin #3)
CH3: V_{FF} (pin #5)
CH4: I_AC

Another function integrated in the L6563S is the brownout protection, which is basically a non-latched shutdown function that must be activated when a mains undervoltage condition is detected. This abnormal condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also occur because the PFC pre-regulator works in open loop and this could be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shutdown the device in case of brownout.

Brownout function is done through sensing of the input mains by an internal comparator connected to RUN (pin #10), connected via a divider to V_{FF} (pin #5) which delivers a voltage signal proportional to the input mains. The enable and disable thresholds at which the L6563S will start or stop the operation can be adjusted by modifying that divider ratio. For additional information please see [*2* in *Section 8: References*].

Figure 24. EVL6563S-100W TM PFC startup attempt at 80Vac, 60 Hz, full load

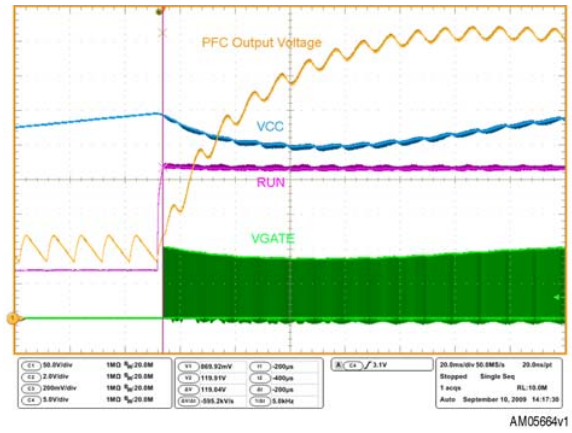


CH1: PFC output voltage
CH2: Vcc voltage (pin #14)
CH3: RUN (pin #10)
CH4: gate drive (pin #13)

In *Figure 24* a startup tentative below the threshold is captured. As visible at startup the RUN pin does not allow PFC startup.

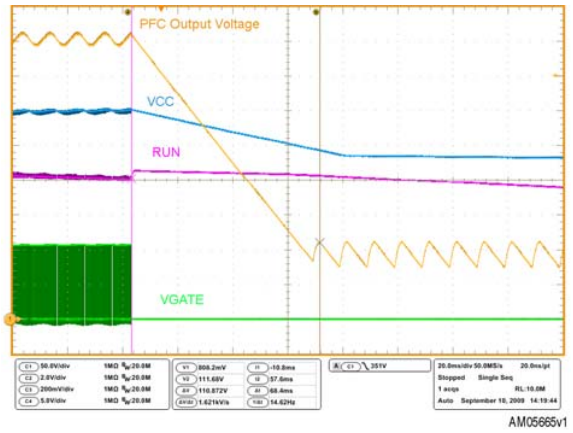
In *Figure 25* and *26* the waveforms of the circuit during operation of the brownout protection are captured. In both cases the mains voltage was increased or decreased slowly. As visible both at turn-on or turn-off there are no bouncing or starting attempts by the PFC converter.

Figure 25. EVL6563S-100W TM PFC: startup with slow input voltage increasing, full load



CH1: PFC output voltage
CH2: Vcc (pin #14)
CH3: RUN (pin #10)
CH4: Gate drive (pin #13)

Figure 26. EVL6533S-100W TM PFC: turn-off with slow input voltage decreasing, full load



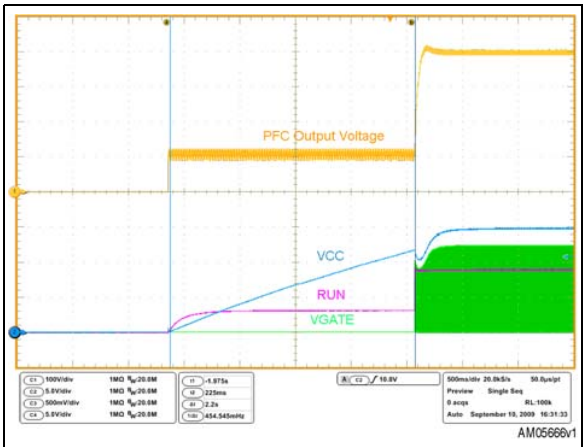
CH1: PFC output voltage
CH2: Vcc (pin #14)
CH3: RUN (pin #10)
CH4: Gate drive (pin #13)

4.4 Startup operation

On this demonstration board the startup resistors R7 and R16 charge C10 and C11 until the L6563S turn-on voltage threshold is reached, at which point the L6563S starts switching. Because once the turn-on threshold is reached the Vcc consumption increases and the current supplied by R7 and R16 is lower, the L6563S is initially supplied by the Vcc capacitor, and then the L1 auxiliary winding provides the voltage to supply the IC.

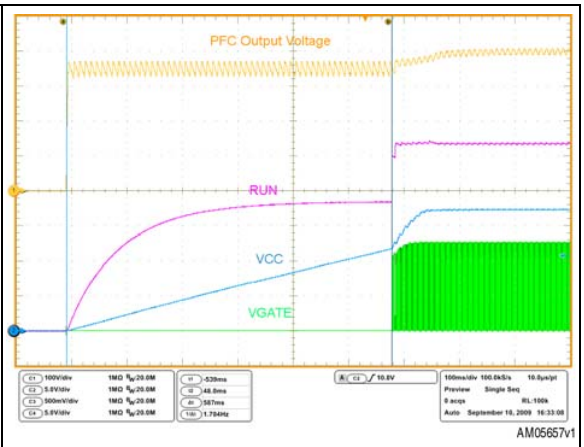
In the following *Figure 27* and *28* the waveforms during the startup of the circuit at mains plug-in are shown. We can notice that the Vcc voltage rises up to the turn-on threshold, and the L6563S starts operating. As mentioned previously, for a short time the energy is supplied by the Vcc capacitor, and then the auxiliary winding with the charge pump circuit takes over. At the same time, the output voltage rises from the peak value of the rectified mains to the nominal value of the PFC output voltage. The good margin of the compensation network allows a clean startup, without any large overshoot.

Figure 27. EVL6563S-100W TM PFC startup at 90 Vac, 60 Hz, full load



CH1: PFC output voltage
CH2: Vcc voltage (pin #14)
CH3: RUN (pin #10)
CH4: Gate drive (pin #13)

Figure 28. EVL6563S-100W TM PFC startup at 265 Vac, 50 Hz, full load



CH1: PFC output voltage
CH2: Vcc voltage (pin #14)
CH3: RUN (pin #10)
CH4: Gate drive (pin #13)

4.5 PFC_OK pin and feedback failure (open loop) protection

During normal operation, the voltage control loop provides for the output voltage (Vout) of the PFC pre-regulator close to its nominal value, set by the resistor ratio of the feedback output divider. In the L6563S the PFC_OK pin has been dedicated to monitor the output voltage with a separate resistor divider composed of R3, R6, R11 (high) and R15 (low), see *Figure 2*. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (V_{OVP}), usually larger than the maximum Vout that can be expected, also including worst-case load/line transients.

For the EVL6563S-100W we have:

- For the EVL6563H-100W we have:
  - V_O = 400 V
  - V_{OVP} = 434 V
  - Select: R3+R4+R11 = 8.8 MΩ

  then:
  - R15 = 8.8 MΩ·2.5/(434-2.5) = 51 kΩ

Once this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. An example is given in *Figure 29*.

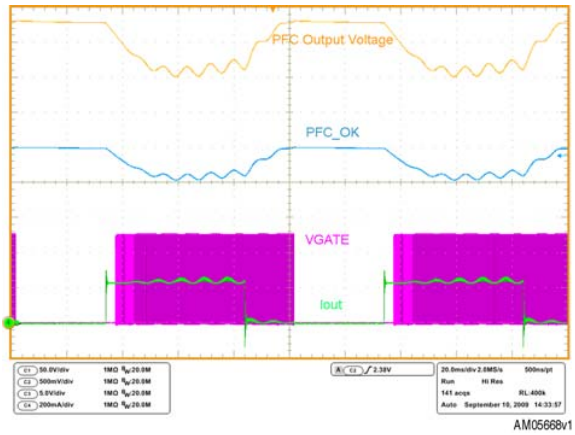
Notice that both feedback dividers connected to L6563S V_INV (pin #1) and PFC_OK (pin #7) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above is able to handle "normal" overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the overvoltage is generated by a feedback disconnection, for instance, when one of the upper resistors of the output divider fails open, an additional circuitry detects the voltage drop of pin INV. If the voltage on pin INV is lower than 1.66 V and at the same time OVP is active, a feedback failure is assumed. Thus, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system, it is necessary to recycle the input power, so that the Vcc voltage of the L6563S goes below 6 V and that one of the PWM controllers goes below its UVLO threshold.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating results in shutting down the IC and stopping the pre-regulator.

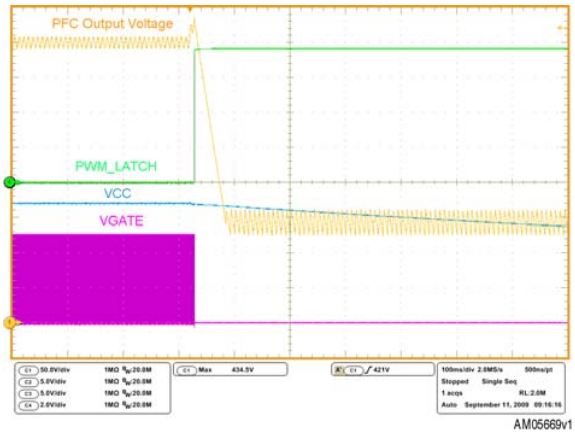
Moreover, the pin PFC_OK doubles its function as a non-latched IC disable. A voltage below 0.23V shuts down the IC, reducing its consumption below 2 mA. To restart the IC, simply let the voltage at the pin go above 0.27 V.

Figure 29. EVL6563S-100W TM PFC load transient at 115 Vac, 60 Hz, full load to no load



CH1: PFC output voltage
CH2: PFC_OK (pin #7)
CH3: gate drive (pin #13)
CH4: Iout

Figure 30. EVL6563S-100W TM PFC open loop at 115 Vac, 60 Hz, full load



CH1: PFC output voltage
CH2: Vcc (pin #14)
CH3: gate drive (pin #13)
CH4: PWM_LATCH (pin #8)

The event of an open loop is captured in *Figure 30*. We can notice the protection intervention, latching the operation of the L6563S. As mentioned previously, to restart the system the input power must be recycled.

4.6 TBO (tracking boost option)

To use the TBO function on L6563S, a dedicated input of the multiplier is available on pin #6 (TBO). The function can be implemented by simply connecting a resistor (RT) between the TBO pin and ground.

Usually, in traditional PFC stages, the DC output voltage is regulated at a fixed value (typically 400 V) but in some applications, it may be advantageous to regulate the PFC output voltage with the "tracking boost" or "follower boost" approach. In this way the circuit with the TBO function provides better efficiency and thanks to the lower differential voltage across the boost inductor, the value of L2 can be reduced as compared to the same circuit without the TBO function.

The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is representative of the mains RMS voltage. The resistor defines a current, equal to V(TBO)/RT, that is internally 1:1 mirrored and sunk from pin INV (pin 1) input of the error amplifier. In this way, when the mains voltage increases, the voltage at the TBO pin increases also as well as the current flowing through the resistor connected between TBO and GND. Then a larger current will be sunk by the INV pin and the output voltage of the PFC pre-regulator will be forced to go higher. Obviously, the output voltage will move in the opposite direction if the input voltage decreases.

To avoid an undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3 V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output

tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open. The device will regulate at a fixed output voltage.

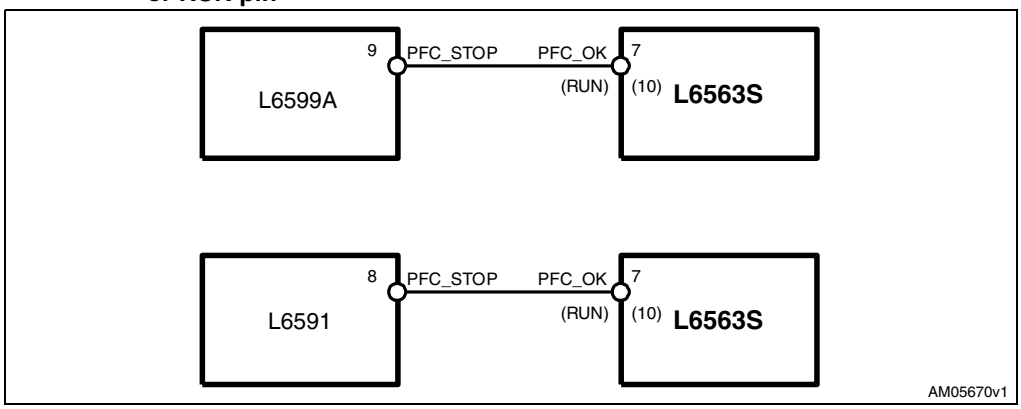
4.7 Power management and housekeeping functions

A special feature of the L6563S is that it facilitates the implementation of the "housekeeping" circuitry needed to coordinate the operation of the PFC stage with the cascaded DC-DC converter. The functions implemented by the housekeeping circuitry ensure that transient conditions like power-up or power-down sequencing or failures of either power stage are properly handled. The L6563S provides pins to do that.

As already mentioned, one communication line between the L6563S and the PWM controller of the cascaded DC-DC converter is the PWM_LATCH (pin #8), which is normally open when the PFC works properly. It goes high if the L6563S loses control of the output voltage (because of a failure of the control loop) with the aim of latching off the PWM controller of the cascaded DC-DC converter as well.

A second communication line can be established via the disable function included in the RUN pin. Typically, this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6563S in case of light load, in order to minimize the no-load input consumption of the power supply.

Figure 31. L6563S on/off control by a cascaded converter controller via the PFC_OK or RUN pin



The third communication line is the PWM_STOP (pin #9), which works in conjunction with the RUN (pin#10). The purpose of the PWM_STOP pin is to inhibit the PWM activity of both the PFC stage and the cascaded DC-DC converter. The pin is an open collector, normally open, that goes low if the device is disabled by a voltage lower than 0.8 V on the RUN (pin #10). It is important to point out that this function works correctly in systems where the PFC stage is the master and the cascaded DC-DC converter is the slave or, in other words, where the PFC stage starts first, powers both controllers and enables/disables the operation of the DC-DC stage. This function is quite flexible and can be used in different ways. In systems comprising an auxiliary converter and a main converter (e.g. a desktop PC's silver box or hi-end flatscreen TV or monitor), where the auxiliary converter also powers the controllers of the main converter, the RUN (pin #10) can be used to start and stop the main converter. In the simplest case, to enable/disable the PWM controller the PWM_STOP (pin #9) can be connected to either the output of the error amplifier or, if the chip is provided with it, to its soft-start pin.

The EVL6563S-100W offers the possibility to test these functions by connecting it to the cascaded converter via the series resistors R28, R29, R30. Regarding the PWM_STOP (pin #9) pin that is an open collector type, if it needs a pull-up resistor, please connect it close to the cascaded PWM for better noise immunity.

Figure 32. Interface circuits that let the L6563S switch on or off a PWM controller, not latched

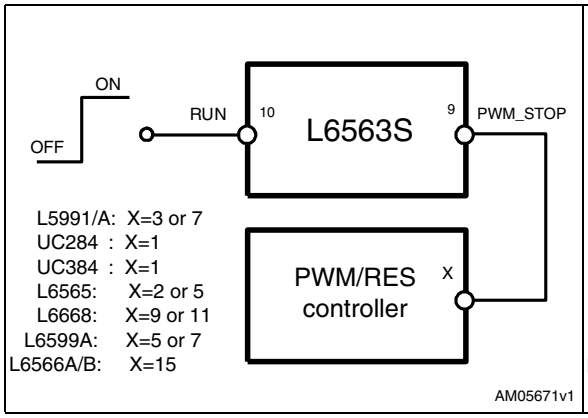
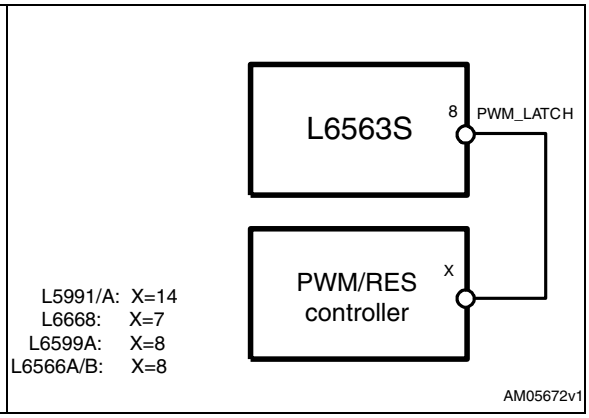


Figure 33. Interface circuits that let the L6563S switch on or off a PWM controller, latched



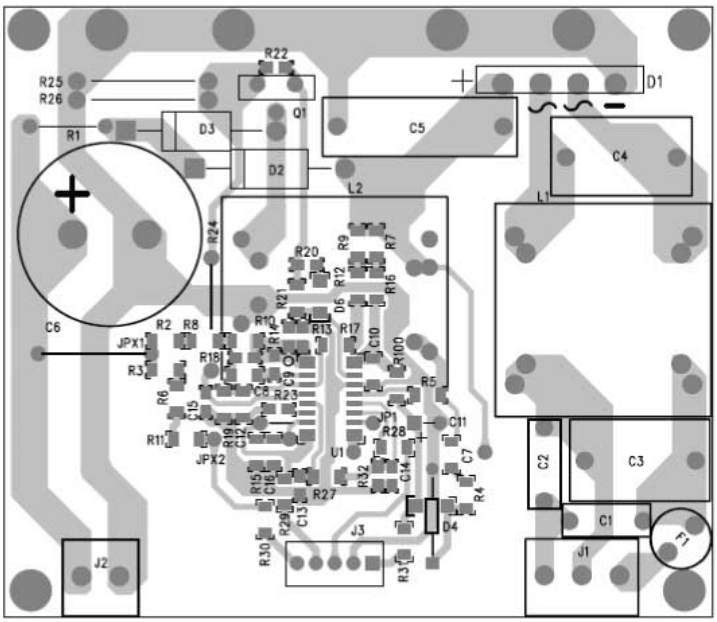
5 Layout hints

The layout of any converter is a very important phase in the design process needing attention by the design engineers like any other design phase. Even if it the layout phase sometimes looks time-consuming, a good layout does indeed save time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages which allows consistent cost saving.

Converters using the L6563S do not require any special or specific layout rule, just the general layout rules for any power converter have to be applied carefully. Basic rules are listed here below. They can be used for other PFC circuits having any power level, working either in transition mode or with a fixed-off time control.

1. Keep power and signal RTN separated. Connect the return pins of components carrying high current such as the input filter, sense resistors, or the output capacitor as close as possible. This point is the RTN star point. A downstream converter will have to be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, MOSFET drain, boost rectifier and output capacitor.
3. Keep signal components as close as possible to each L6563S relevant pin. Specifically, keep the tracks relevant to the pin #1 (INV) net as short as possible. Components and traces relevant to the error amplifier have to be placed far from traces and connections carrying signals with high dV/dt like the MOSFET drain. For high-power converters or very compact PCB layouts, a 10 nF capacitor connected to pin #8 (PWM_LATCH) and pin #12 (GND) might be required to decrease the noise picked up by this pin while it is in its high impedance status.
4. Please connect heatsinks to power GND.
5. Add an external shield to the boost inductor and connect it to power GND.
6. Please connect the RTN of signal components including the feedback, PFC_OK and MULT dividers close to the L6563S pin #14 (GND).
7. Connect a ceramic capacitor (100÷470 nF) to pin #14 (Vcc) and pin #12 (GND), close to the L6563S. Connect this point to the RTN star point (see rule *1*).

Figure 34. EVL6563S-100W TM PFC PCB layout (SMT side view)



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6 EMI filtering and conducted EMI pre-compliance measurements

The following figures show the peak measurement of the conducted noise at full load and nominal mains voltages for both mains lines. The limits shown in the diagrams are EN55022 class-B which is the most popular regulation for domestic equipment using a two-wire mains connection.

It is also useful to remind that typically a PFC produces a significant differential mode noise with respect to other topologies and therefore in case an additional margin with respect to the limits is required, we suggest trying to increase the across-the-line (X) capacitors or the capacitor after the rectifier bridge C5. This will be more effective and cheaper than increasing the size of the common-mode filter coil that would filter the differential mode noise by the leakage inductance between the two windings only.

In order to recognize if the circuit is affected by common mode or differential mode noise it is sufficient to compare the spectrum of phase and neutral line measurements. If the two measurements are very similar, the noise is almost totally common mode. If there is a significant difference between the two measurement spectrums, their difference represents the amount of differential mode noise. Of course to get a reliable comparison the two measurements have to be done in the same conditions. If the peak measurement is used as in the figures below, some countermeasures will have to be used, like synchronizing the sweep of the spectrum analyzer with the input voltage. This is necessary with TM PFC having a switching frequency that is modulated along the sine wave.

Because the differential mode produces the common mode noise by the magnetic field induced by the current, decreasing the differential mode consequently limits the second one.

Figure 35. EVL6563S-100W TM PFC CE peak measurement at 100 Vac, 50 Hz, full load, phase

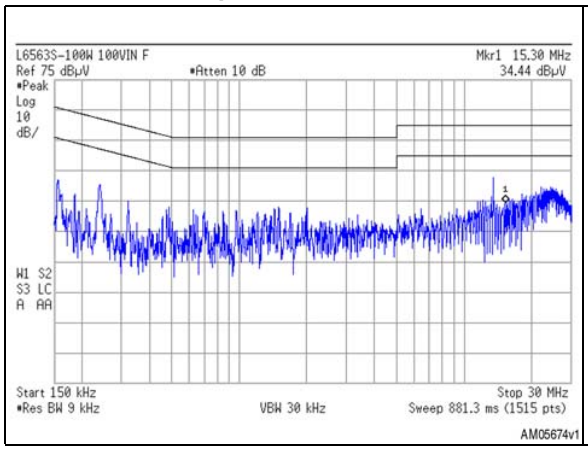


Figure 36. EVL6563S-100W TM PFC CE peak measurement at 100 Vac, 50 Hz, full load, neutral

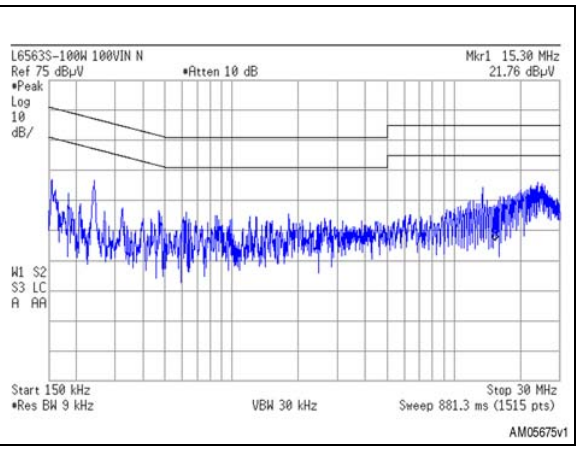


Figure 37. EVL6563S-100W TM PFC CE peak measurement at 230 Vac, 50 Hz, full load, phase

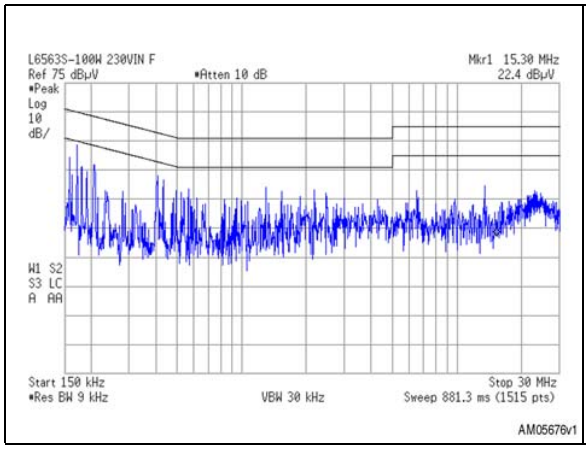
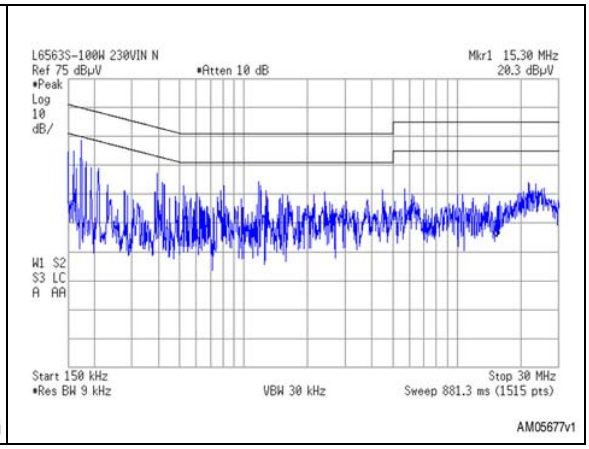


Figure 38. EVL6563S-100W TM PFC CE peak measurement at 230 Vac, 50 Hz, full load, neutral



As visible in the diagrams, in all test conditions there is a good margin of the measures with respect to the limits. The measurements have been done in peak detection to speed up the sweep, otherwise taking a long time. Please note that the measurements done in quasi-peak or average as required by the regulation will be much lower because of the jittering effect of the TM control that cannot be evaluated in peak detection.

7 PFC coil specifications

7.1 General description and characteristics

- Applications: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, 6+6 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temp.: 60 °C
- Mains insulation: N.A.
- Unit finish: varnish

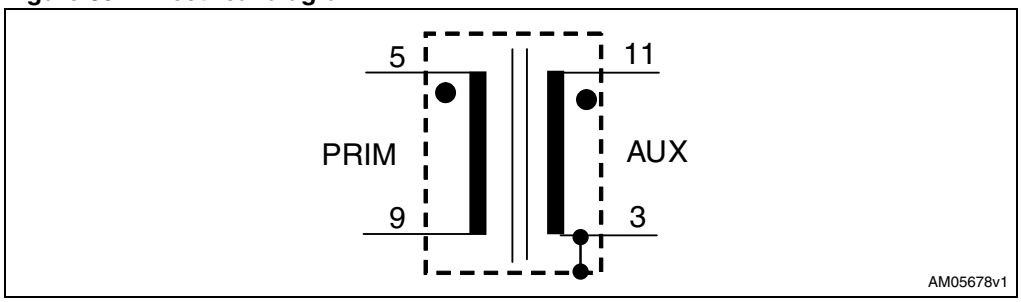
7.2 Electrical characteristics

- Converter topology: boost, transition mode
- Core type: PQ26/20 - PC44
- Min. operating frequency: 40 kHz
- Typical operating freq: 120 kHz
- Primary inductance: 520 µH 10% at 1 kHz - 0.25 V (see note below)
- Peak primary current: 4.2 Apk
- RMS primary current: 1.4 Arms

Note: Measured between pins #5 and #9

7.3 Electrical diagram

Figure 39. Electrical diagram



7.4 Winding characteristics

Table 2. Winding characteristics

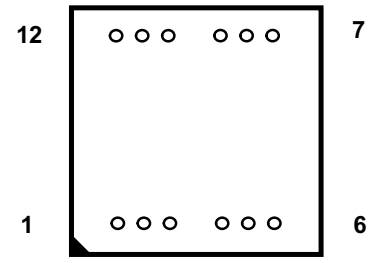
Pins	Winding	RMS current	Number of turns	Wire type
5 - 9	Primary(1)	1.4 A_{RMS}	57.5 - fit	Multi stranded #7 x ϕ 0.20 mm
11 - 3	Aux (2)	5.5 spaced	5.5 - spaced	ϕ 0.28 mm

1. Primary winding external insulation: 2 layers of polyester tape
2. Aux winding is wound on top of primary winding. External insulation with 2 layers of polyester tape

7.5 Mechanical aspect and pin numbering

- Maximum height from PCB: 21.5 mm
- Coil former type: vertical, 6+6 pins
- TDK P/N: BPQ26/20-1112CP
- Pins #1, 2, 4, 6, 7, 10, 12 are removed - pin 8 is for polarity key
- External copper shield: not insulated, wound around the ferrite core, including the coil former. It must be well adhered to the ferrite. Height is 8 mm. Connected to pin #3 by a soldered, solid wire.

Figure 40. Top view



7.6 Unit identification

- Manufacturer: TDK
- Manufacturer P/N: SRW2620PQ-X22V102

8 References

1. L6563S datasheet.
2. AN3027 “How to design a Transition Mode PFC pre-regulator with the L6563S and L6563H”.

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
04-Jun-2010	1	Initial release.
06-Sep-2010	2	Content reworked to improve readability.