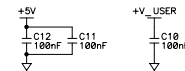


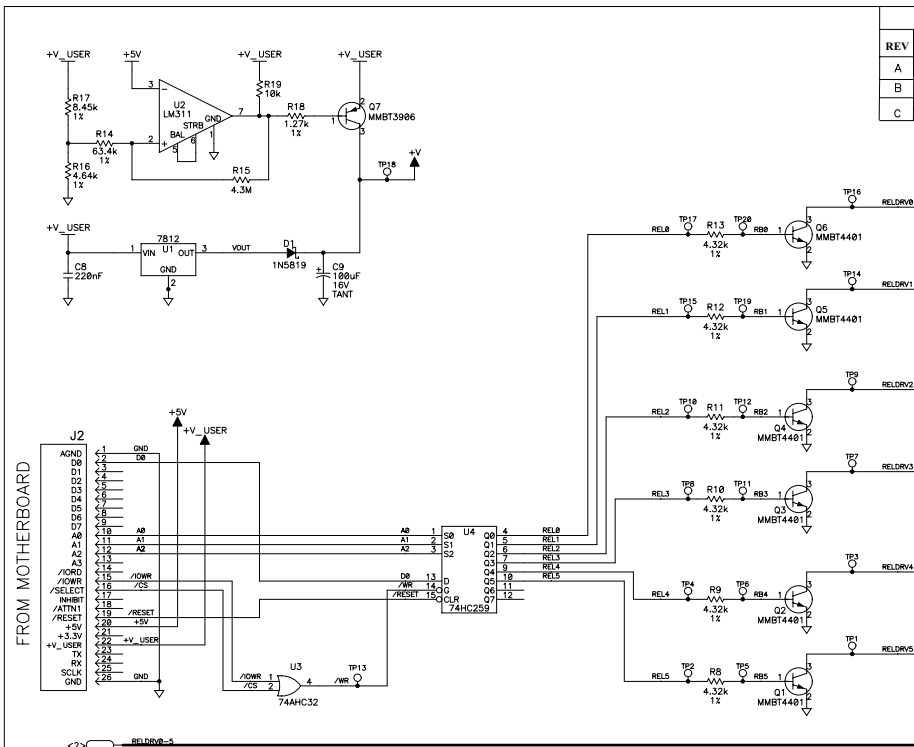
| REVISION HISTORY |        |   | REVISION APPROVAL |               |                  |               |
|------------------|--------|---|-------------------|---------------|------------------|---------------|
| REV              | ECO    | DESCRIPTION                               | PROJECT ENGINEER  | APPROVAL DATE | DOCUMENT CONTROL | APPROVAL DATE |
| A                | E11217 | INITIAL RELEASE                           | DM                | 11/20/01      | KIS              | 7/17/01       |
| B                | E11564 | CHANGED PE7 TO OUTPUT INHIBIT             | DM                | 28JUN01       | KIS              | 7/17/01       |
| C                | E11715 | CORRECTED REL2COM TO REL2NO ON J1 PIN 14. | DM                | 11/2/01       | KIS              | 11/1/01       |

TABLE A

| REF DES | DEVICE  | DEVICE VOLTAGE INFORMATION |     |     |         |             | DEVICE: FILTER CAP |
|---------|---------|----------------------------|-----|-----|---------|-------------|--------------------|
|         |         | AGND                       | GND | +5V | +V_USER | NO CONNECTS |                    |
| U1      | 7812    |                            |     |     |         |             |                    |
| U2      | LM311   |                            | 4   |     | 8       |             | C10                |
| U3      | 74AHC32 |                            | 3   | 5   |         |             | C11                |
| U4      | 74HC259 |                            | 8   | 16  |         |             | C12                |



- NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTOR VALUES ARE IN OHMS, 1/10W, 5%
  2. ALL CAPACITORS ARE 50VDC OR HIGHER.
  3. THE ORIGINATOR SOURCE OF A VOLTAGE IS REPRESENTED BY (VCC), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY (VCC).



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| APPEND THE FOLLOWING DOCUMENTS WHEN CHANGING THIS DOCUMENT: |  | DRAWING CONTENT:            |                 | TITLE      |   |
|---|--|-----------------------------|-----------------|------------|---|
|   |  | DRAWN BY: (INITIAL RELEASE) | J.H.            | 26JAN00    | SCHEMATIC DIAGRAM<br>SR9500 SERIES<br>RELAY BOARD |
|   |  | REVISED BY:                 | K.SCHALLER      | NOV1, 2001 |   |
|   |  | APPROVALS: INITIAL RELEASE  |                 |            |   |
|   |  | PROJECT ENGINEER:           | DARREN MUSGROVE | 11/20/00   |   |
|   |  | ENGINEERING MANAGER:        |                 |            | SIZE <b>B</b> DWG NO. <b>090-0098</b>             |
|   |  | SIGNATURES                  |                 | DATE       | SCALE NONE RELEASE DATE 11/20/00 SHEET 1 OF 2     |



