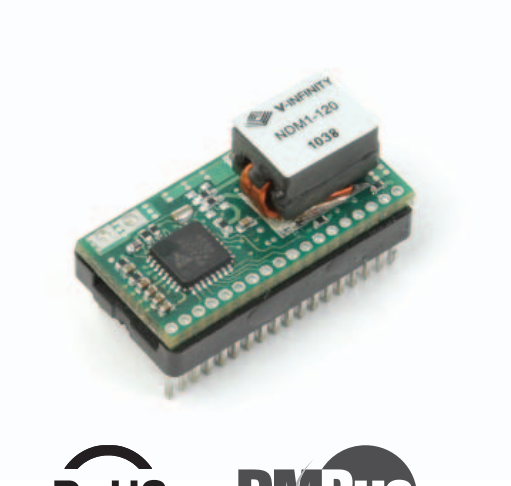
MODEL: NDM1-12-120

DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER

FEATURES

- Compact package (0.5" x 0.925" x 0.46")
- 12 A output
- High efficiency, 95%
- 8.5 ~ 14 V input range
- 0.6 ~ 2.5 V output range
- Auto-control™ technology
- Through-hole
- PMBus compliant
- Voltage/current/temperature monitoring
- Programmable output voltages
- Voltage margining
- Differential voltage sense
- Synchronize controllers for phase spreading operations
- Programmable soft start and soft stop
- Pre-bias startup
- Input under voltage lockout
- Output over voltage protection
- Output over current protection
- Fast over current protection
- Over temperature protection



RoHS PMBus

CONTENTS

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

ABSOLUTE MAXIMUM RATINGS

characteristics		min	nom	max	units
VIN	Input voltage	8		15	V
VOUT	Output voltage	0.5		2.8	V
IOUT	Output current			20	A
Logic IO Voltage	SYNC, PG, FAULT, CTRL, SLART, SDA, SCL	-0.3		5.5	V
Ground Voltage	GND	-0.3		+0.3	V
Analog Pin Voltage	VOUT, VSET, CRC, SENSE+, SENSE-, ADDR1, ADDR2	-0.3		5.5	V
Operating ambient			TBD		
Storage temp.		-55		125	˚C

INPUT / SUPPLY

parameter	conditions/description	min	nom	max	units
voltage		8.5	12	14	V
idle current	sysgood, no output, V_{IN} = 12 V			50	mA

OUTPUT

parameter	conditions/description	min	nom	max	units
voltage adjustment range	set using PMBus	0.6		2.5	V
voltage margin range[1]		-20	5	20	%
voltage accuracy	0.6 V ≤ Vout < 1.2 1.2 V ≤ Vout < 2.5		±3 ±2		% %
voltage ripple			8	25	mVp-p
current range		0		12	A
line regulation	V_{IN} = 8.5 ~ 14 V	-1		1	%
load regulation	V_{IN} = 12 V	-1		1	%
SENSE+ input bias current	SENSE+ = 4V	864	1,000	1,185	µA
SENSE- input bias current	SENSE- = 0.1V	20	25	30	µA
ramp-up time	adjustable via PMBUS	0.5		147.5	ms
ON time delay range	adjustable via PMBUS	0		1,000	ms
start-up time				50	ms
load transient voltage deviation	C_O = 500 µF		±35		mV
load transient recovery time	V_{IN} = 12 V, C_O = 500 µF , V_O = 1 V, 50% load step			100	µs
recommended minimum output capacitor	ceramic	500			µF

1.Voltage absolute maximum of 2.8 V

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

GENERAL / POWER / EFFICIENCY

parameter	conditions/description	min	nom	max	units
output power		0		30	W
efficiency	V_{IN} = 12 V, V_O = 1 V, 50% of maximum I_O V_{IN} = 12 V, V_O = 1 V, maximum I_O V_{IN} = 12 V, V_O = 2.5 V, 50% of maximum I_O V_{IN} = 12 V, V_O = 2.5 V, maximum I_O		92.2 89.0 94.9 93.4		% %
idle power	sysgood, no output, V_{IN} = 12 V			0.6	W
switching frequency			500		kHz

FAULT PROTECTION

parameter	conditions/description	min	nom	max	units
power good range		-10		10	%nom
over voltage threshold (OVP)				3.8	V
over current threshold (OCP)	adjustable via PMBUS			20	A
fast current protection (LCP) threshold	must be 2x OCP			40	A
fast current protection (LCP) set point accuracy		-20		20	%
fast current protection (LCP) delay		0.2		0.25	µs
thermal protection threshold (OTP)	adjustable via PMBUS	-40	105	125	˚C
thermal protection hysteresis			15		˚C

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

COMMUNICATION CONNECTIONS

symbol	pin	IO type	nominal operating voltage	description
n/c	1	--	--	No connect
SENSE+	2	Analog I	0 ~ 2.8 V	Output voltage positive sense input
SENSE-	3	Analog I	0 ~ 0.1 V	Output voltage negative sense input
n/c	4	--	--	No connect
ADDR2	5	Analog I	Resistor	Address setting for serial communication/configuration
ADDR1	6	Analog I	Resistor	Address setting for serial communication/configuration
VSET	7	Analog I	Resistor	Output voltage setpoint configuration pin
CRC	8	Analog I	-0.1 ~ 0.1 V	Return path for external setting resistors (VSET, ADDR1, ADDR2)
SYNC	9	Digital IO (pull-up)	3.3 V	Frequency sync. port. Controller can be configured as master or slave.
PG	10	Digital IO (pull-up)	3.3 V	Power Good. Indicates output voltage rail is within regulation. Goes low under any fault condition or recognition of shutdown request. May be used to cascade (sequence) VR start-up in combination with SYSG pin (on following VRs).
FAULT	11	Digital IO (pull-up)	3.3 V	Fault output. Wired and Internal pull-up. Goes low under any fault condition (UVLO, OCP, OVP, OTP). When pulled low controller is disabled and restarts again when released. Used for fault management between multiple POLs
CTRL	12	Digital IO	3.3 V	Control or Enable pin. No internal pull-up resistor.
SALRT	13	Digital IO	3.3 V	Alert line. Communicates fault or pending fault alert to master or host system power manager.
SDA	14	Digital IO	3.3 V	SMBus compatible data serial input/output.
SCL	15	Digital IO	3.3 V	SMBus compatible clock serial input.
n/c	16	--	--	No connect
5V	17	Power in	5 V in	Supply voltage for driver
3.3V	18	Power in	3.3 V in	Supply voltage for controller

POWER CONNECTIONS

symbol	pin	IO type	nominal operating voltage	description
VIN	19~20	Power	8.5 ~ 14 V	Input voltage
GND	21~22	Ground	--	Power ground
VOUT	23~24	Power	0.6 ~ 2.5 V	Output voltage

LOGIC INPUT/OUTPUT CHARACTERISTICS

parameter	conditions/description	min	nom	max	units
input high voltage (V_{IH})	CTRL, SCL, SDA, SYNC, PG, FAULT	2			V
input low voltage (V_{IL})	CTRL, SCL, SDA, SYNC, PG, FAULT			0.8	V
output high voltage (V_{OH})	SALRT, SCL, SDA, SYNC, PG, FAULT	2.25			V
output low voltage (V_{OL})	SALRT, SCL, SDA, SYNC, PG, FAULT			0.4	V

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

PMBUS

parameter	conditions/description	min	nom	max	units
setup time, SMBus (t_{set})		300			ns
hold time, SMBus (t_{hold})		250			ns

ANALOG SIGNALS

parameter	conditions/description	min	nom	max	units
analog IO	SENSE+	0		2.8	V
analog IO	SENSE-	0		0.1	V

POWER MANAGEMENT FEATURES

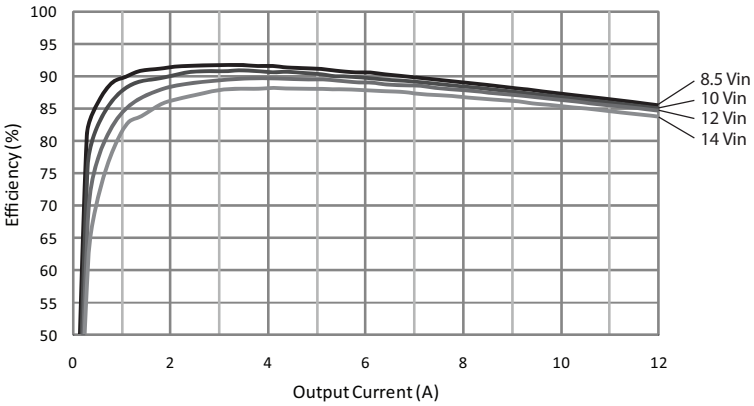
parameter	conditions/description	min	nom	max	units
number of addressable devices		1		113	devices
input UVLO turn-on threshold		8.5			V
input UVLO turn-off threshold				8.1	V
PMBUS input voltage monitoring accuracy		-170		170	mV
PMBUS output voltage monitoring accuracy		-30		30	mV
PMBUS output current monitoring accuracy	0.6 V ≤ Vout < 2.0, Io ≥ 6 A 2.0 V ≤ Vout < 2.5, Io ≥ 6 A		±12% ±15%		
PMBUS temperature monitoring accuracy		-5		5	˚C

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

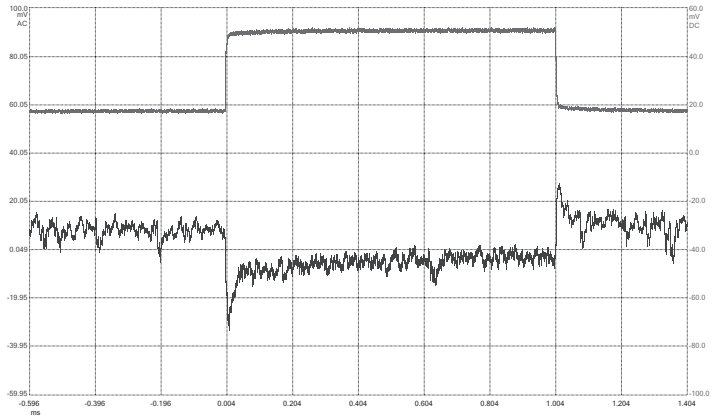
0.6V / 12A TYPICAL CHARACTERISTICS

Conditions (applies to all graphs unless stated otherwise): V_I = 12 V, I_O = 12 A load, Co = 500 µF

Efficiency



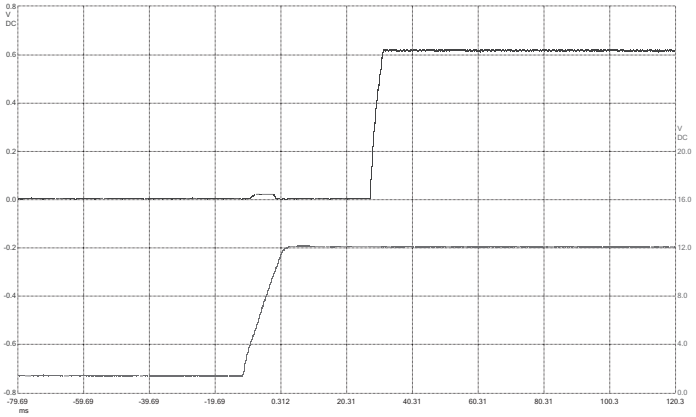
Output Load Transient Response



Current step-change (3-9-3 A)
Top Trace: Load Current
Slew Rate: (1A/µs)

Bottom Trace: Output Voltage (20 mV /div)
Time Scale: (200 µs / div)

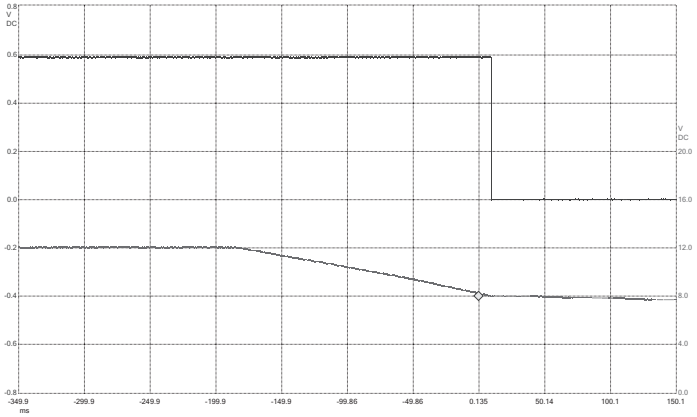
Start-up



Top Trace: Output Voltage (200 mV / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (20 ms / div)

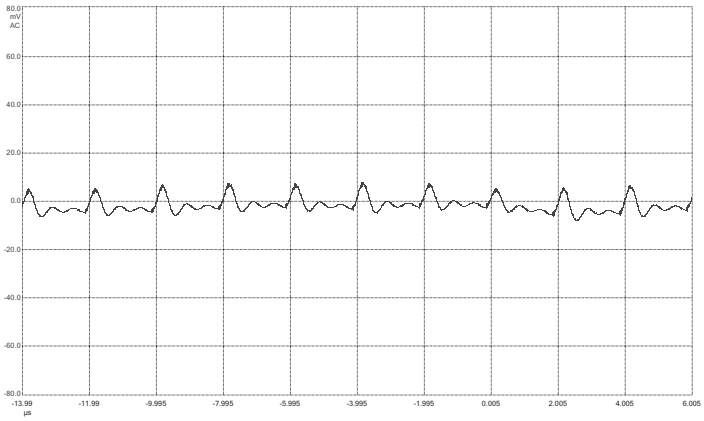
Shut-down



Top Trace: Output Voltage (200 mV / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (50 ms / div)

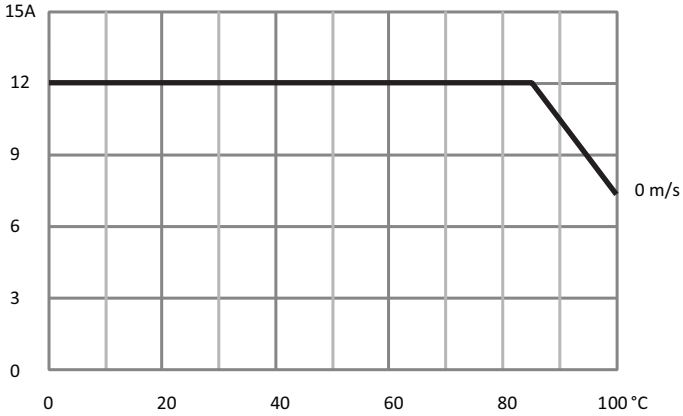
Output Ripple and Noise



Trace: Output Voltage (20 mV / div)

Time Scale: (2 µs / div)

Output Current Derating



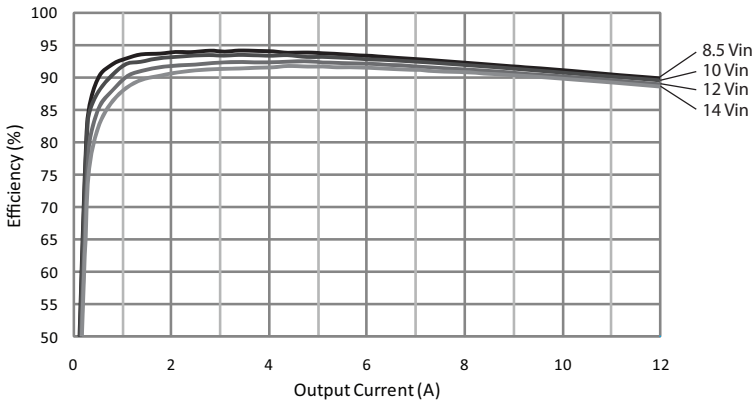
Vi=12V, modules mounted on a 6" X 4", 2 oz, 6-Layer test board

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

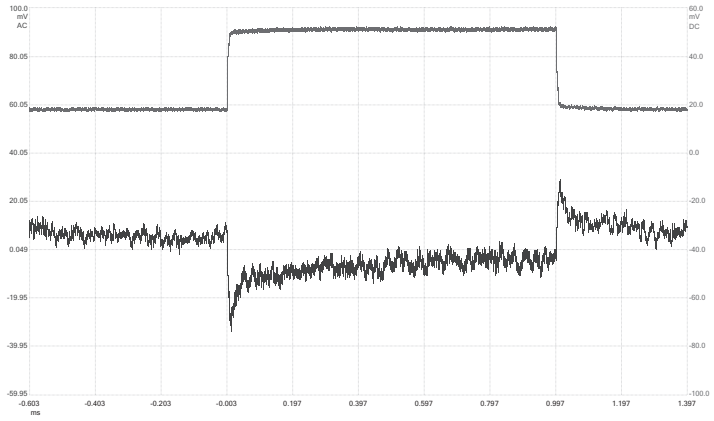
1.0V / 12A TYPICAL CHARACTERISTICS

Conditions (applies to all graphs unless stated otherwise): V_I = 12 V, I_O = 12 A load, Co = 500 µF

Efficiency



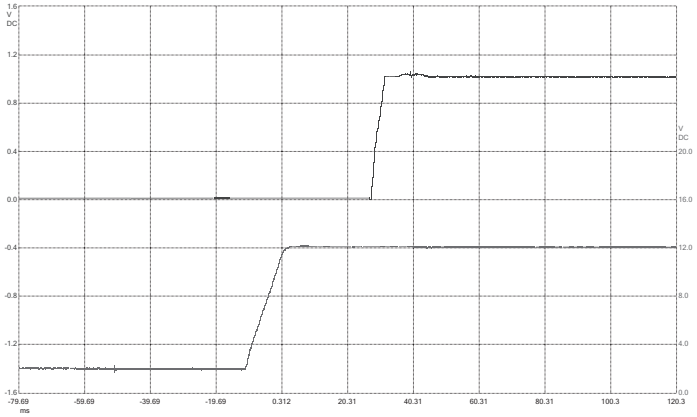
Output Load Transient Response



Current step-change (3-9-3 A)
Top Trace: Load Current
Slew Rate: (1A/µs)

Bottom Trace: Output Voltage (20 mV /div)
Time Scale: (200 µs / div)

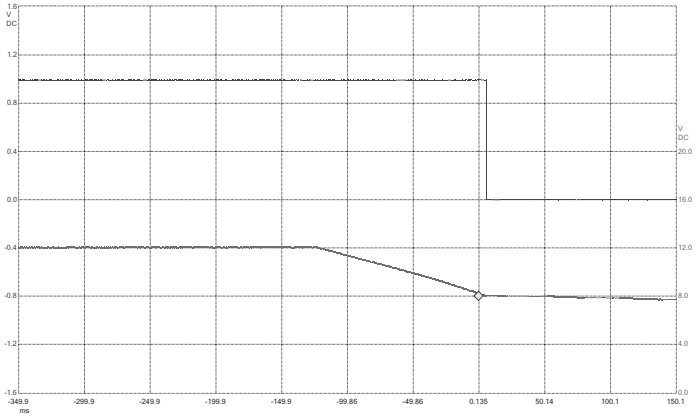
Start-up



Top Trace: Output Voltage (400 mV / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (20 ms / div)

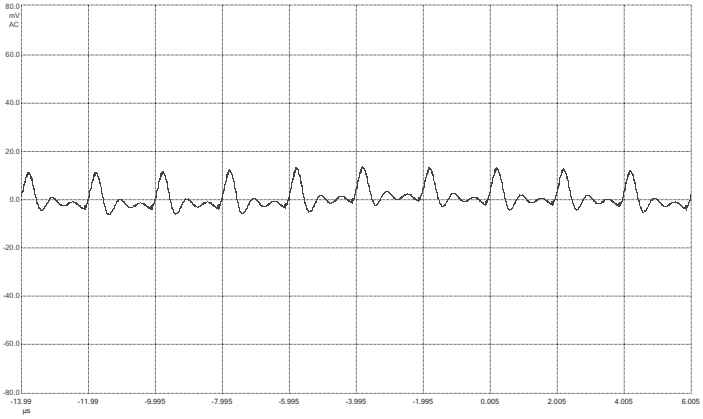
Shut-down



Top Trace: Output Voltage (400 mV / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (50 ms / div)

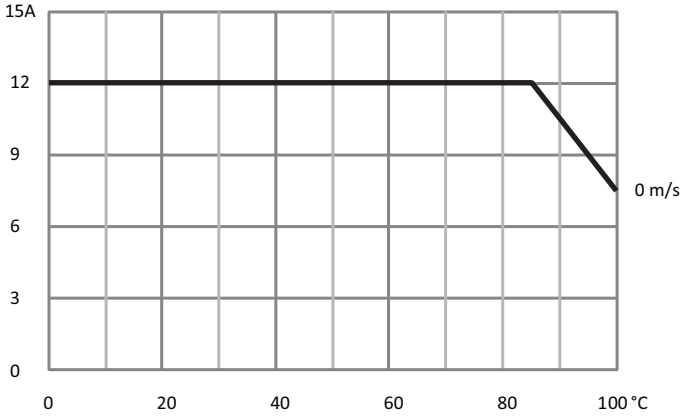
Output Ripple and Noise



Trace: Output Voltage (20 mV / div)

Time Scale: (2 µs / div)

Output Current Derating



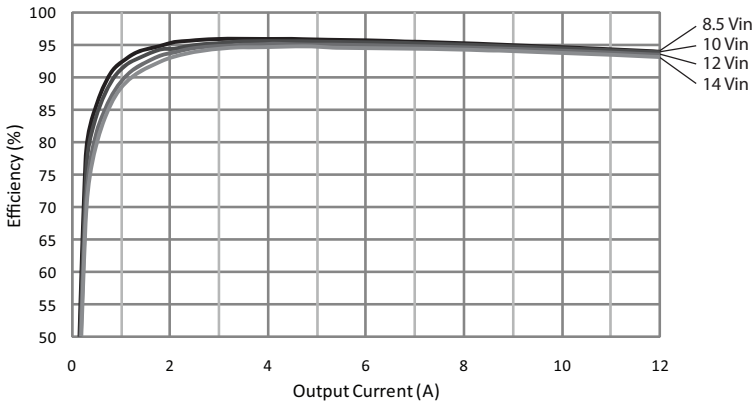
Vi=12V, modules mounted on a 6" X 4", 2 oz, 6-Layer test board

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

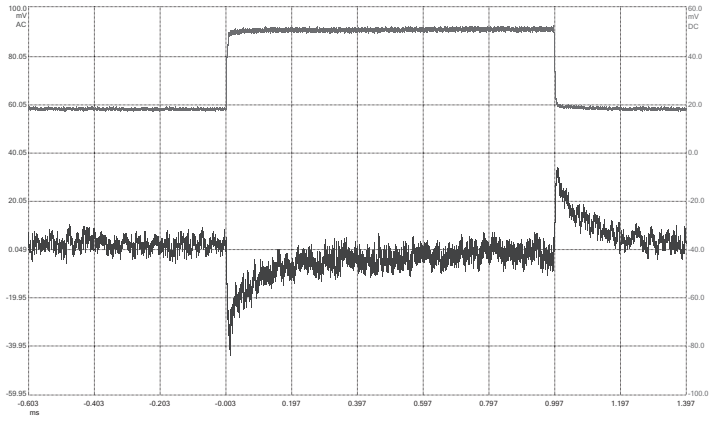
2.5V / 12A TYPICAL CHARACTERISTICS

Conditions (applies to all graphs unless stated otherwise): V_I = 12 V, I_O = 12 A load, Co = 500 µF

Efficiency



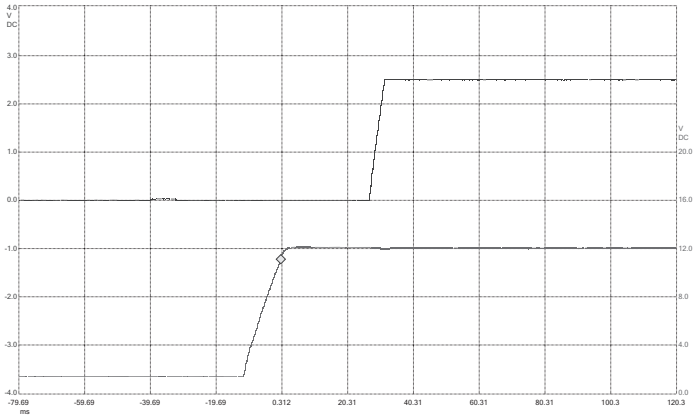
Output Load Transient Response



Current step-change (3-9-3 A)
Top Trace: Load Current
Slew Rate: (1A/µs)

Bottom Trace: Output Voltage (20 mV /div)
Time Scale: (200 µs / div)

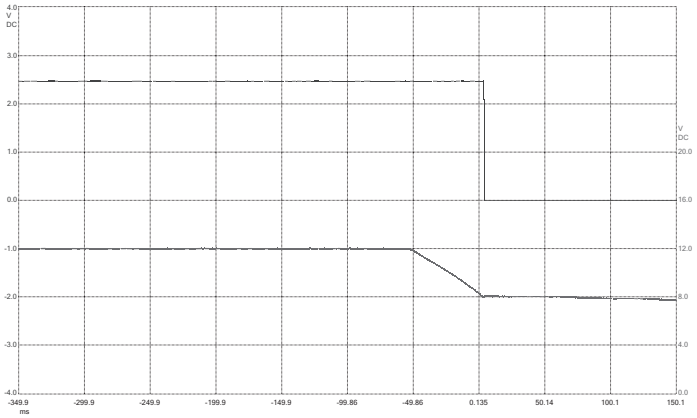
Start-up



Top Trace: Output Voltage (1.0 V / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (20 ms / div)

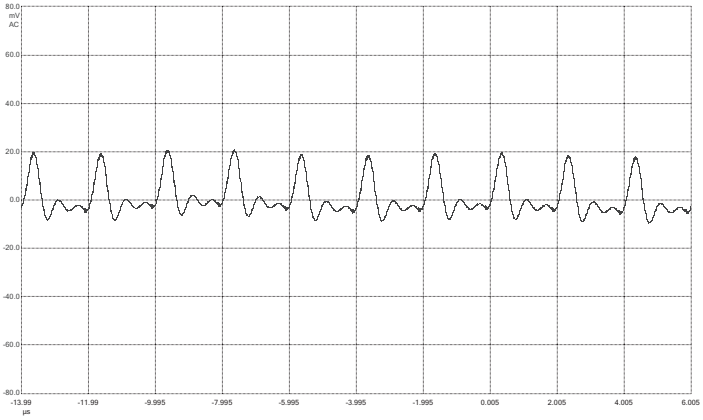
Shut-down



Top Trace: Output Voltage (1.0 V / div)
Bottom Trace: Input Voltage (4 V / div)

Time Scale: (20 ms / div)

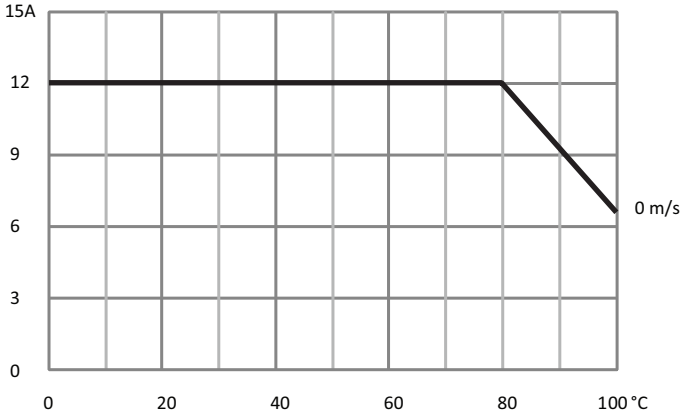
Output Ripple and Noise



Trace: Output Voltage (20 mV / div)

Time Scale: (2 µs / div)

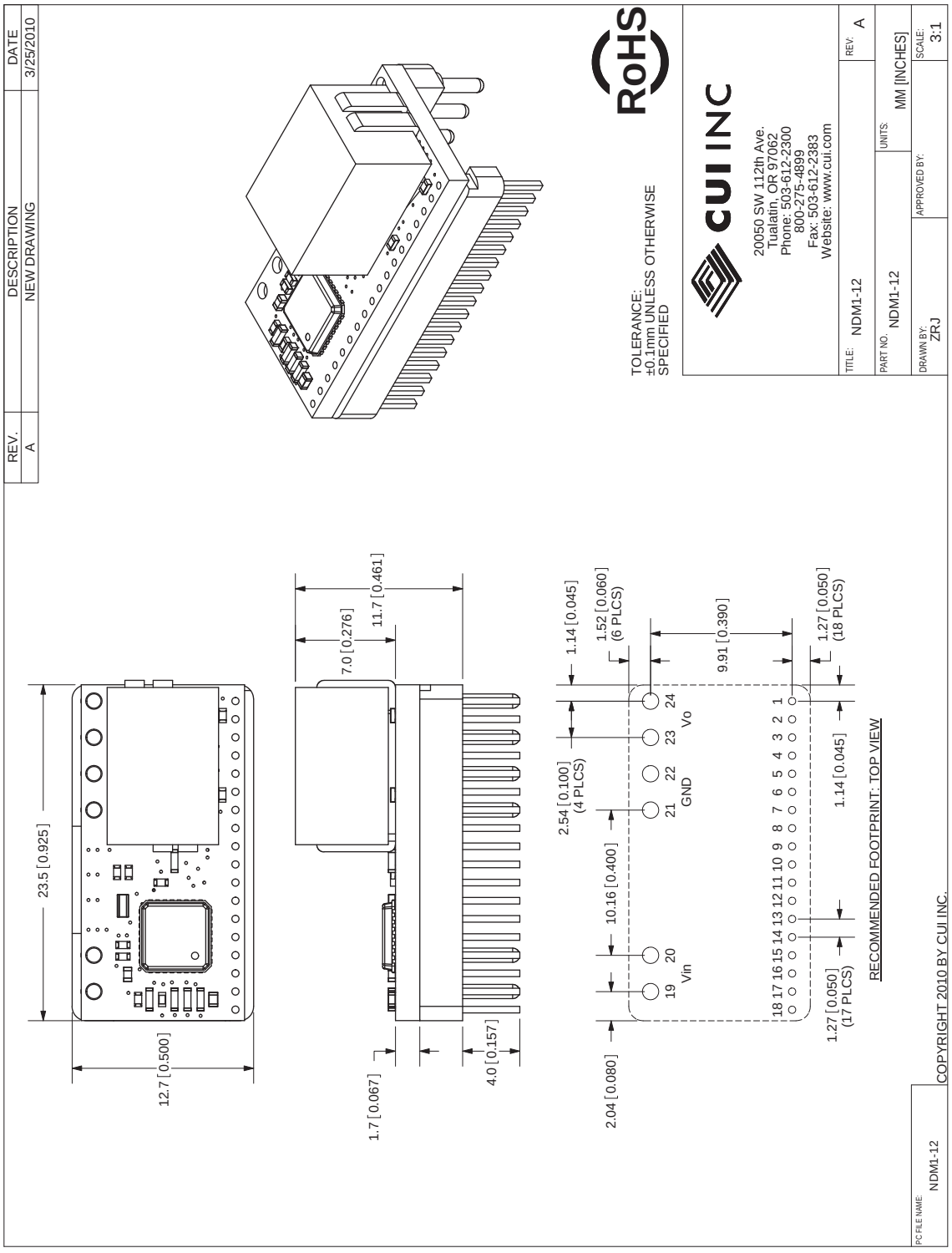
Output Current Derating



Vi=12V, modules mounted on a 6" X 4", 2 oz, 6-Layer test board

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

MECHANICAL DRAWING (THROUGH-HOLE)



MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

OPERATING INFORMATION - POWER MANAGEMENT

INPUT FILTERING

The NDM1-12 module has built-in capacitances to supply the pulsed current due to PWM switching. However, to help minimize input voltage ripples, additional input capacitance is recommended as follows: 1x 330µF POSCAP or electrolytic and 3x 22µF ceramic capacitors, placed as close as possible to the input pins. (see Figure 1) If large, long-term load transients are present, additional bulk capacitances are recommended, such as a 1000µF low-ESR electrolytic or OSCON.

OUTPUT CAPACITANCE

The amount of output capacitance required depends on the output ripple and noise requirements and transient performance, even though the NDM1-12 POL module does not require output capacitance for low noise operations. As good starting point is 5x100µF ceramic. (see Figure 1) These capacitors should be placed as close to the load as possible. Additional high frequency capacitors can be placed next to the load to improve transient performance at the load.

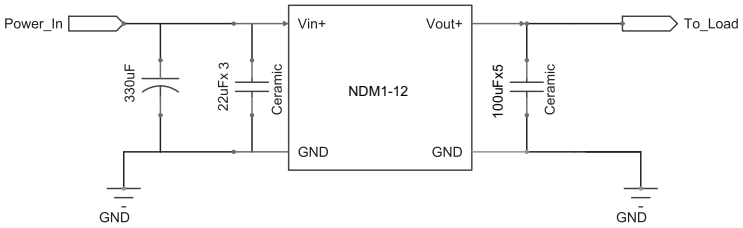


Figure 1: Recommended Circuit

AUTO-CONTROL™

The NDM1-12 utilizes an Auto-Control™ algorithm to achieve stability and optimal transient response. There is no need for any external compensation, as the algorithm automatically takes into account the input voltage, output voltage, load current conditions, and output capacitance. Auto-control™ achieves this by constantly monitoring the regulated output voltage on a cycle-by-cycle basis and adjusting the parameters of the controller to optimize the regulation. As the control algorithm takes into account all variations in the power stage, including operating conditions, component variations and component aging, the control loop can maintain high gain up to as high a bandwidth as stability will allow, resulting in highest loop performance without sacrificing stability. The default algorithm is configured for balanced ripple and noise and transient response. The algorithm can be customized for better ripple and noise or faster transient response.

Auto-Control™ performance can be observed during operation in the Demo tab of the V-Infinity Intelligence Center GUI. As the regulation of a DC-DC converter varies with load current, transient load step, amount of bulk capacitance, inductor value etc.; so Auto-Control™ varies also to optimize the regulation.

The user has the ability to set the optimization goal of the Auto-Control™ algorithm in the V-Infinity Intelligence Center GUI. This is available on the GUI Demo tab under “Optimization Factor”. Nine settings are available, with 1 corresponding to the least aggressive optimization, ideal for low ripple, and 9 corresponding to the most aggressive optimization, ideal for fast transient response. The module defaults to 5, and this is ideal for the majority of applications where a good balance of noise and transient response is desired.

Auto-Control™ also offers Quiet Mode and high ESR Output Cap Optimization Mode options to achieve different design goals.

Quiet Mode
When Quiet Mode is turned on the module is always tuned to achieve the best regulation. Auto-Control™ will tune to a low value to give a low loop bandwidth, minimizing the amplification of wide band noise resulting in the lowest output deviation.

When Quiet Mode is turned off the module is always tuned to achieve the best transient response. This means that during load transients the module will tune to a high Auto-Control™ value to give the highest loop bandwidth and lowest sensitivity. When there is no transient disturbance and the output voltage consists mainly of wide bandwidth noise the module keeps Auto-Control™ at a suitable value so that transient bursts are well regulated. This may increase the observed ripple during steady state load.

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

High ESR Output Cap Optimization Mode
Auto-Control™ automatically tunes for a wide range of capacitor values and types including low ESR MLCC, with High ESR Output Cap Optimization Mode set to LOW. However, even further improvements are possible for capacitor types where the ESR zero is significant, by setting the High ESR Output Cap Optimization Mode to HIGH. Beware that selecting High ESR Output Cap Optimization Mode HIGH when only MLC capacitors are employed may result in low level oscillation. By default high ESR output cap optimization Mode is set to OFF.

Auto-Control™ Technology Advantages

- Robust reliable control. Impervious to variations in components and the application context.
- Optimized higher performance control. Significantly improves transient performance and reduces the number of decoupling capacitors required in the end application.
- Enables the use of lower cost (poorer tolerance components) without risking stability.

REMOTE SENSING

In general, the load distribution circuit should have minimal impedance due to the large load current, to help achieve good regulation and low distribution loss. If needed, remote sensing can be implemented to improve regulation and transient response. Connect the +Sense and –Sense pins to the +Vout and –Vout points where regulation is needed, through two separate differential pair traces.

OUTPUT ON/OFF CONTROL

By default, the device is configured to be always on without on/off control. The output of NDM1-12 can be turn on and off through the CTRL pin. Either positive or negative logic can be configured. With positive logic, the module will be turned on with a logic high on the CTRL pin, and turned off with a logic low signal. Negative logic is just the opposite. The device can also be configured to be always on without on/off control, which is the default device setting. The CTRL pin can also be used to allow for sequencing (see OUTPUT VOLTAGE SEQUENCING).

POWERGOOD SIGNAL

The NDM1-12 module provides a PG signal to indicate the status of normal operations. It is an open collector signal that requires a pull up resistor to a 3.3V line. It goes high when the output voltage is within regulation, and automatically adjusts for different output voltages. It goes low whenever the output voltage is out of regulation is such cases as over-current , over temperature or input under voltage.

STARTUP WITH PRE-BIAS

The NDM1-12 allows a power-up into a Pre-bias condition. A Pre-bias condition happens when a voltage is present on the output of the power converter before it is enabled.

The converter starts its ramp following the predefined power-up sequence (delay and ramp). When the reference voltage reaches the Pre-bias voltage level, the PWM output is enabled.

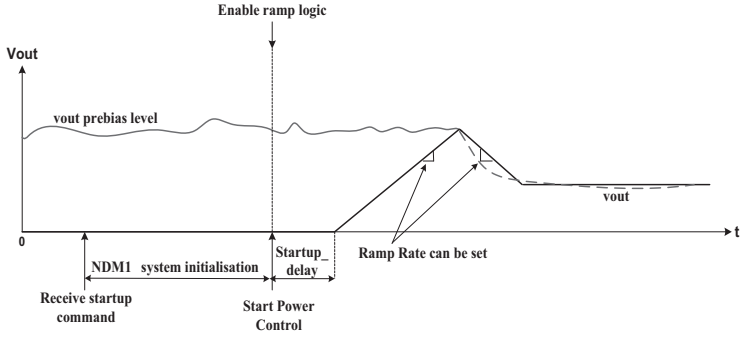


Figure 2: Pre-bias is greater than Vout

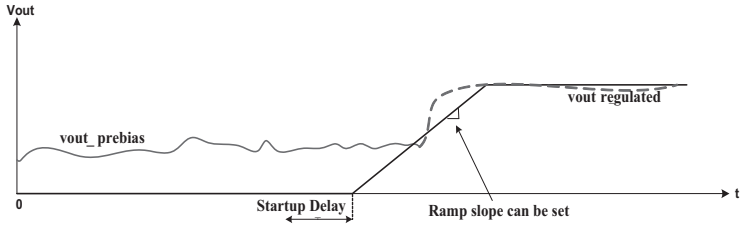


Figure 3: Pre-bias is less than Vout

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

SYNC FUNCTION

The NDM1-12 module achieved voltage regulation thru digital pulse width modulation (DPWM). A synchronization method is provided where multiple slave devices are controlled by a single master device via open loop phase alignment of the PWM patterns.

The DPWM synchronization allows the timing of the pulse width modulation to be aligned between the master and slave(s) at the same switching frequency rate. The DPWM synchronization will prevent the devices from drifting from each other with respect to the start of the pulse width modulation. By default the slave phase shift is 180˚ from the master.

Figure 4 illustrates the connectivity of the SYNC signal for the case where two slave devices are used in a master/slave configuration. This case shows the example where several NDM1-12 modules are used to control various voltage rails at the same switching frequency. DPWM synchronization ensures that the starting points of each slaves PWM patterns are under the control of the designated master device and that the master and slave on-chip oscillators are frequency locked to within a certain error margin.

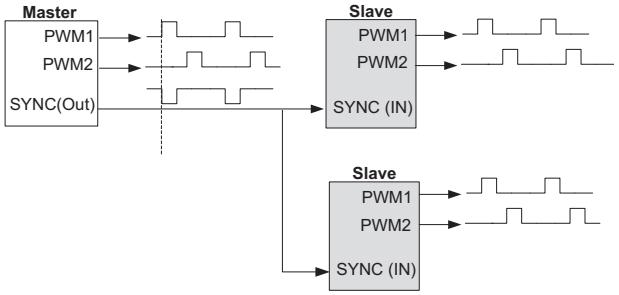


Figure 4: Block Diagram of Master-Slave Synchronization Connection

The slave device will check for slow and fast arriving SYNC pulses and flag the error condition if enabled. An error condition will cause an exit from master-slave synchronization, resulting in the slave returning to free-running PWM generation which is not aligned to the master. The slave will again begin the synchronization process. After all three stages of the synchronization process are completed, the slave PWM will again be synchronized to the master.

OUTPUT VOLTAGE TRIMMING

As a digital POL module, the NDM1-12 module can be programmed via PMBus command to different output voltages without any hardware circuit board modifications. The output voltage can also be trimmed at the factory or via the V-Infinity GUI and stored in non-volatile memory in the NDM1-12 module.

STARTUP DELAY AND RAMP UP TIME

POL startup delay and startup ramp up rate are adjustable through GUI or PMBus commands. The startup delay range is 0mS to 1048mS. The default set up is 0mS. Ramp up rate ranges from 2.6V/mS to 10.13mV/mS. Ramp up is monolithic and default set up is 1V/mS.

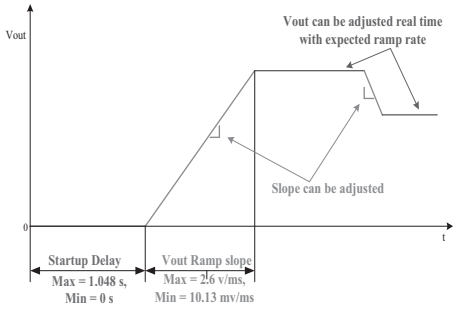


Figure 5: Adjustable range of startup delay and ramp up rate.

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OUTPUT VOLTAGE SEQUENCING

The NDM1-12 can be configured to achieve advanced voltage sequencing between power rails. This capability eliminates the need for additional power management circuitry, in a system environment with multiple voltage domains. Ensuring consistent and predictable start-up of multiple voltage rails after power-on or power system reset (due to power outage or fault condition) prevents catastrophic and unpredictable current flows through digital processors and other loads served.

Coordination of voltage rails and predictable shutdown under fault conditions reduces the risk of unpredictable system behavior where a problem occurs with one of the voltage rails in a system application.

Programmable power-on sequencing delays may also be used to ensure certain voltage rails are stabilized before energizing mission critical functions.

A recommended configuration for multiple module systems is shown in figure 6 where the control signal is used to initiate sequencing during normal operations and the FAULT signal is used for fault management. Before the load systems are connected, it is necessary to program the ON Rise Time, On Time Delay, and OFF Time Delay for each module. This can be easily accomplished using the V-Infinity GUI which is the ideal tool to program and fine tune these parameters during development. In the Basic tab of the Configure section of the GUI the ON Rise Time, On Time Delay, and OFF Time Delay can all be independently set to meet system requirements. Either positive or negative logic of the CONTROL pin can be configured as required. Figure 7 illustrated the timing diagram for normal sequencing.

Upon assertion of the CONTROL pin the ON Time Delay begins. The output voltage will begin to rise after the ON Time Delay is over. The output voltage will rise monotonically until reaching regulation. The amount of time to reach regulation from the end of the ON Time Delay is the On Rise Time. When the CONTROL pin becomes unasserted the OFF Time Delay begins and the output voltage will remain regulated until this delay is over. The voltage ramp during turn-off is not controlled by the module, but by the load current as it discharges the output capacitance. Once the system designer is satisfied with the timing sequence, the timing parameters can be permanently stored in the non-volatile memory of the module.

For fault management, the FAULT pin of each module can be tied together so that if there is a fault (Over Voltage, Over Current, Input Under Voltage, or Temperature) on any module in the system all units will shut down immediately and remain off until the fault condition is removed. The turn-off delays are ignored in a fault condition and there is no ramp down control.

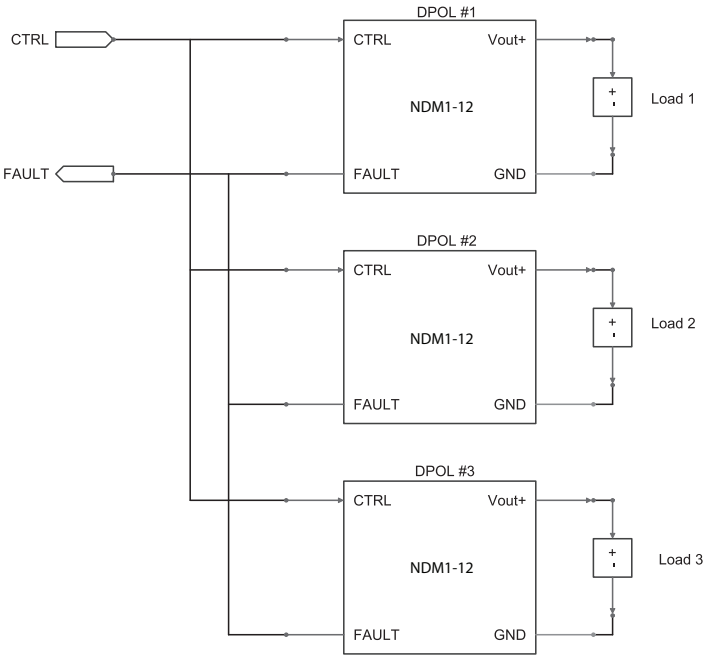

Figure 6: Multiple Module Configuration

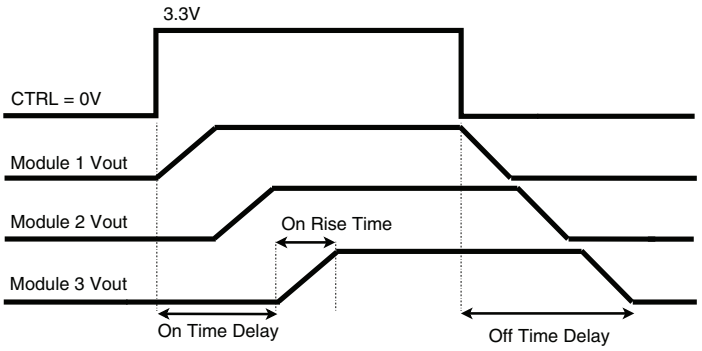

Figure 7: Timing Diagram

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MARGINING

During test and development, it is often required to vary the output voltage around its target set point in order to determine whether the load can operate over a specified supply voltage range (Figure 8)

The NDM1-12 provides the ability to set the output voltage at a predefined higher or lower value around the target set point. The Margin limit can be set through the GUI or PMBus command. The output can be commanded to switch between the High value, Nominal or Low value as a percentage of the nominal value. The range can be set ±20% of the nominal target output voltage value.

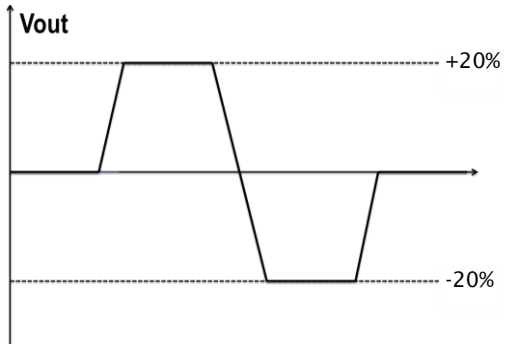

Figure 8: Voltage Margining

POWER FAULT MANAGEMENT

NDM1-12 supports the following fault conditions:

- Input undervoltage lockout (UVLO).
- Output overvoltage protection (OVP).
- Output over current protection (OCP).
- Over temperature protection (OTP)

INPUT UNDERVOLTAGE LOCKOUT (UVLO)

A UVLO condition inhibits the output while the input voltage is below the programmed threshold. The output of the NDM1-12 will not turn on until the input voltage exceeds the Vin UVLO Turn-On Threshold and will turn off if the input voltage falls below the Vin UVLO Turn-Off Threshold. The supported UVLO threshold range can be programmed via PMBus from 8.5V to 14V.

In the continuous presence of a UVLO fault the controller will make an infinite number of attempts to re-start power control with no relaxation time between attempts, allowing very fast system response once the UVLO fault condition clears.

OUTPUT OVERVOLTAGE PROTECTION (OVP)

The NDM1-12 offers output overvoltage protection to protect load circuitry from being subjected to a voltage higher than its electrical specifications (limits).

The output of the NDM1-12 module will be turned off and device will enter an OVP fault state when the output voltage exceeds the pre-programmed OVP threshold for a time greater than the pre-programmed hysteresis delay.

The module enters a hiccup mode and attempts to restart every 250ms. A maximum number of 8 OVP restart attempts every 250ms are made. Thereafter an infinite number of re-start attempts are made every 1 minute. It will recover automatically when the output voltage is reduced to less than the OVP limit.

A maximum number of 8 OVP restart attempts every 250ms are made. Thereafter an infinite number of re-start attempts are made every 1 minute.

OUTPUT OVERCURRENT PROTECTION (OCP)

The device will enter an OCP fault state and the output of the NDM1-12 module will be turned off if the load current is 15-20% over the nominal load current. The module enters a hiccup mode and attempts to restart every 250ms. It will recover automatically when the load current is reduced to less than the OCP limit. The OCP threshold level can be programmed via GUI or PMBUS

OUTPUT LETHAL CURRENT PROTECTION (LCP)

The NDM1-12 offers fast (through analog sense circuits) output overcurrent protection in the event of overload conditions or short circuit between the output voltage nodes (SENSE+) and ground (SENSE-) over and above standard OCP.

The device will enter an LCP fault state when the output current rises above a pre-programmed LCP threshold. The LCP threshold level can only be programmed through the PMBus. The LCP response time is on the order of 250 ns and must be 2x the OCP threshold.

In the case of an LCP fault the device will make an infinite number of attempts to re-start power control with a relaxation time of 250 ms between attempts.

OVER TEMPERATURE PROTECTION (OTP)

The NDM1-12 offers thermal protection through its on-chip temperature sensor. The device will respond to the OTP fault by forcing the PWM1 signal from the controller to enter tri-state, immediately disabling power control. In the continuous presence of an OTP fault, the device will make an infinite number of attempts to re-start power control with a relaxation time of 250 ms between attempts. It recovers automatically when the module temperature is cooled down by 20˚C.

CONFIGURATION INPUTS

The NDM1-12 is equipped with a number of configuration inputs. These inputs can be used to configure a NDM1-12 if serial communication is not available. External configuration resistors are connected to the configuration inputs. If no external configuration resistors are detected, the NDM1-12 remains at factory default configuration. Device settings determined by configuration inputs can be modified through serial communication during normal operation. NDM1-12 configuration settings are determined in the sequence shown in Figure 9.

Configuration resistors are determined during the NDM1-12 start-up process only. Once a NDM1-12 has completed its start-up sequence, the configuration resistors are ignored (until the next start-up).

Device settings determined through configuration resistors may be overwritten subsequently through serial communication during normal operation.

The following configuration inputs are available
- ADDR1 and ADDR2
- VSET

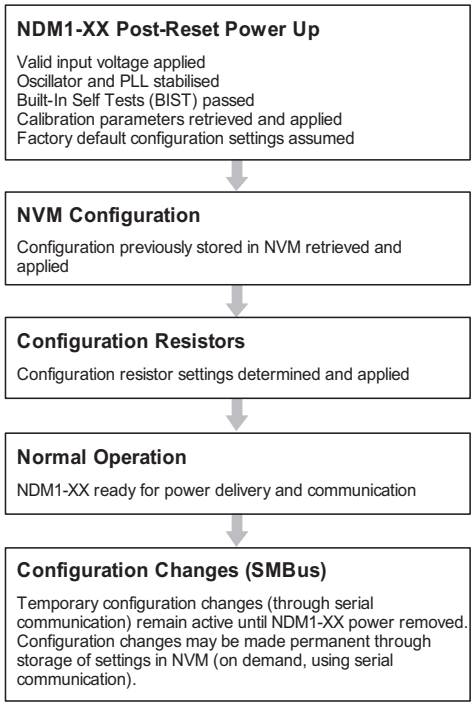

Figure 9: Device start-up and configuration

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CONFIGURATION USING DOWN RESISTORS

Configuration inputs ADDR1 and ADDR2 are used to assign an initial SMBus address to a device. In small-scale systems with up to 16 NDM1-12 devices, only one of the address inputs is required (ADDR1).

All configuration resistors (with the exception of VSET) should be selected from the standard E12 (or higher) series, with 1% tolerance, and 100ppm temperature coefficient. Configuration resistors should be connected to the configuration inputs, and grounded to the CRC pin, as illustrated in Figure 10. For all functions except VSET, sixteen distinct values of configuration resistors are detected (including short [0Ω] to CRC, or floating input). For VSET any value of resistance ranging from 6.2kΩ..68kΩ (outside any standard resistance series) may be used to choose the desired output voltage set-point.

Configuration input readings are filtered internally by the NDM1-12. In addition to this, noisy environments may require the connection of a small filter capacitance (100pF) in parallel with the configuration resistors.

The current injected into the configuration resistors is small (10µA typ.), resulting in negligible power dissipation and ground currents.

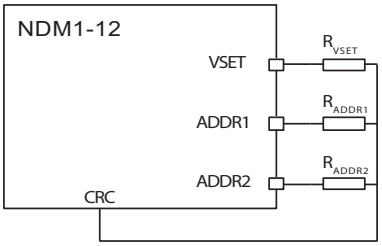

Figure 10: Configuration inputs

CONFIGURATION INPUT VSET

Configuration input VSET can be used to configure the output voltage set-point, as well as initial behavior of control pin CTRL. Resistor RVSET can be chosen in a continuous range from 0kΩ..100kΩ but NDM1-12 output voltage restrictions (documented elsewhere) limit the useful RVSET range to approximately 8.2kΩ..47KΩ. The resulting output voltage can be determined by the following equation:

$$Vout_{setpoint} = \frac{R_{VSET}}{18.75K\Omega} \cdot 1V$$

and is valid for all values of RVSET except for cases where pin VSET is shorted to CRC (or RVSET<10Ω or VSET is floating (or RVSET>90kΩ). For both of these two special cases of RVSET (shorted to CRC, or floating) the output voltage set-point will remain at the factory default level of 0.6V. This relationship is shown in Figure 11.

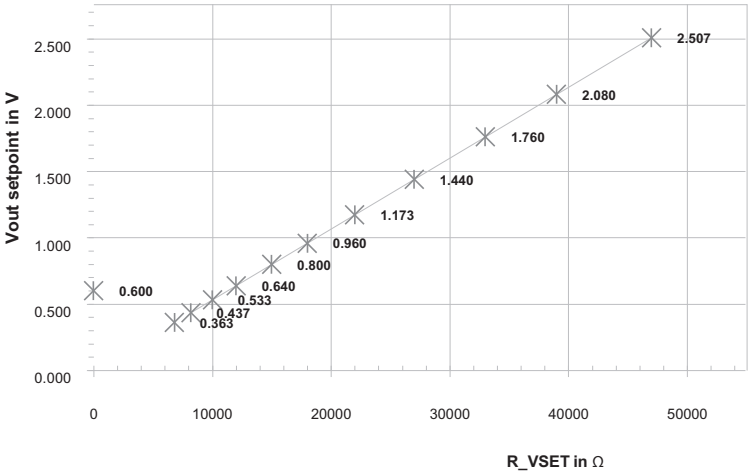

Figure 11: R VSET versus Output Voltage

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CONFIGURATION INPUTS ADDR1 AND ADDR2

Configuration inputs ADDR1 and ADDR2 are used to assign an initial SMBus address to a NDM1-12 slave device. Unique device addresses are required in systems where multiple SMBus devices are connected through serial interface lines SDA (SMBus data) and SCL (SMBus clock). Bus conflicts will occur if more than one device responds to the same SMBus address.

If serial communication is not required, or the factory-default SMBus address of 16 decimal (or 0x10) is acceptable, both inputs ADDR1 and ADDR2 may be left floating. In smaller-scale systems with up to sixteen NDM1-12 slave devices it is sufficient to utilize ADDR1 only (while ADDR2 is shorted to CRC). In this case, SMBus addresses 16..31 (0x10..0x1F) can be assigned through RADDR1. In larger-scale systems both RADDR1 and RADDR2 can be used, in which case any SMBus address in the range 16..127 (0x10..0x7F) can be assigned to the device.

Note that a number of SMBus addresses in the address range 0..15 are reserved for special purposes (e.g. SMBus Alert Response, SMBus Host). SMBus addresses in the range 0..15 should be avoided, and cannot be assigned through ADDR1 and ADDR2 configuration inputs.

If RADDR2 is not used (and ADDR2 is connected to CRC), the effective SMBus address is

$$ADDR_{SMBus} = 16 + index(R_{ADDR1}) \text{ with } index(R_{ADDR1}) = 0..15$$

If both RADDR1 and RADDR2 are used, the effective SMBus address is

$$ADDR_{SMBus} = 16\,(1+index(R_{ADDR2})) + index(R_{ADDR1}) \text{ with } index\,(R_{ADDR2}) = 0..6$$

Table 1 offers a summary of assigned SMBus addresses as a function of RADDR1 and RADDR2.

R_{ADDR1} in kΩ	R_{ADDR2} in kΩ																
	0 index 0	6.8 index 1	8.2 index 2	10 index 3	12 index 4	15 index 5	18 index 6	22 index 7	27 index 8	33 index 9	39 index 10	47 index 11	56 index 12	68 index 13	82 index 14	100 index 15
0 index 0	16	32	48	64	80	96	112	16	16	16	16	16	16	16	16	16
6.8 index 1	17	33	49	65	81	97	113	17	17	17	17	17	17	17	17	17
8.2 index 2	18	34	50	66	82	98	114	18	18	18	18	18	18	18	18	18
10 index 3	19	35	51	67	83	99	115	19	19	19	19	19	19	19	19	19
12 index 4	20	36	52	68	84	100	116	20	20	20	20	20	20	20	20	20
15 index 5	21	37	53	69	85	101	117	21	21	21	21	21	21	21	21	21
18 index 6	22	38	54	70	86	102	118	22	22	22	22	22	22	22	22	22
22 index 7	23	39	55	71	87	103	119	23	23	23	23	23	23	23	23	23
27 index 8	24	40	56	72	88	104	120	24	24	24	24	24	24	24	24	24
33 index 9	25	41	57	73	89	105	121	25	25	25	25	25	25	25	25	25
39 index 10	26	42	58	74	90	106	122	26	26	26	26	26	26	26	26	26
47 index 11	27	43	59	75	91	107	123	27	27	27	27	27	27	27	27	27
56 index 12	28	44	60	76	92	108	124	28	28	28	28	28	28	28	28	28
68 index 13	29	45	61	77	93	109	125	29	29	29	29	29	29	29	29	29
82 index 14	30	46	62	78	94	110	126	30	30	30	30	30	30	30	30	30
100 index 15	31	47	63	79	95	111	127	16	16	16	16	16	16	16	16	16

Table 1: Assigned (decimal) SMBus address as a function of R_{ADDR1} and R_{ADDR2}

Note: Addresses are represented in hexadecimal in the GUI

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SUPPORTED PMBUS COMMANDS

FUNCTIONALITY	COMMAND CODE	COMMAND NAME	DESCRIPTION
On, Off and Margin Testing	01h	OPERATION	Turn the unit on and off from the CONTROL pin
On, Off and Margin Testing	02h	ON_OFF_CONFIG	Configures CONTROL pin & serial bus commands needed to turn the unit on and off
Fault Management	03h	CLEAR_FAULTS	Clear any fault bits that have been set
Set Output Voltage	20h	VOUT_MODE	Use linear output voltage setting
Set Output Voltage	21h	VOUT_COMMAND	Can use external resistor divider V0>2.5V
Vout Margin	25h	VOUT_MARGIN_HIGH	Can be done through VOUT_COMMAND
Vout Margin	26h	VOUT_MARGIN_LOW	Can be done through VOUT_COMMAND
Set Output Voltage	27h	VOUT_TRANSITION_RATE	Shall be the same as soft-start rate
Input Under Voltage	35h	VIN_ON	Literal format: Fixed voltage divider for 12 V op
Input Under Voltage	36h	VIN_OFF	Literal format: Fixed voltage divider for 12 V op
Fault Management	40h	VOUT_OV_FAULT_LIMIT	Over voltage protection
Fault Management	46h	IOUT_OC_FAULT_LIMIT	Set current limit
Fault Management	4Fh	OT_FAULT_LIMIT	Over-temperature fault limit. Had default value
Vout Sequencing	60h	TON_DELAY	Time from enable to output ramp starting
Vout Sequencing	61h	TON_RISE	The time from when the output starts to rise until the voltage entered the regulation band
Vout Sequencing	64h	TOFF_DELAY	The time from a stop condition is received until stops transferring energy to the output
Status	78h	STATUS_BYTE	Returns one byte of information with a summary of the most critical faults
Status	79h	STATUS_WORD	Returns two bytes of information with a summary of the unit's fault condition
Telemetry	88h	READ_VIN	Reurns the input voltage in volts
Telemetry	8Bh	READ_VOUT	The actual, measured output voltage in the same format as set by the VOUT-MODE
Telemetry	8Ch	READ_IOUT	The measured output current in amperes
Telemetry	8Dh	READ_TEMPERATURE1	temperature readings can be returned for each device
Telemetry	94h	READ_DUTY_CYCLE	The duty of PMBus device's main converter in %

Table 2: Supported PMBus commands

THROUGH-HOLE SOLDERING INFORMATION

To ensure module performance and reliability, adherence to IPC-A-610D standards for solder joint acceptability is recommended.

The NDM1-12 module is designed for RoHS compliant plated through hole mounting by wave or manual soldering. The recommended pot temperature is a maximum 270ºC with a maximum dwell time of 10 seconds. A maximum preheat temperature of 150ºC with a preheat rate of 3ºC/s is suggested.

To prevent damage to the module during manual soldering, special attention should be taken to avoid direct contact between the hot soldering iron tip and the pins for longer than 3 seconds.

MODEL: NDM1-12-120 **DESCRIPTION: NON-ISOLATED DIGITAL DC-DC POL CONVERTER**

REVISION HISTORY

rev.	description	date
A	initial release	10/12/2010