HCPL-M454

Ultra High CMR, Small Outline, 5 Lead, High Speed Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-M454 is similar to Avago's other high speed transistor output optocouplers, but with shorter propagation delays and higher CTR. The HCPL-M454 also has a guaranteed propagation delay difference (t_{PLH} - t_{PHL}). These features make the HCPL-M454 an excellent solution to IPM inverter dead time and other switching problems.

The HCPL-M454 CTR, propagation delays, and CMR are specified both for TTL load and drive conditions and for IPM (Intelligent Power Module) load and drive conditions. Specifications and typical performance plots for both TTL and IPM conditions are provided for ease of application.

This diode-transistor optocoupler uses an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional

Applications

- Inverter Circuits and Intelligent Power Module (IPM) Interfacing: Shorter propagation delays and guaranteed (t_{PLH} - t_{PHL}) specifications. (See power inverter dead time section)
- High speed logic ground isolation: TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- Line Receivers: High common mode transient immunity (>15 kV/µs for a TTL load/drive) and low input-output capacitance (0.6 pF)
- Replace pulse transformers: ave board space and weight
- Analog signal ground isolation: Integrated photon detector provides improved linearity over phototransistors

Features

- Function compatible with HCPL-4504
- Surface mountable
- Very small, low profile JEDEC registered package outline
- Compatible with infrared vapor phase reflow and wave soldering processes
- Short propagation delays for TTL and IPM applications
- Very high common mode transient immunity: Guaranteed 15 kV/µs at V_{CM} = 1500 V
- High CTR: >25% at 25°C
- Guaranteed specifications for common IPM applications
- TTL compatible
- Guaranteed ac and dc performance over temperature: 0°C to 70°C
- Open collector output
- Safety approval:

  UL Recognized 3750 Vac / 1 min. per UL 1577

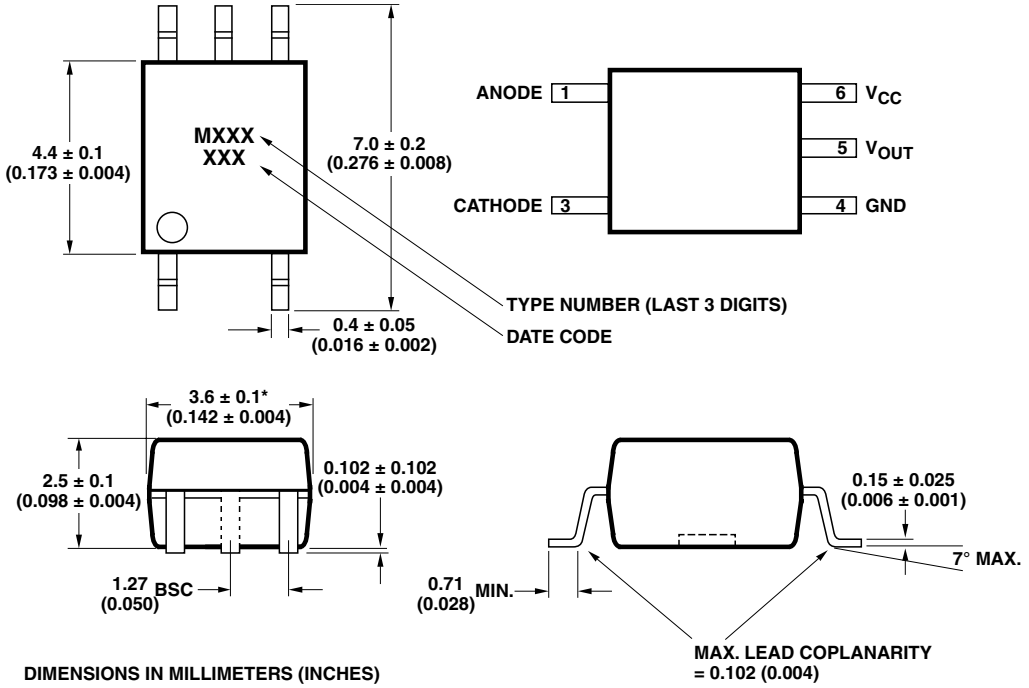
  IEC/EN/DIN EN 60747-5-2

  Approved V_{IORM} = 560 Vpeak for Option 060.

  CSA Approved
- Lead free option "-000E"

CAUTION: *The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Outline Drawing (JEDEC MO-155)



DIMENSIONS IN MILLIMETERS (INCHES)

* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Ordering Information

HCPL-M454 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option: RoHS Compliant	Option: non RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
HCPL-M454	-000E	no option	SO-5	X			100 per tube
	-500E	#500		X	X		1500 per reel
	-060E	-060		X		X	100 per tube
	-560E	-560		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-M454-560E to order product of SO-5 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and RoHS compliant.

Example 2:

HCPL-M454 to order product of SO-5 Surface Mount package inTube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

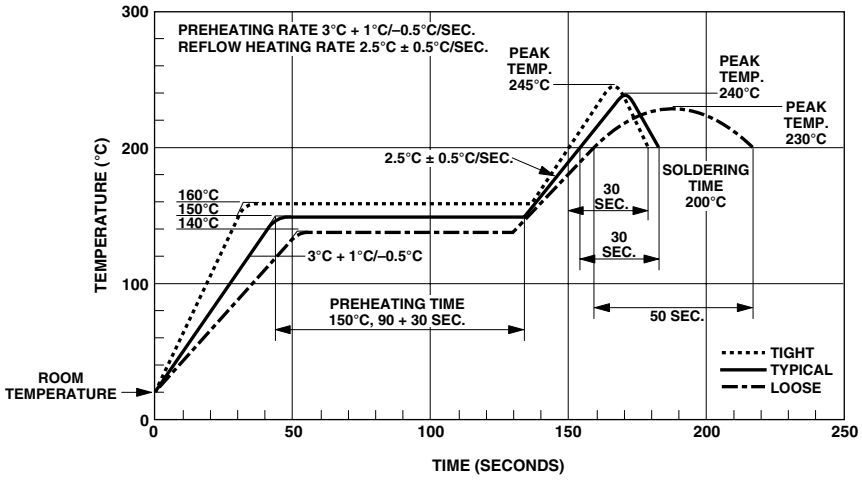
Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

Absolute Maximum Ratings

(No Derating Required up to 85°C)

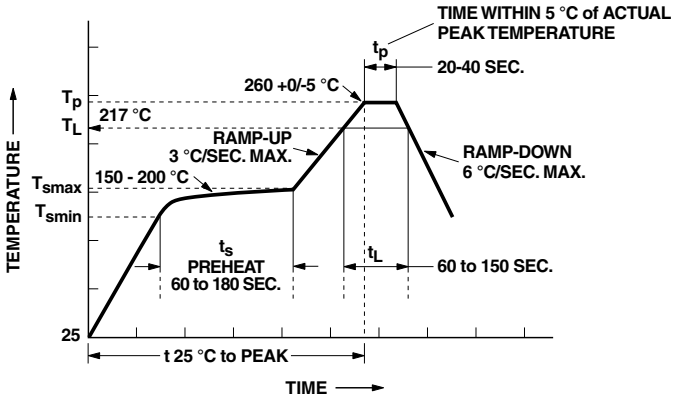
Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to +100°C
Average Input Current - I_F ..... 25 mA[1]
Peak Input Current - I_F ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current - I_F ..... 1.0 A
(≤1 µs pulse width, 300 pps)
Reverse Input Voltage - V_R (Pin 3-1) ..... 5 V
Input Power Dissipation ..... 45 mW[3]
Average Output Current - I_O (Pin 5) ..... 8 mA
Peak Output Current ..... 16 mA
Output Voltage - V_O (Pin 5-4) ..... -0.5 V to 20 V
Supply Voltage - V_{CC} (Pin 6-4) ..... -0.5 V to 30 V
Output Power Dissipation ..... 100 mW[4]
Infrared and Vapor Phase Reflow Temperature ..... see below

Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

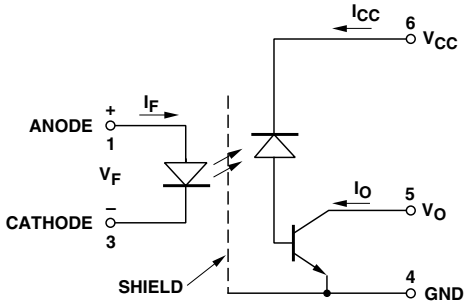
Recommended Pb-Free IR Profile



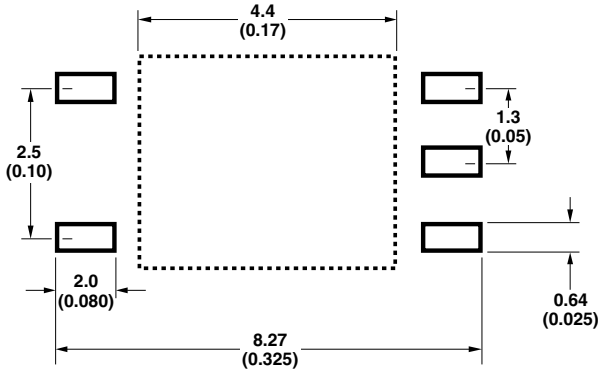
NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Schematic



Land Pattern Recommendation



DIMENSION IN MILLIMETERS (INCHES)

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(IO1)	≥ 5	mm	Measured from input terminals to output terminals
Minimum External Tracking Path (Creepage)	L(IO2)	≥ 5	mm	Measured from input terminals to output terminals
Minimum Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

DC Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 11)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	25	32	60	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA	1,2,4	5
		21	34				V_O = 0.5 V	V_{CC} = 4.5 V		
Current Transfer Ratio	CTR	26	35	65	%	T_A = 25°C	V_O = 0.4 V	I_F = 12 mA	1,2,4	5
		22	37				V_O = 0.5 V	V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}		0.2	0.4	V	T_A = 25°C	I_O = 3.0 mA	I_F = 16 mA		
			0.2	0.5			I_O = 2.4 mA	V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	5	
			0.01	1.0		T_A = 25°C	V_O = V_{CC} = 15 V			
				50						
Logic Low Supply Current	I_{CCL}		50	200	µA	I_F = 16 mA	V_{CC} = 15 V	V_O = open		11
Logic High Supply Current	I_{CCH}		0.02	1	µA	T_A = 25°C	I_F = 0 mA V_O = open	V_{CC} = 15 V		11
			0.02	2						
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
			1.5	1.8						
Input Reverse Breakdown Current	BV_R	5			V	I_R = 10 µA				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}		60		pF	f = 1 MHz	V_F = 0 V			
Input-Output Insulation Voltage	V_{ISO}	3750			V_{RMS}		RH < 50% T_A = 25°C	t = 1 min		6,12
Resistance (Input-Output)	R_{I-O}		$10^{[12]}$		Ω	V_{I-O} = 500 Vdc				6
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz				6

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified

Parameter	Sym.	Min.	Typ.	Max.	Units		Test Conditions	Fig.	Note	
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz Duty Cycle = 10%	8, 9	9	
			0.2	0.5			I_F = 16 mA R_L = 1.9 kΩ V_{THHL} = 1.5 V	V_{CC} = 5.0 V C_L = 15 pF		
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50%	10-14	10	
		0.1	0.5	1.0			I_F = 12 mA R_L = 20 kΩ V_{THHL} = 1.5 V	V_{CC} = 15.0 V C_L = 100 pF		
Propagation Delay Time to Logic High at Output	t_{PLH}		0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz Duty Cycle = 10%	8, 9	9	
			0.3	0.7			I_F = 16 mA R_L = 1.9 kΩ V_{THLH} = 1.5 V	V_{CC} = 5.0 V C_L = 15 pF		
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50%	10-14	10	
		0.2	0.8	1.4			I_F = 12 mA R_L = 20 kΩ V_{THLH} = 2.0 V	V_{CC} = 15.0 V C_L = 100 pF		
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz Duty Cycle = 50%	10-14	13	
		-0.7	0.3	1.3			I_F = 12 mA R_L = 20 kΩ V_{THHL} = 1.5 V	V_{CC} = 15.0 V C_L = 100 pF V_{THLH} = 2.0 V		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V C_L = 15 pF V_{CM} = 1500 V_{P-P}	R_L = 1.9 kΩ I_F = 0 mA	7	7,9
		15	30			T_A = 25°C	V_{CC} = 15.0 V C_L = 100 pF V_{CM} = 1500 V_{P-P}	R_L = 20 kΩ I_F = 0 mA	7	8,10
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V C_L = 15 pF V_{CM} = 1500 V_{P-P}	R_L = 1.9 kΩ I_F = 16 mA	7	7,9
		10	30			T_A = 25°C	V_{CC} = 15.0 V C_L = 100 pF V_{CM} = 1500 V_{P-P}	R_L = 20 kΩ I_F = 12 mA	7	8,10
		15	30			T_A = 25°C	V_{CC} = 15.0 V C_L = 100 pF V_{CM} = 1500 V_{P-P}	R_L = 20 kΩ I_F = 16 mA	7	8,10

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mA/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mA/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O), to the forward LED input current (I_F), times 100.
6. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5 and 6 shorted together.
7. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
8. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal,V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0$ V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The $R_L = 20$ kΩ, $C_L = 100$ pF load represents an IPM (Intelligent Power Mode) load.
11. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, $I_{i-e} \leq 5$ µA).
13. The difference between t_{PLH} and t_{PHL}, between any two HCPL-M454 parts under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section).

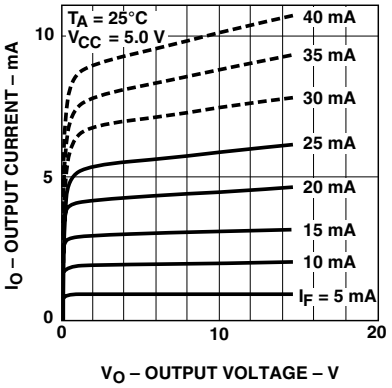


Figure 1. DC and Pulsed Transfer Characteristics.

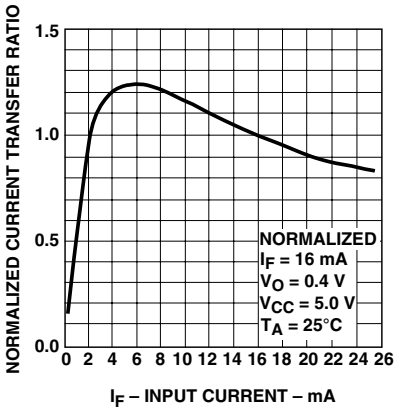


Figure 2. Current Transfer Ratio vs. Input Current.

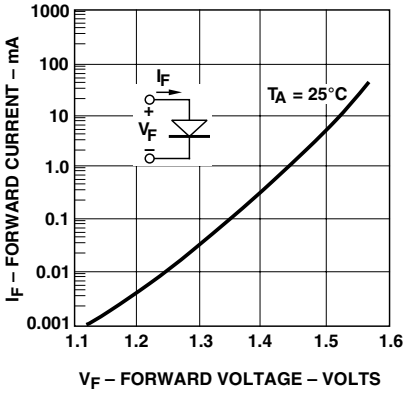


Figure 3. Input Current vs. Forward Voltage.

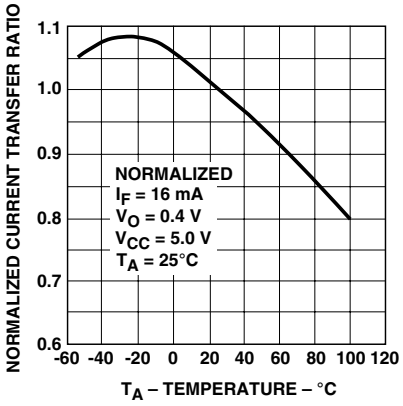


Figure 4. Current Transfer Ratio vs. Temperature.

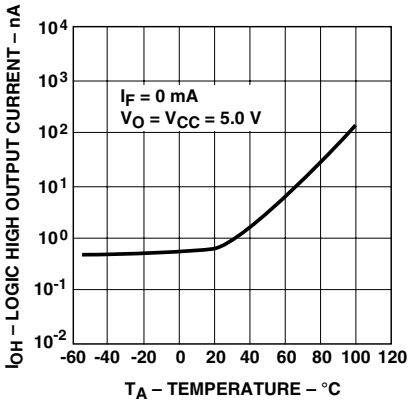


Figure 5. Logic High Output Current vs. Temperature.

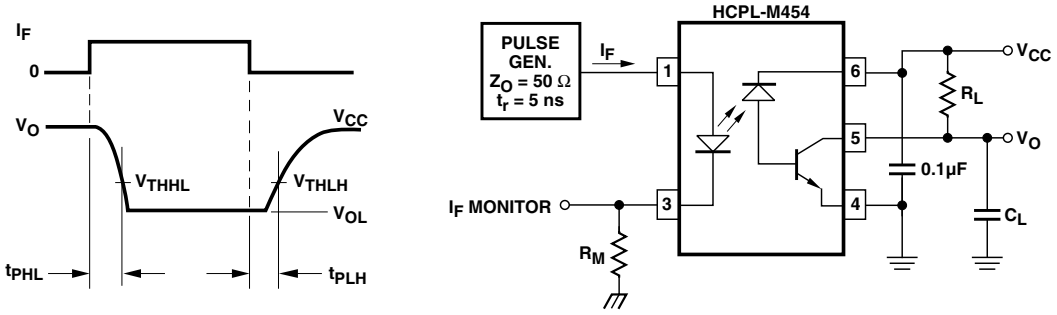


Figure 6. Switching Test Circuit.

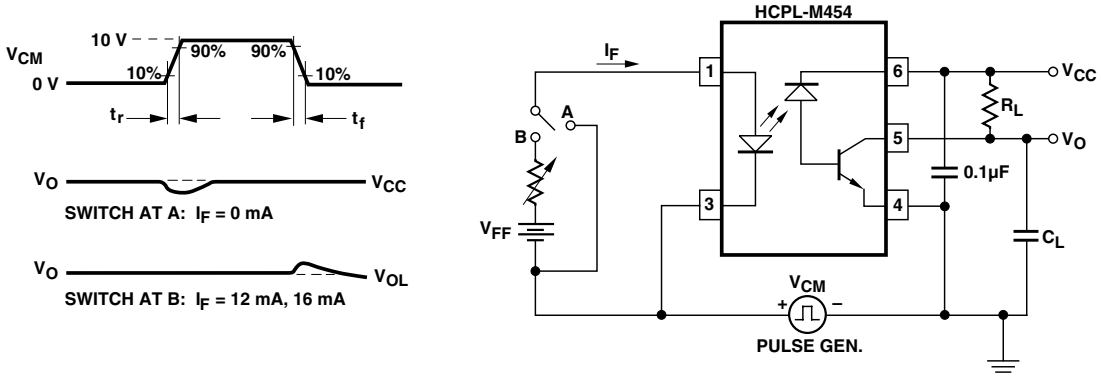


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

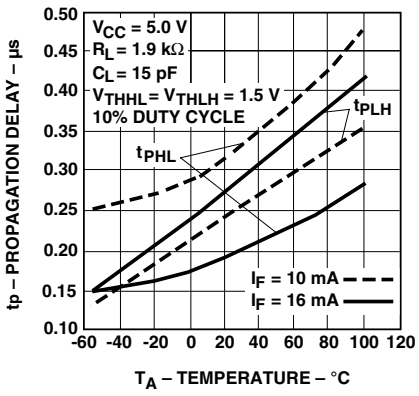


Figure 8. Propagation Delay Time vs. Temperature.

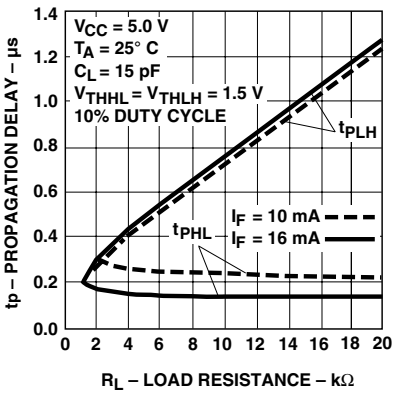


Figure 9. Propagation Delay Time vs. Load Resistance.

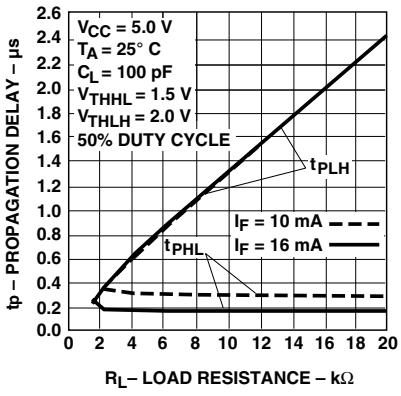


Figure 10. Propagation Delay Time vs. Load Resistance.

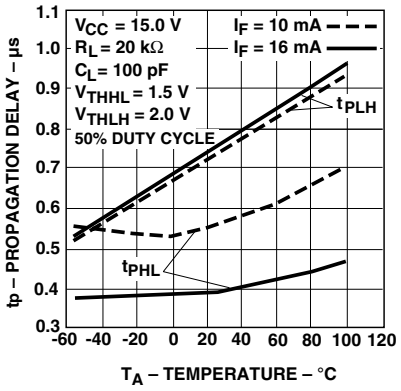


Figure 11. Propagation Delay Time vs. Temperature.

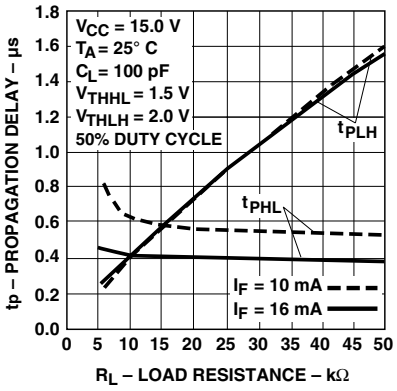


Figure 12. Propagation Delay Time vs. Load Resistance.

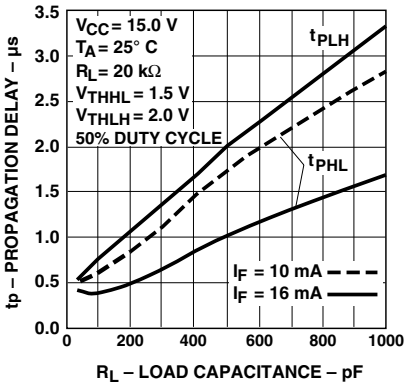


Figure 13. Propagation Delay Time vs. Load Capacitance.

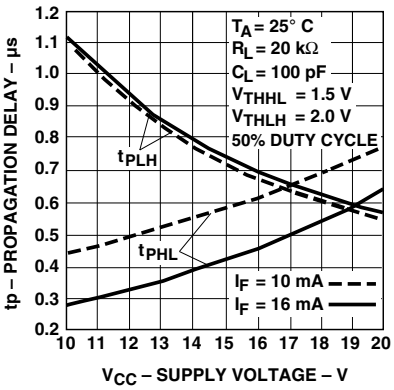


Figure 14. Propagation Delay Time vs. Supply Voltage.

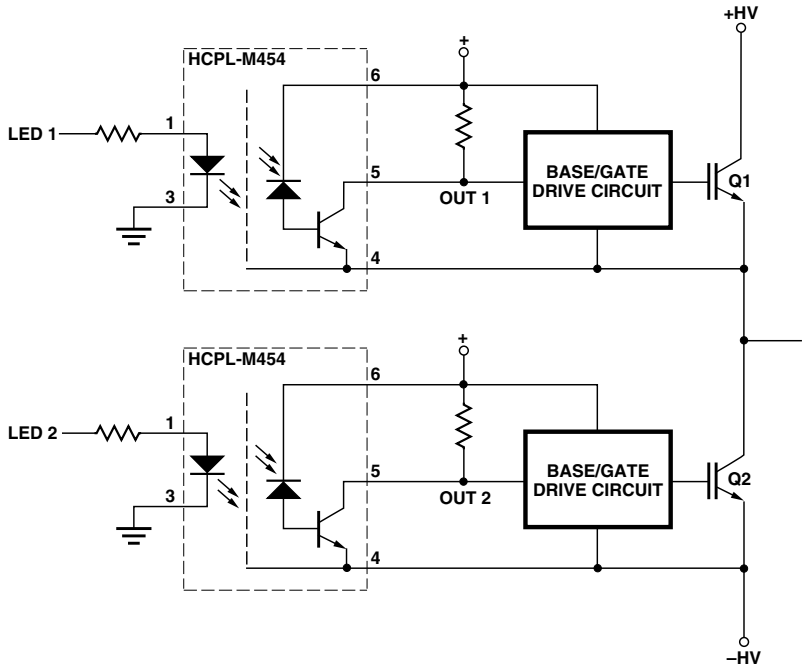


Figure 15. Typical Power Inverter.

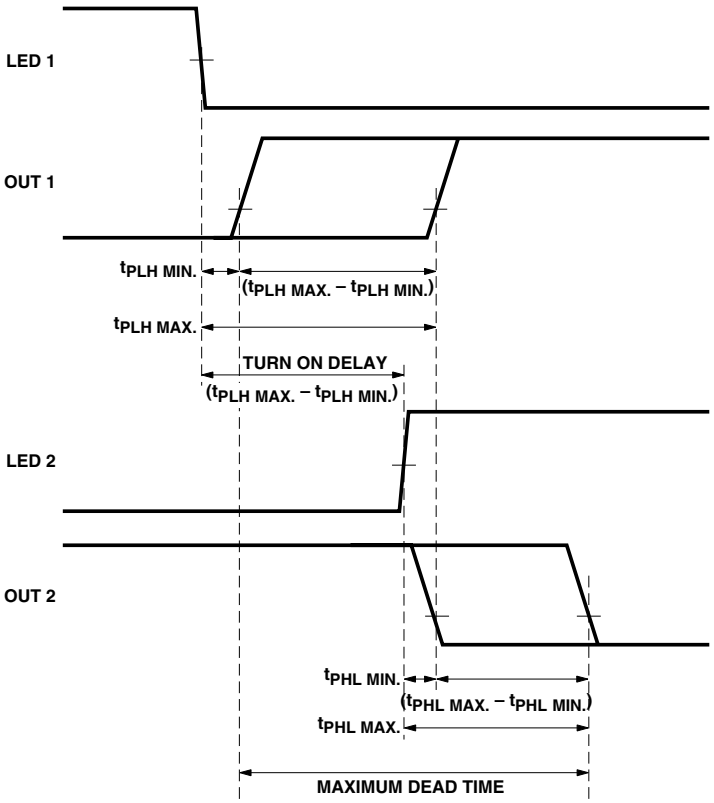


Figure 16. LED Delay and Dead Time Diagram.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-M454 includes a specification intended to help designers minimize "dead time" in their power inverter designs. The new "propagation delay difference" specification (t_{PLH} - t_{PHL}) is useful for determining not only how much optocoupler switching delay is needed to prevent "shoot-through" current, but also for determining the best achievable wort-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 15), it is essential that they never conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistor and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 16. The waveforms labeled "LED1", "LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 16 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) will never turn on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than (t_{PLHmax} - t_{PHLmin}), which also happens to be the maximum data sheet value for the propagation delay difference specification, (t_{PLH} - t_{PHL}). The HCPL-M454 specifies a maximum (t_{PLH} - t_{PHL}) of 1.3 µs over an operating temperature range of 0-70°C.

Although $(t_{PLH} - t_{PHL})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PLH} - t_{PHL})_{max}$, the minimum dead time is zero (i.e., there is zero time between the turn-off of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PLH} - t_{PHL})_{max}$, it can be seen in Figure 16 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turn-off delay,

$$[(t_{PLHmax}-t_{PLHmin}) + (t_{PHLmax}-t_{PHLmin})],$$

This expression can be rearranged to obtain

$$[(t_{PLHmax}-t_{PHLmin}) - (t_{PHLmin}-t_{PHLmax})],$$

and further rearranged to obtain

$$[(t_{PLH}-t_{PHL})_{max} - (t_{PLH}-t_{PHL})_{min}],$$

which is the maximum minus the minimum data sheet values of (t_{PLH} - t_{PHL}). The difference between the maximum and minimum values depends directly on the total spread of propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-M454 specifies a minimum (t_{PLH} - t_{PHL}) of -0.7 µs over an operating temeprature range of 0-70°C, resulting in a maximum dead time of 2.0 µs when the LED turn-on delay is equal to $(t_{PLH} - t_{PHL})_{max}$, or 1.3 µs.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PLH} - t_{PHL})_{max}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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