

HCPL0700, HCPL0701, HCPL0730, HCPL0731

Low Input Current High Gain Split Darlington Optocouplers

Single Channel: HCPL0700, HCPL0701, Dual Channel: HCPL0730, HCPL0731

Features

- Low input current: 0.5mA
- Superior CTR: 2000%
- Superior CMR – 10 kV/μs
- CTR guaranteed 0°C to 70°C
- U.L. Recognized (file# E90700)
- VDE 0884 recognized (file# 136616)
– approval pending for HCPL0730/0731
- BSI recognized (file# 8661, 8662)
– HCPL0700/0701 only

Applications

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver

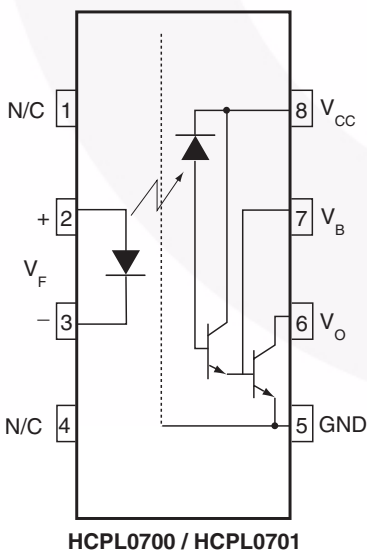
Description

The HCPL0700, HCPL0701, HCPL0730 and HCPL0731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector housed in a compact 8-pin small outline package. The HCPL0730 and HCPL0731 devices have two channels per package for optimum mounting density.

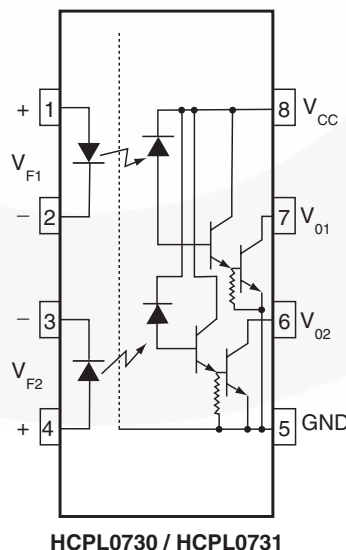
The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

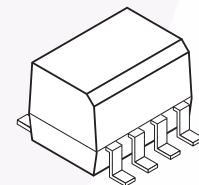
Schematics



HCPL0700 / HCPL0701



HCPL0730 / HCPL0731



Truth Table

LED	V _O
ON	LOW
OFF	HIGH

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units	
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$	
T_{OPR}	Operating Temperature	-40 to +85	$^\circ\text{C}$	
	Reflow Temperature Profile (Refer to page 12)			
EMITTER				
I_F (avg)	DC/Average Forward Input Current	20	mA	
I_F (pk)	Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	40	mA	
I_F (trans)	Peak Transient Input Current - ($\leq 1 \mu\text{s}$ P.W., 300 pps)	1.0	A	
V_R	Reverse Input Voltage	5	V	
P_D	Input Power Dissipation	35	mW	
DETECTOR				
I_O (avg)	Average Output Current (Pin 6)	60	mA	
V_{EBR}	Emitter-Base Reverse Voltage	HCPL0700/HCPL0701	0.5	V
V_{CC}, V_O	Supply Voltage, Output Voltage	HCPL0700/HCPL0730	-0.5 to 7	V
		HCPL0701/HCPL0731	-0.5 to 18	
P_D	Output power dissipation	100	mW	

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max	Unit	
EMITTER								
V_F	Input Forward Voltage	$I_F = 1.6\text{mA}$	$T_A = 25^\circ\text{C}$	HCPL0700/01	1.0	1.25	1.7	V
				HCPL0730/31		1.35		
		All				1.75		
BV_R	Input Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}, I_R = 10\mu\text{A}$	All	5.0				
DETECTOR								
I_{OH}	Logic High Output Current	$I_F = 0\text{mA}, V_O = V_{CC} = 18\text{V}$	HCPL0701/31		0.01	100	μA	
		$I_F = 0\text{mA}, V_O = V_{CC} = 7\text{V}$	HCPL0700/30		0.01	250		
I_{CCL}	Logic Low Supply Current	$I_F = 1.6\text{mA}, V_O = \text{Open}, V_{CC} = 18\text{V}$	HCPL0700/01		0.4	1.5	mA	
		$I_{F1} = I_{F2} = 1.6\text{mA}, V_{CC} = 7\text{V}$	HCPL0730		0.8	3		
		$V_{O1} = V_{O2} = \text{Open}, V_{CC} = 18\text{V}$	HCPL0731		1			
I_{CCH}	Logic High Supply Current	$I_F = 0\text{mA}, V_O = \text{Open}, V_{CC} = 18\text{V}$	HCPL0700/01			10	μA	
		$I_{F1} = I_{F2} = 0, V_{CC} = 7\text{V}$	HCPL0730		0.001	20		
		$V_{O1} = V_{O2} = \text{Open}, V_{CC} = 18\text{V}$	HCPL0731		0.01			

Transfer Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
CTR	COUPLED Current Transfer Ratio (Note 1, 2)	$I_F = 0.5\text{mA}, V_O = 0.4\text{V}, V_{CC} = 4.5\text{V}$	HCPL0701/31	400		5000	%
		$I_F = 1.6\text{mA}, V_O = 0.4\text{V}, V_{CC} = 4.5\text{V}$	HCPL0700	300		2600	
			HCPL0701	500		2600	
			HCPL0730	300		5000	
			HCPL0731	500		5000	
V_{OL}	Logic Low Output Voltage	$I_F = 0.5\text{mA}, I_O = 2\text{mA}, V_{CC} = 4.5\text{V}$	HCPL0701			0.4	V
		$I_F = 1.6\text{mA}, I_O = 8\text{mA}, V_{CC} = 4.5\text{V}$	HCPL0731			0.4	
		$I_F = 5\text{mA}, I_O = 15\text{mA}, V_{CC} = 4.5\text{V}$				0.4	
		$I_F = 12\text{mA}, I_O = 24\text{mA}, V_{CC} = 4.5\text{V}$				0.4	
		$I_F = 1.6\text{mA}, I_O = 4.8\text{mA}, V_{CC} = 4.5\text{V}$	HCPL0700/0730			0.4	

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^\circ\text{C}, t = 5\text{ s},$ $V_{I-O} = 3000\text{ VDC}$ (Note 4)			1.0	μA
V_{ISO}	Withstand Insulation Test Voltage	$R_H \leq 50\%, T_A = 25^\circ\text{C},$ $I_{I-O} \leq 2\mu\text{A}, t = 1\text{ min.}$ (Note 4, 5)	2500			V_{RMS}
R_{I-O}	Resistance (Input to Output)	$V_{I-O} = 500\text{ VDC}$ (Note 4)		10^{12}		Ω

 *All typicals at $T_A = 25^\circ\text{C}$

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)

Switching Characteristics ($V_{CC} = 5\text{V}$)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit			
T_{PHL}	Propagation Delay Time to Logic Low (Note 2) (Fig. 14)	$R_L = 4.7\text{k}\Omega$, $I_F = 0.5\text{mA}$	HCPL0701			30	μs			
			HCPL0731			120				
			HCPL0701			$T_A = 25^\circ\text{C}$		3	25	
			HCPL0731			5		100		
		$R_L = 270\ \Omega$, $I_F = 12\text{mA}$	HCPL0701					2		
			HCPL0731					3		
			HCPL0701					$T_A = 25^\circ\text{C}$	0.3	1
			HCPL0731					0.4	2	
		$R_L = 2.2\ \text{k}\Omega$, $I_F = 1.6\text{mA}$	HCPL0700					15		
			HCPL0730/0731					25		
			HCPL0700					$T_A = 25^\circ\text{C}$	1	10
			HCPL0730/0731					2	20	
T_{PLH}	Propagation Delay Time to Logic High (Note 2) (Fig. 14)	$R_L = 4.7\ \text{k}\Omega$, $I_F = 0.5\text{mA}$	HCPL0701/31			90	μs			
			HCPL0701/31			$T_A = 25^\circ\text{C}$		12	60	
		$R_L = 270\ \Omega$, $I_F = 12\text{mA}$	HCPL0701					10		
			HCPL0731					15		
			HCPL0701					$T_A = 25^\circ\text{C}$	1.6	7
			HCPL0731					1.6	10	
		$R_L = 2.2\ \text{k}\Omega$, $I_F = 1.6\text{mA}$	HCPL0700/30/31					50		
			HCPL0700/30/31					$T_A = 25^\circ\text{C}$	7	35
		ICM_H	Common Mode Transient Immunity at Logic High	$I_F = 0\text{mA}$, $ V_{CM} = 10\ \text{V}_{P-P}$, $T_A = 25^\circ\text{C}$, $R_L = 2.2\text{k}\Omega$ (Note 3) (Fig. 15)	ALL	1,000	10,000		$\text{V}/\mu\text{s}$	
		ICM_L	Common Mode Transient Immunity at Logic Low	$I_F = 1.6\text{mA}$, $ V_{CM} = 10\ \text{V}_{P-P}$, $T_A = 25^\circ\text{C}$, $R_L = 2.2\ \text{k}\Omega$ (Note 3) (Fig. 15)	ALL	1,000	10,000		$\text{V}/\mu\text{s}$	

*All typicals at $T_A = 25^\circ\text{C}$

Notes:

- Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
- Pin 7 open. Use of a resistor between pins 5 and 7 will decrease gain and delay time.
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\ \text{V}$).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

Typical Performance Curves

Fig. 1 Propagation Delay vs. Temperature (HCPL0700, HCPL0701)

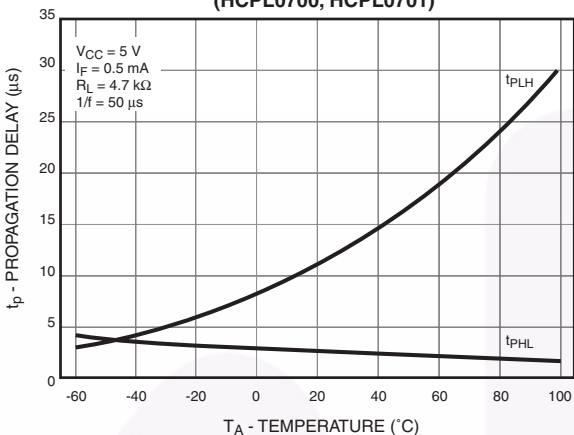


Fig. 2 Propagation Delay vs. Temperature (HCPL0700, HCPL0701)

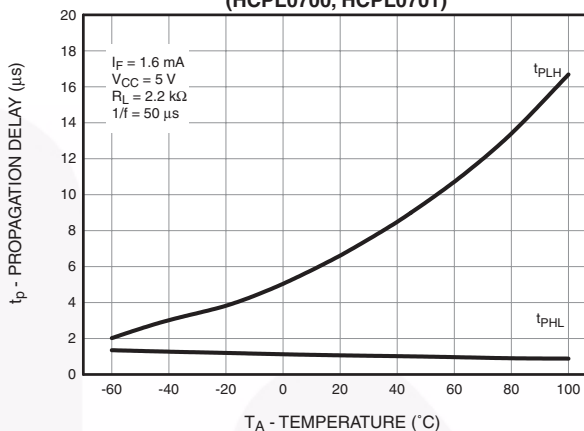


Fig. 3 Propagation Delay vs. Temperature (HCPL0700, HCPL0701)

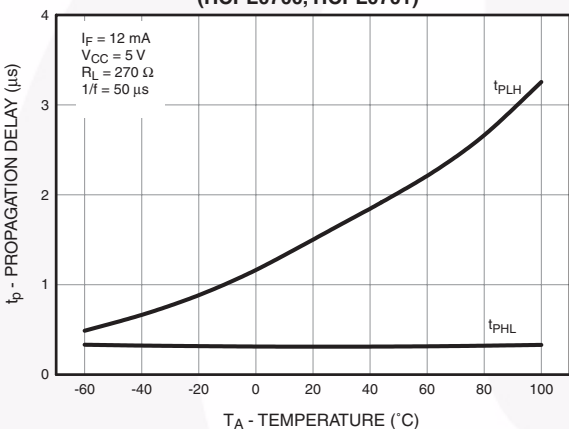


Fig. 4 Logic High Output Current vs. Temperature (HCPL0700, HCPL0701)

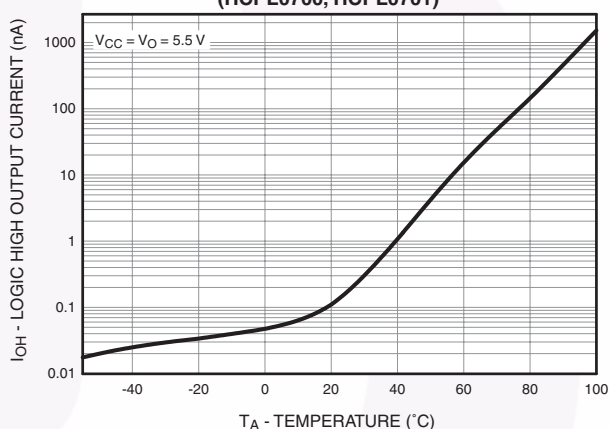


Fig. 5 Propagation Delay vs. Input Forward Current (HCPL0730, HCPL0731)

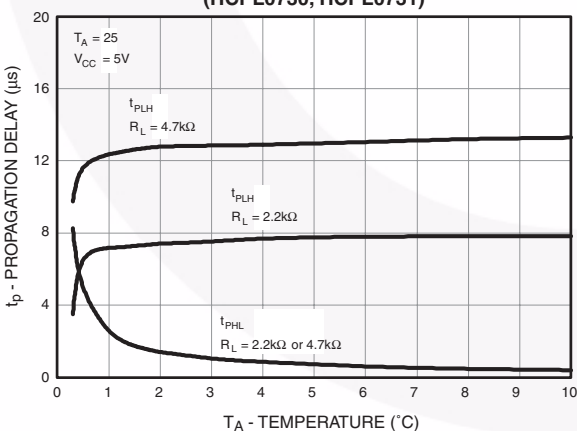
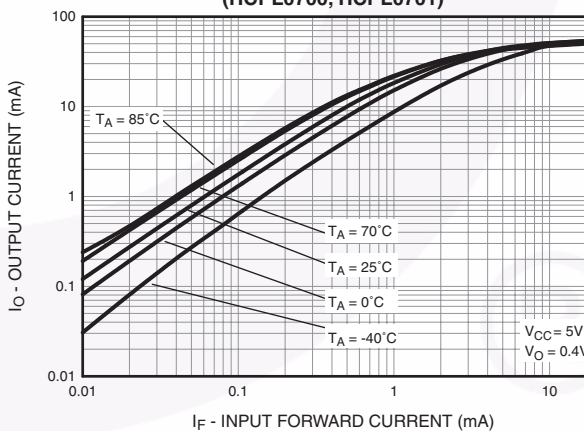


Fig. 6 Output Current vs. Input Forward Current (HCPL0700, HCPL0701)



Typical Performance Curves (Continued)

Fig. 7 Input Forward Current vs. Forward Voltage (HCPL0700, HCPL0701)

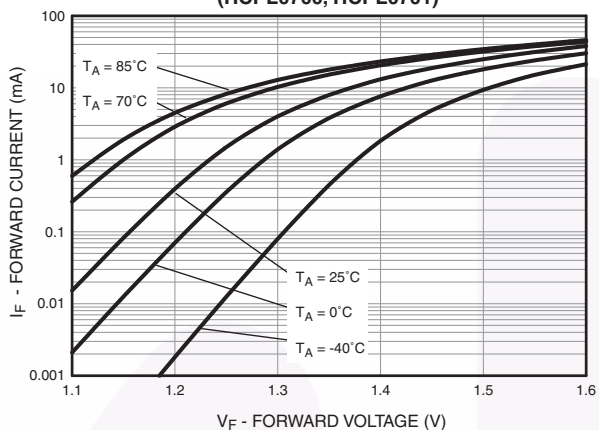


Fig. 8 Input Forward Current vs. Forward Voltage (HCPL0730, HCPL0731)

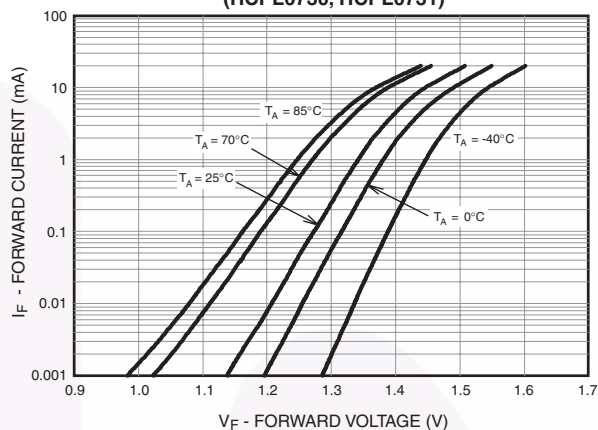


Fig. 9 Logic Low Supply Current vs. Input Forward Current (HCPL0700, HCPL0701)

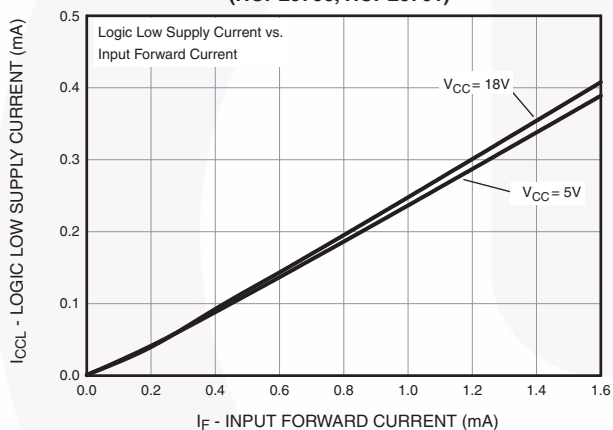


Fig. 10 Supply Current vs. Input Forward Current (HCPL0730, HCPL0731)

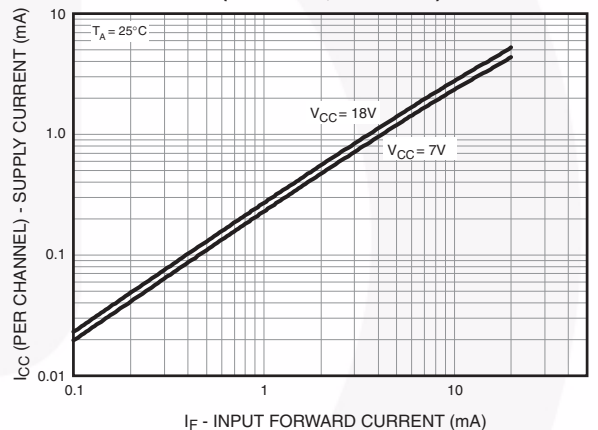


Fig. 11 DC Transfer Characteristics (HCPL0700, HCPL0701)

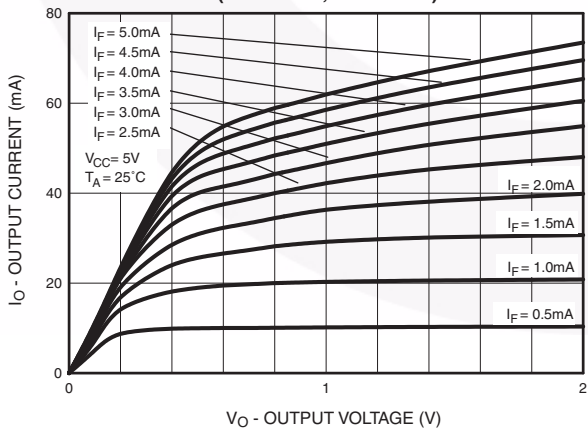
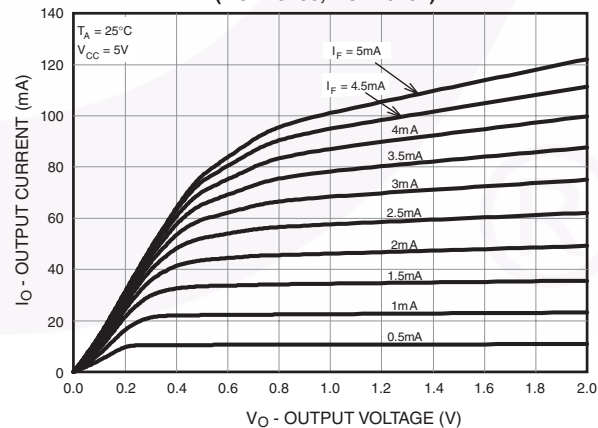
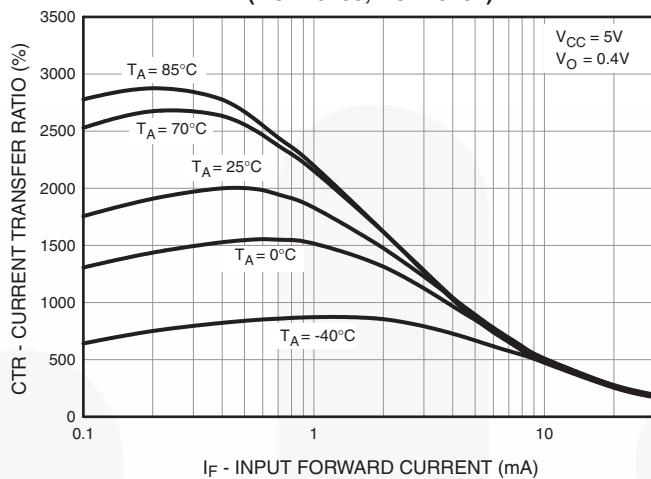


Fig. 12 DC Transfer Characteristics (HCPL0730, HCPL0731)

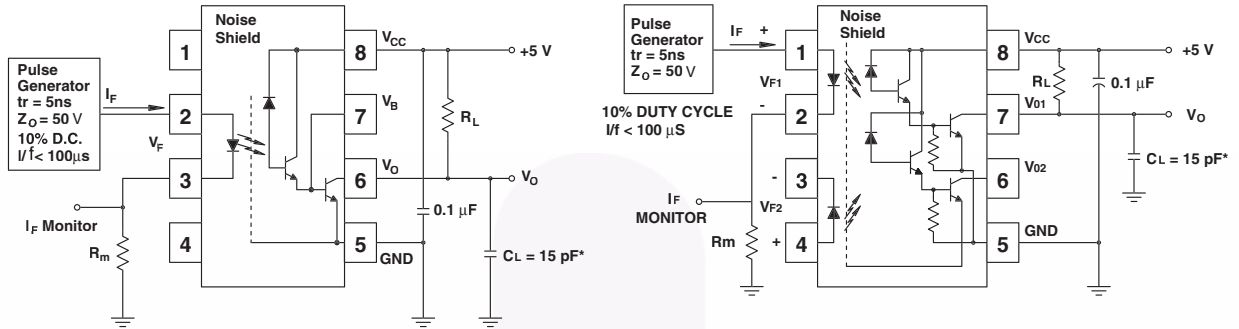


Typical Performance Curves (Continued)

Fig. 13 Current Transfer Ratio vs. Input Forward Current (HCPL0700, HCPL0701)



Test Circuits



Test Circuit for HCPL-0700 and HCPL-0701

Test Circuit for HCPL-0730 and HCPL-0731

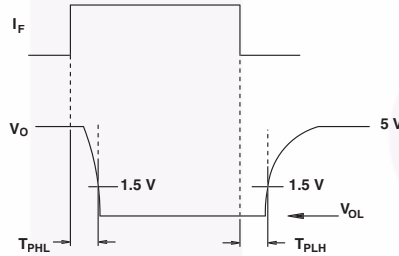
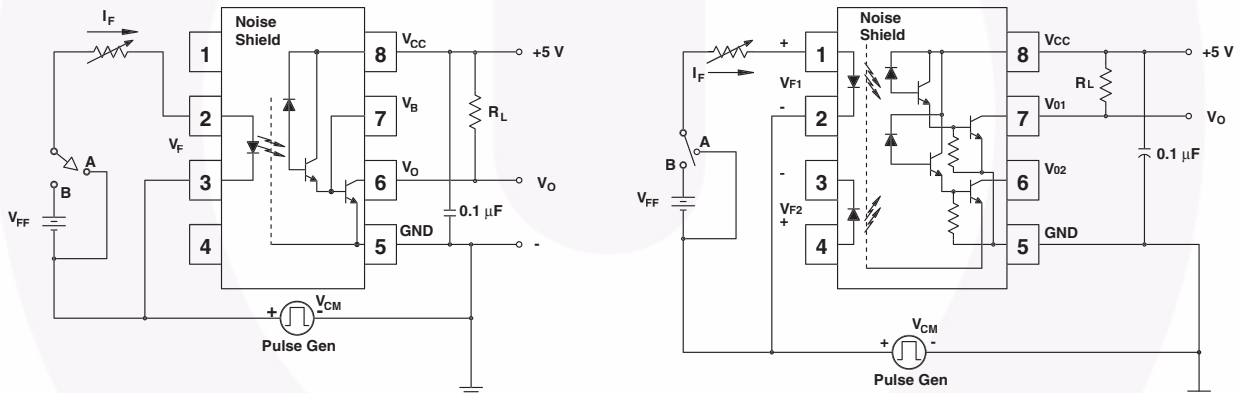


Fig. 14 Switching Time Test Circuit



Test Circuit for HCPL-0700 and HCPL-0701

Test Circuit for HCPL-0730 and HCPL-0731

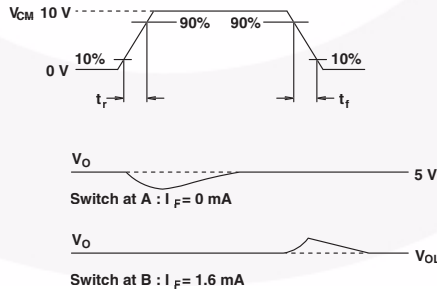
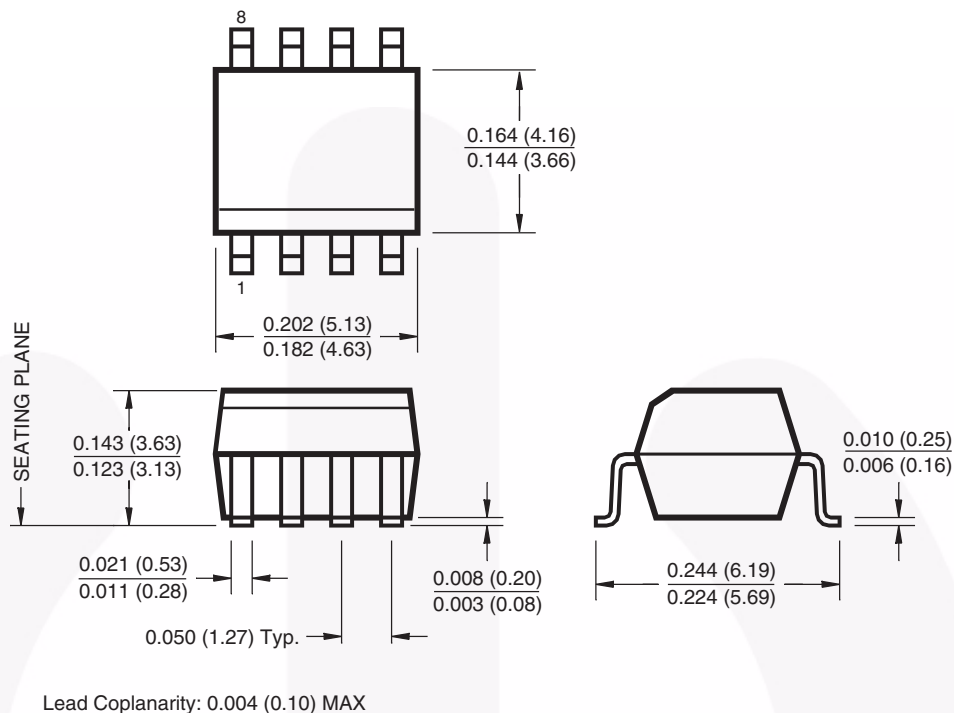


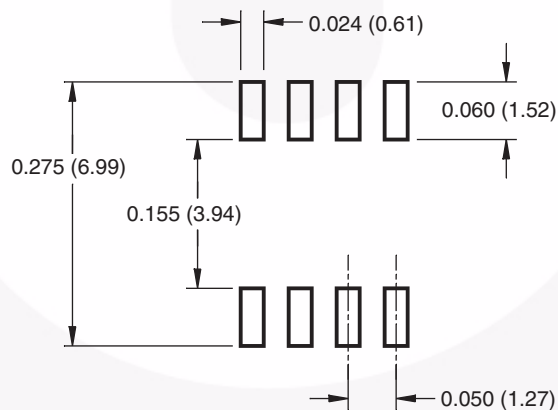
Fig. 15 Common Mode Immunity Test Circuit

Package Dimensions

8-pin SOIC Surface Mount



Recommended Pad Layout



Dimensions in inches (mm).

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Ordering Information

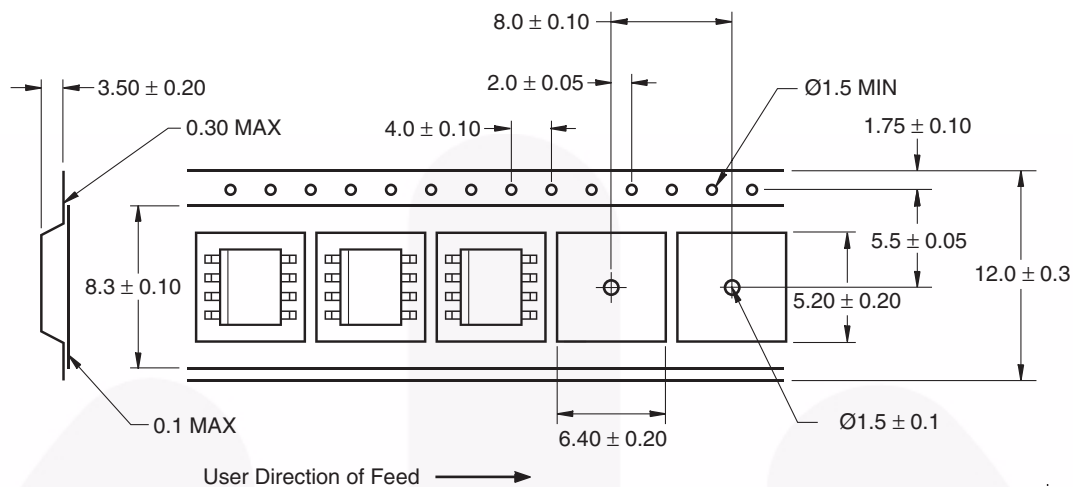
Option	Part Number Example	Description
V	HCPL0700V	VDE 0884
R2	HCPL0700R2	Tape and reel (2500 units per reel)
R2V	HCPL0700R2V	VDE 0884, Tape and reel (2500 units per reel)

Marking Information



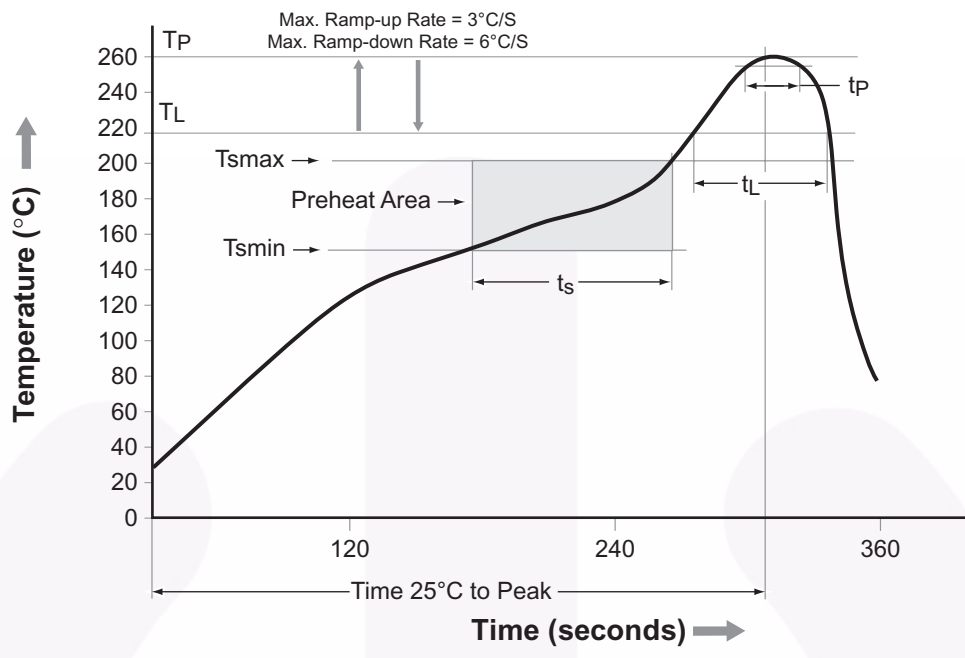
Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Carrier Tape Specification



Dimensions in mm

Reflow Profile








Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T _{smín})	150°C
Temperature Max. (T _{smáx})	200°C
Time (t _s) from (T _{smín} to T _{smáx})	60–120 seconds
Ramp-up Rate (t _L to t _p)	3°C/second max.
Liquidous Temperature (T _L)	217°C
Time (t _L) Maintained Above (T _L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t _p) within 5°C of 260°C	30 seconds
Ramp-down Rate (T _P to T _L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



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| CTL™ | Gmax™ | Quiet Series™ | TinyLogic® |
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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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