FAIRCHILD SEMICONDUCTOR®

April 2009

FOD0708 Single Channel CMOS Optocoupler, FOD0738 Dual Channel CMOS Optocoupler

Features

- +5V CMOS compatibility
- 15ns typical pulse width distortion
- 30ns max. pulse width distortion
- 40ns max. propagation delay skew
- High speed: 15 MBd
- 60ns max. propagation delay
- 10kV/µs minimum common mode rejection
- –40°C to 100°C temperature range
- UL approved (file #E90700)

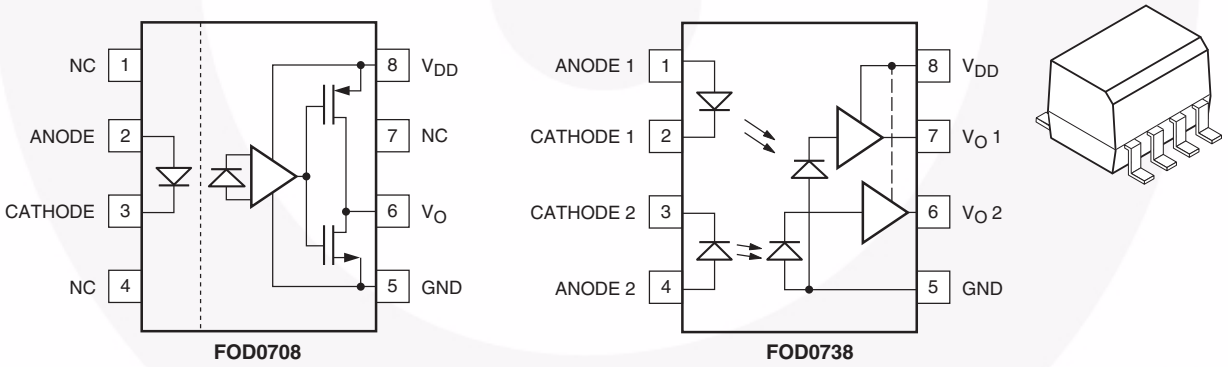
Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

General Description

The FOD0708 and FOD0738 optocouplers consist of an AlGaAs LED optically coupled to a high speed trans-impedance amplifier and voltage comparator. These optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The devices are housed in a compact 8-pin SOIC package for optimum mounting density.

Schematics



TRUTH TABLE

LED	V_O OUTPUT
OFF	H
ON	L

Note: A 0.1µF bypass capacitor must be connected between pins 5 and 8.

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Units
T_S	Storage Temperature	–40	+125	°C
T_A	Ambient Operating Temperature	–40	+100	°C
V_{DD}	Supply Voltages	0	6	Volts
V_O	Output Voltage	–0.5	V_{DD} + 0.5	Volts
I_O	Average Output Current		2	mA
I_F	Average Forward Input Current		20	mA
	Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane		
	Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile Section		
	LED Power Dissipation Single Channel Dual Channel	 40mW (derate above 95°C, 1.4mW/°C) 40mW per channel (derate above 90°C, 1.2mW/°C)		
	Detector Power Dissipation Single Channel Dual Channel	 85mW (derate above 75°C, 1.8mW/°C) 65mW per channel (derate above 90°C, 2.0mW/°C)		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
T_A	Ambient Operating Temperature	–40	+100	°C
V_{DD}	Supply Voltages	4.5	5.5	Volts
I_F	Input Current (ON)	10	16	mA

Electrical Characteristics (T_A = –40°C to +100°C) and 4.5 V ≤ V_{DD} ≤ 5.5 V

Symbol	Parameter		Test Conditions	Min.	Typ.*	Max.	Units	Fig.
V_F	Input Forward Voltage		I_F = 12mA	1.3	1.45	1.8	V	9
BV_R	Input Reverse Breakdown Voltage		I_R = 10µA	5			V	
V_{OH}	Logic High Output Voltage		I_F = 0, I_O = –20µA	4.0	5.0		V	
V_{OL}	Logic Low Output Voltage		I_F = 12mA, I_O = 20µA		0.01	0.1	V	
I_{TH}	Input Threshold Current	(FOD0708) (FOD0738)	I_{OL} = 20µA		4.0 4.4	8.2 8.2	mA	1,5
I_{DDL}	Logic Low Output Supply Current	(FOD0708) (FOD0738)	I_F = 12mA		3.4 6.9	14.0 18.0	mA	3,7
I_{DDH}	Logic High Output Supply Current	(FOD0708) (FOD0738)	I_F = 0		3.7 7.5	11.0 15.0	mA	4,8

*All typicals at T_A = 25°C and V_{DD} = 5V unless otherwise noted.

Switching Characteristics

Over recommended temperature (T_A = –40°C to +100°C) and 4.5 V ≤ V_{DD} ≤ 5.5 V. All typical specifications are at T_A = 25°C, V_{DD} = +5 V.

Symbol	Parameter	Test Conditions		Min.	Typ.*	Max.	Units
t_{PHL}	Propagation Delay Time to Logic Low Output	I_F = 12mA, C_L = 15pF CMOS Signal Levels (Note 1) (Fig. 10)		20		60	ns
t_{PLH}	Propagation Delay Time to Logic High Output	I_F = 12mA, C_L = 15pF CMOS Signal Levels, (Note 1) (Fig. 10)	FOD0708	13		60	ns
			FOD0738	11		60	
PW	Pulse Width			100			ns
| PWD |	Pulse Width Distortion	I_F = 12mA, C_L = 15pF, CMOS Signal Levels (Note 2)		0		30	ns
t_{PSK}	Propagation Delay Skew	I_F = 12mA, C_L = 15pF, CMOS Signal Levels (Note 3)				40	ns
t_R	Output Rise Time (10%–90%)	I_F = 12mA, C_L = 15pF, CMOS Signal Levels			12		ns
t_F	Output Fall Time (90%–10%)	I_F = 12mA, C_L = 15pF, CMOS Signal Levels			8		ns
| CM_H |	Common Mode Transient Immunity at Logic High Output	V_{CM} = 1000V, T_A = 25°C, I_F = 0mA, (Note 4) (Fig. 11)		25	50		kV/µs
| CM_L |	Common Mode Transient Immunity at Logic Low Output	V_{CM} = 1000V, T_A = 25°C, I_F = 12mA, (Note 5) (Fig. 11)		25	50		kV/µs

*All typicals at T_A = 25°C and V_{DD} = 5V unless otherwise noted.

Isolation Characteristics

(T_A = -40°C to +100°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ.*	Max	Unit
Input-Output Insulation Leakage Current	Relative humidity = 45%, T_A = 25°C, t = 5s, V_{I-O} = 3000 VDC (Note 6)	I_{I-O}			1.0	µA
Withstand Insulation Test Voltage	I_{I-O} ≤ 10µA, R_H < 50%, T_A = 25°C, t = 1 min. (Note 6)	V_{ISO}	2500			V_{RMS}
Resistance (Input to Output)	V_{I-O} = 500V (Note 6)	R_{I-O}		10^{12}		Ω
Capacitance (Input to Output)	f = 1MHz (Note 6)	C_{I-O}		0.6		pF

*All typical values are at V_{CC} = 5 V, T_A = 25°C

Notes:

1. Propagation delay time, high to low (t_{PHL}), is measured from the 50% level on the rising edge of the input pulse to the 2.5V level of the falling edge of the output voltage signal. Propagation delay time, low to high (t_{PLH}), is measured from the 50% level on the falling edge of the input pulse to the 2.5V level of the rising edge of the output voltage signal.
2. Pulse width distoration is defined as the absolute difference between the high to low and low to high propagation delay times, | t_{PHL} – t_{PLH} |.
3. Propagation delay skew, t_{PSK}, is defined as the worst case difference in t_{PHL} or t_{PLH} between units within the recommended operating range of the device.
4. CM_H – The maximum tolerated rate of rise of the common mode voltage to ensure the output will remain in the high state, (i,e., V_{OUT} > 2.0V) Measured in kilovolts per microsecond (kV/µs).
5. CM_L – The maximum tolerated rate of fall of the common mode voltage to ensure the output will remain in the low state, (i,e., V_{OUT} < 0.8V). Measured in kilovolts per microsecond (kV/µs).
6. Isolation voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, pins 1,2,3,4 are common, and pins 5,6,7,8 are common.

Typical Performance Curves

Figure 1. FOD0708
Typical Input Threshold Current
vs Ambient Temperature

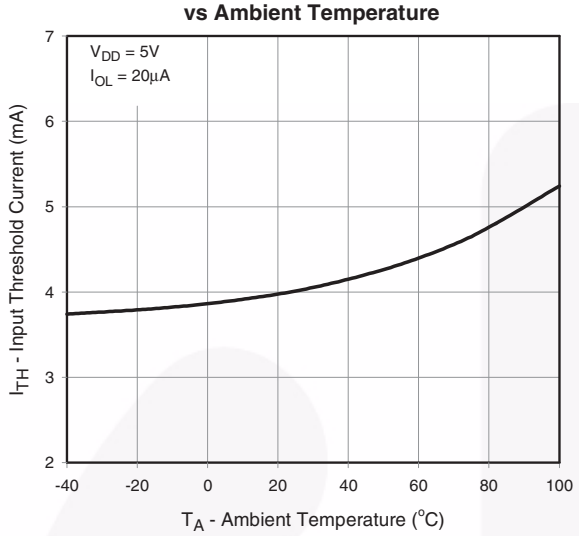


Figure 2. FOD0708
Typical Switching Speed vs Pulse Input Current

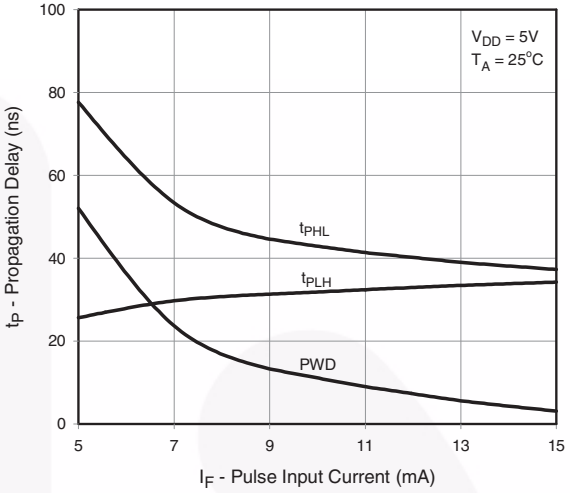


Figure 3. FOD0708
Typical Logic Low Output Supply Current
vs Ambient Temperature

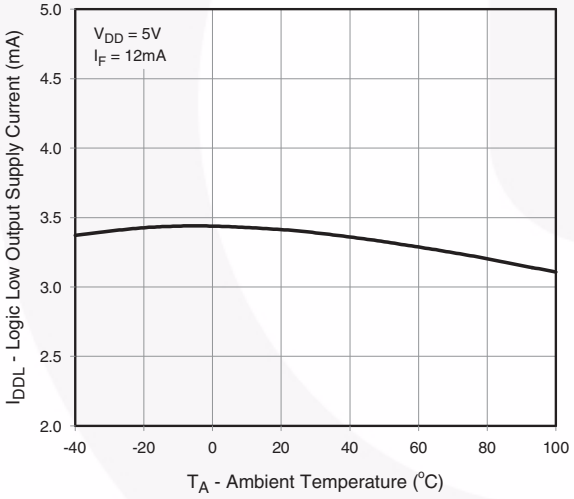
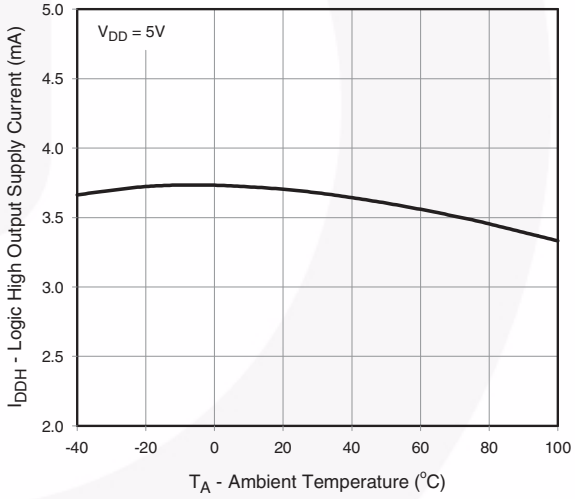


Figure 4. FOD0708
Typical Logic High Output Supply Current
vs Ambient Temperature



Typical Performance Curves (Continued)

Figure 5. FOD0738
Typical Input Threshold Current
vs Ambient Temperature

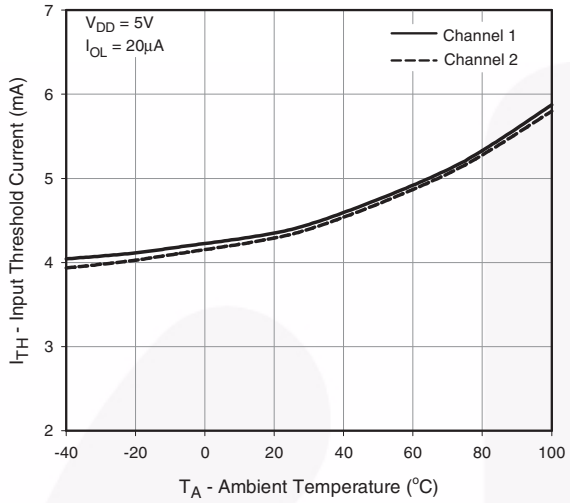


Figure 6. FOD0738
Typical Switching Speed vs Pulse Input Current

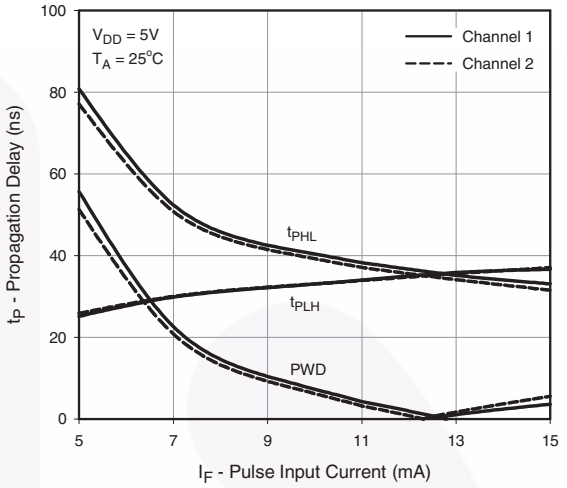


Figure 7. FOD0738
Typical Logic Low Output Supply Current
vs Ambient Temperature

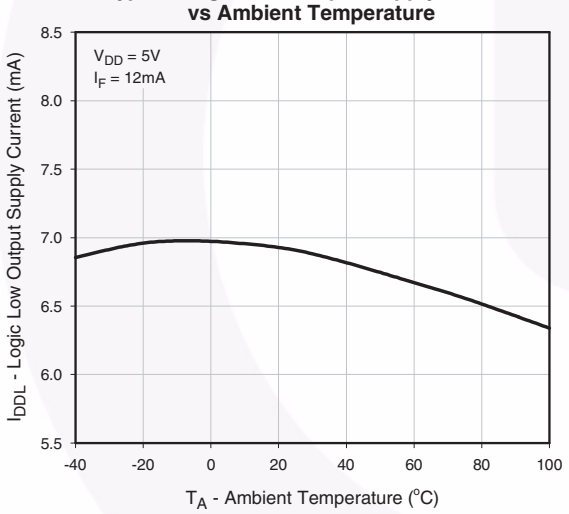
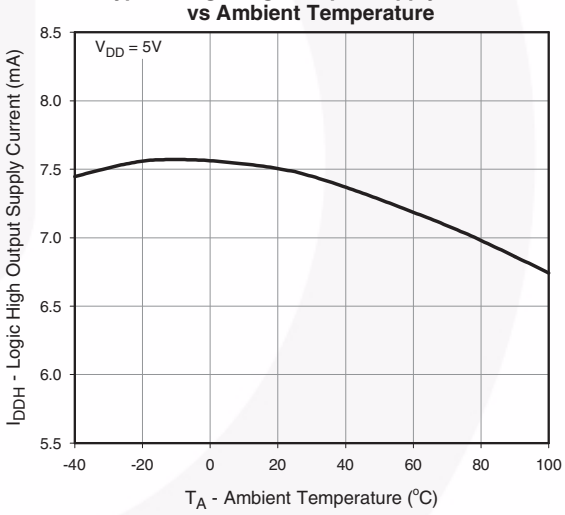
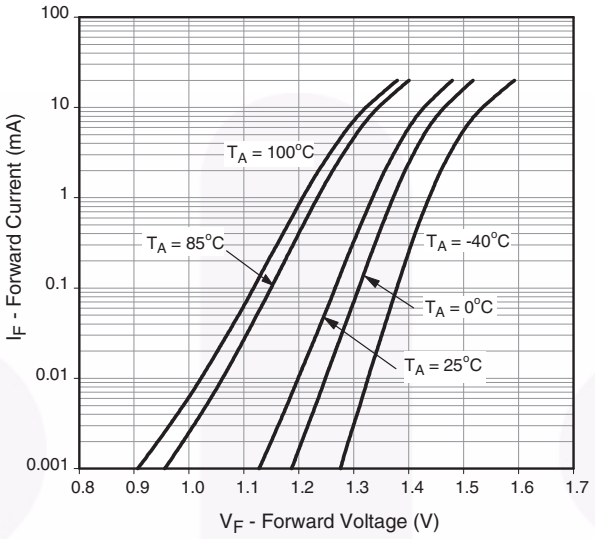


Figure 8. FOD0738
Typical Logic High Output Supply Current
vs Ambient Temperature



Typical Performance Curves (Continued)

Figure 9. Input Forward Current vs. Forward Voltage



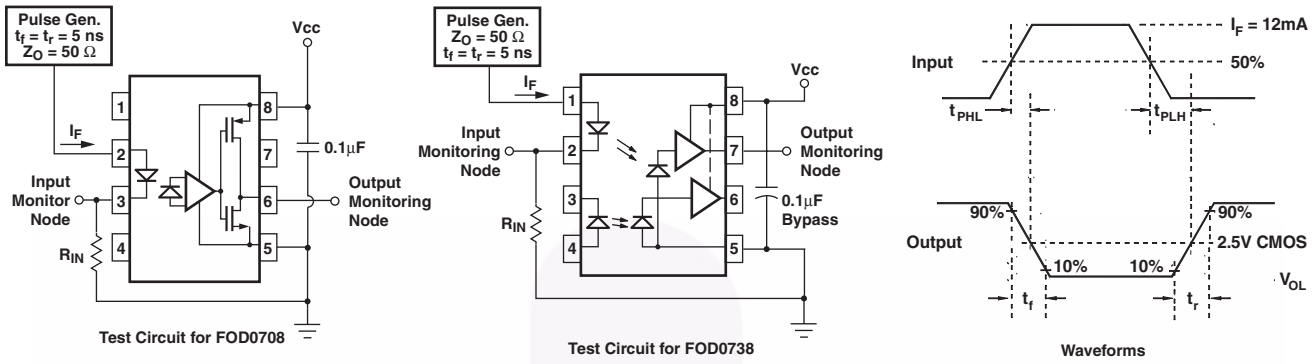


Fig. 10 Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f.

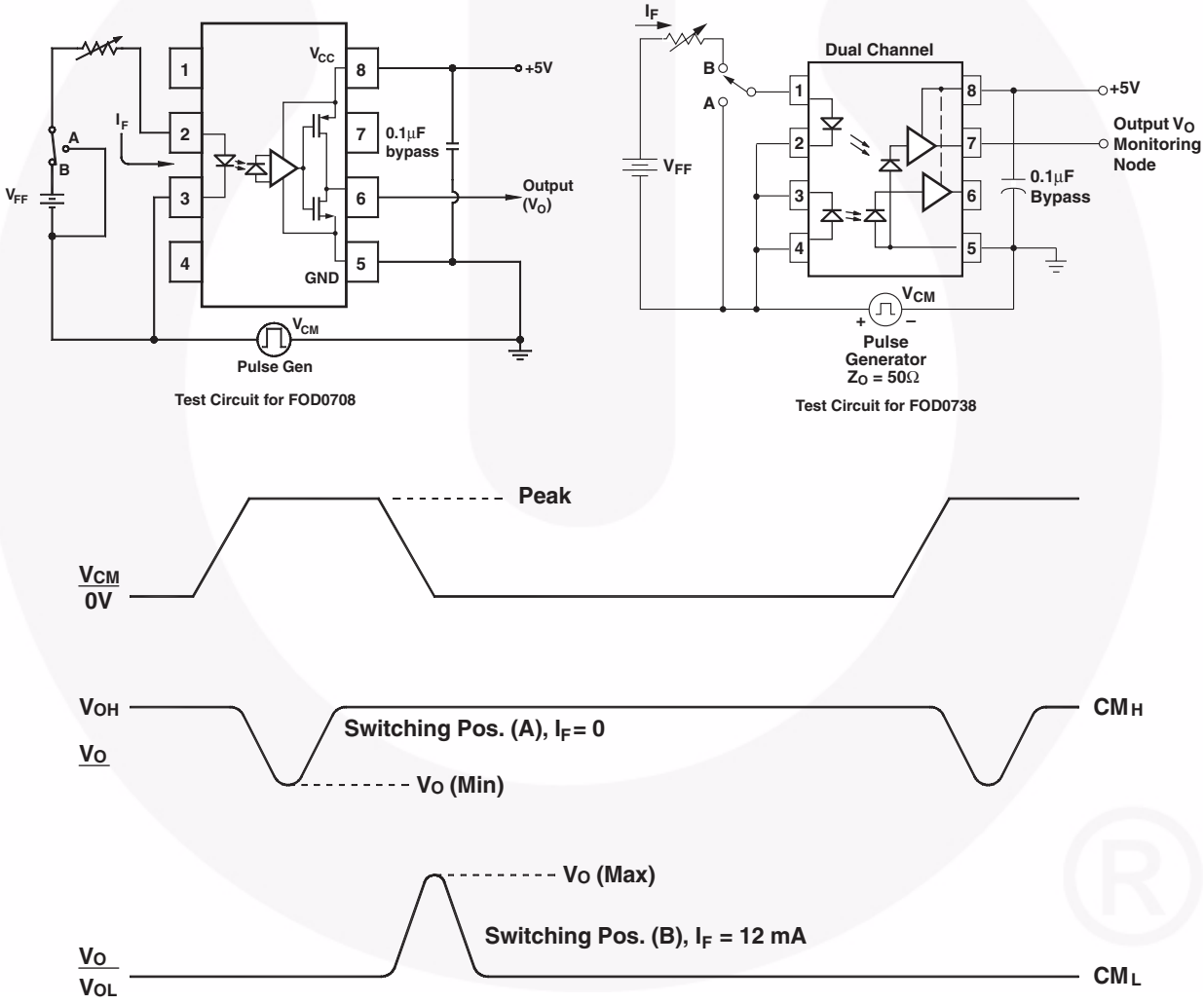
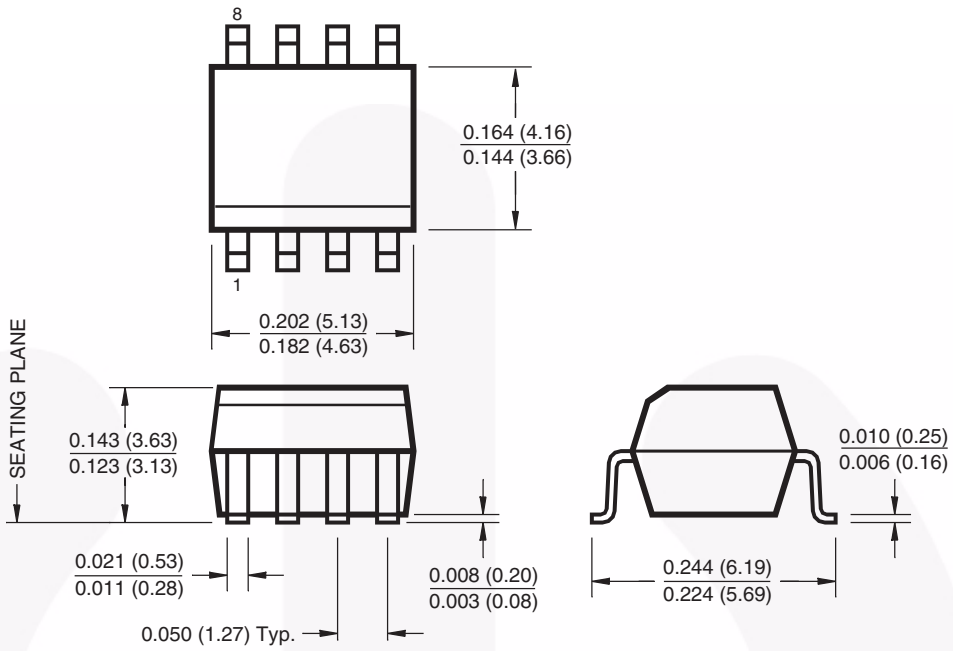


Fig. 11 Test Circuit Common Mode Transient Immunity (FOD0708 and FOD0738)

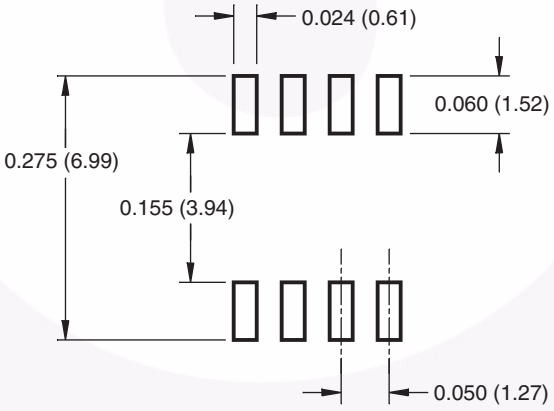
Package Dimensions

8-pin SOIC Surface Mount



Lead Coplanarity: 0.004 (0.10) MAX

Recommended Pad Layout



Dimensions in inches (mm).

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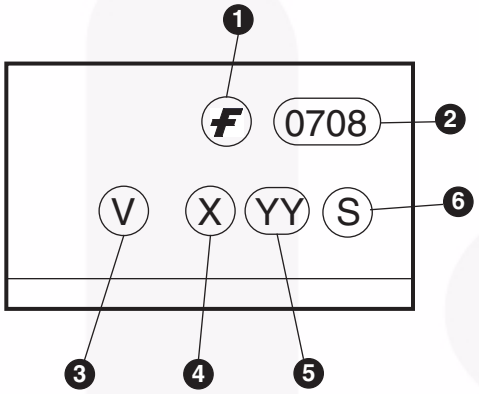
http://www.fairchildsemi.com/packaging/

Ordering Information

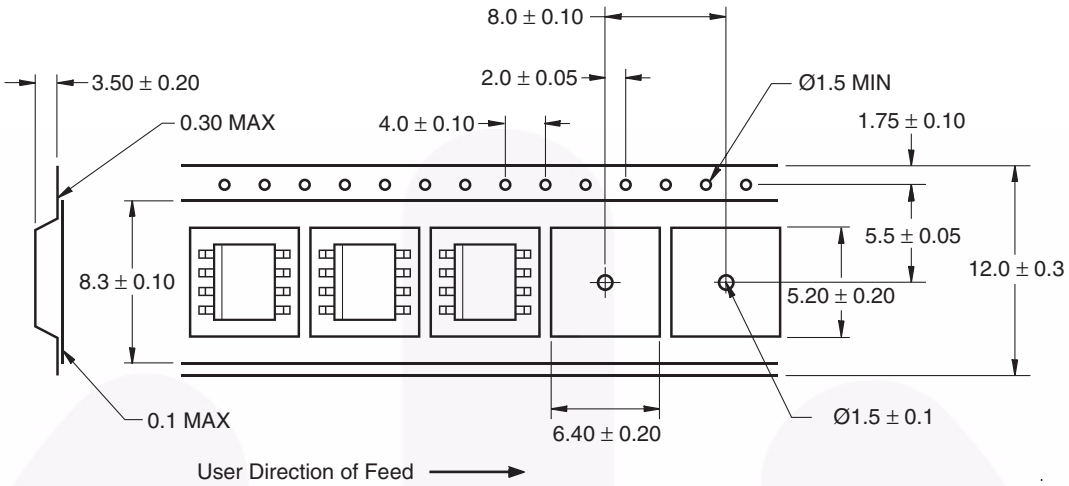
Option	Order Entry Identifier	Description
No Suffix	FOD0708	Shipped in tubes (50 units per tube)
R2	FOD0708R2	Tape and Reel (2500 units per reel)

Marking Information



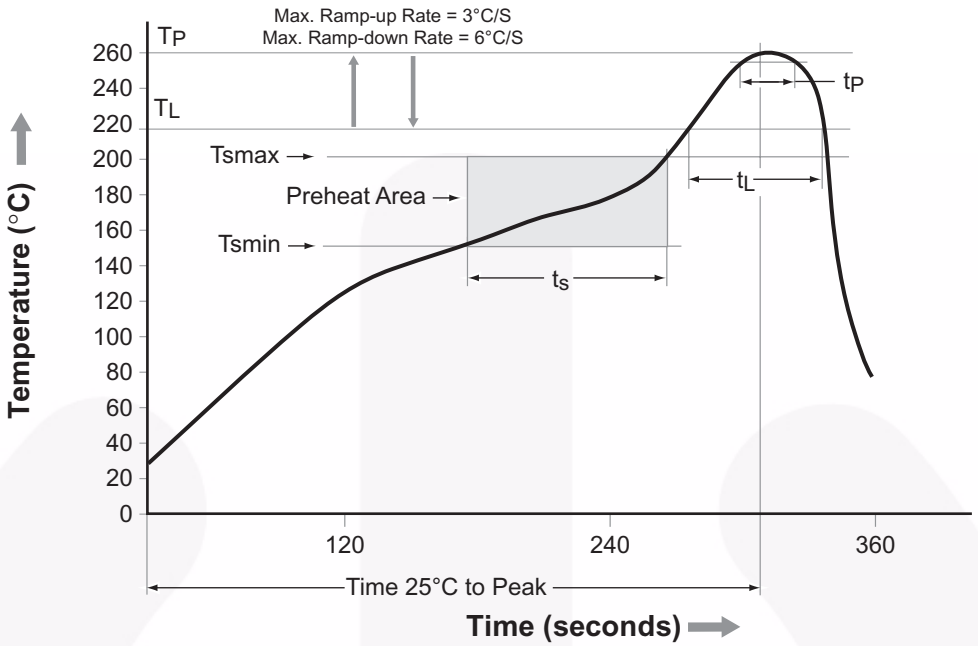
Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., ‘5’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Carrier Tape Specification



Dimensions in mm

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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