ACPL-W70L-000E and ACPL-K73L-000E

Single-channel and Dual-channel High Speed 15 MBd CMOS optocoupler with Glitch-Free Power-Up Feature

Data Sheet

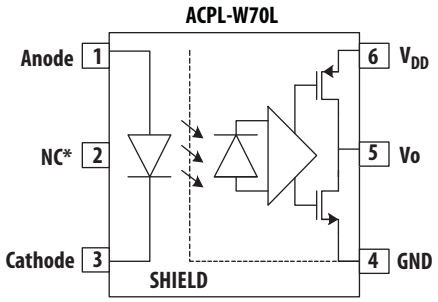
Lead (Pb) Free
RoHS 6 fully compliant

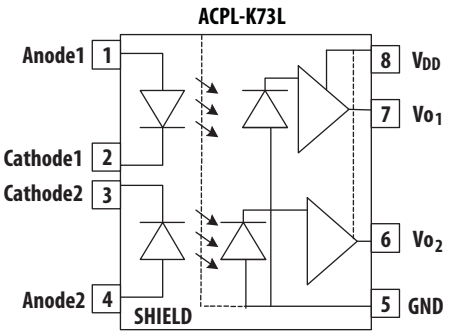
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The ACPL-W70L (single-channel) and ACPL-K73L (dual-channel) are 15 MBd CMOS optocouplers in SSOIC-6 and SSOIC-8 package respectively. The optocouplers utilize the latest CMOS IC technology to achieve outstanding performance with very low power consumption. Basic building blocks of ACPL-W70L and ACPL-K73L are high speed LEDs and CMOS detector ICs. Each detector incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Component Image





TRUTH TABLE

LED	V_O, OUTPUT
OFF	L
ON	H

A 0.1µF bypass capacitor must be connected between pins 4 and 6 for ACPL-W70L and pins 5 and 8 for ACPL-K73L.

Features

- +3.3V and 5 V CMOS compatibility
- 25ns max. pulse width distortion
- 55ns max. propagation delay
- 40ns max. propagation delay skew
- High speed: 15 MBd min
- 10 kV/µs minimum common mode rejection
- –40 to 105°C temperature range
- Glitch-Free Power-UP Feature
- Safety and regulatory approvals:
  - UL recognized: 5000 V rms for 1 min. per UL 1577
  - CSA component acceptance Notice #5
  - IEC/EN/DIN EN 60747-5-2 approved Option 060

Applications

- Digital field bus isolation:
  - CANBus, RS485, USB
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface
- DC/DC converter

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

ACPL-W70L and ACPL-K73L will be UL Recognized with 5000 V_{rms} for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Gull Wing	Tape& Reel	UL 5000 V_{rms}/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-W70L	-000E	SSO-6	X			X		100 per tube
	-500E		X		X	X		1000 per reel
	-060E		X			X	X	100 per tube
	-560E		X		X	X	X	1000 per reel
ACPL-K73L	-000E	SSO-8	X			X		80 per tube
	-500E		X		X	X		1000 per reel
	-060E		X			X	X	80 per tube
	-560E		X		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

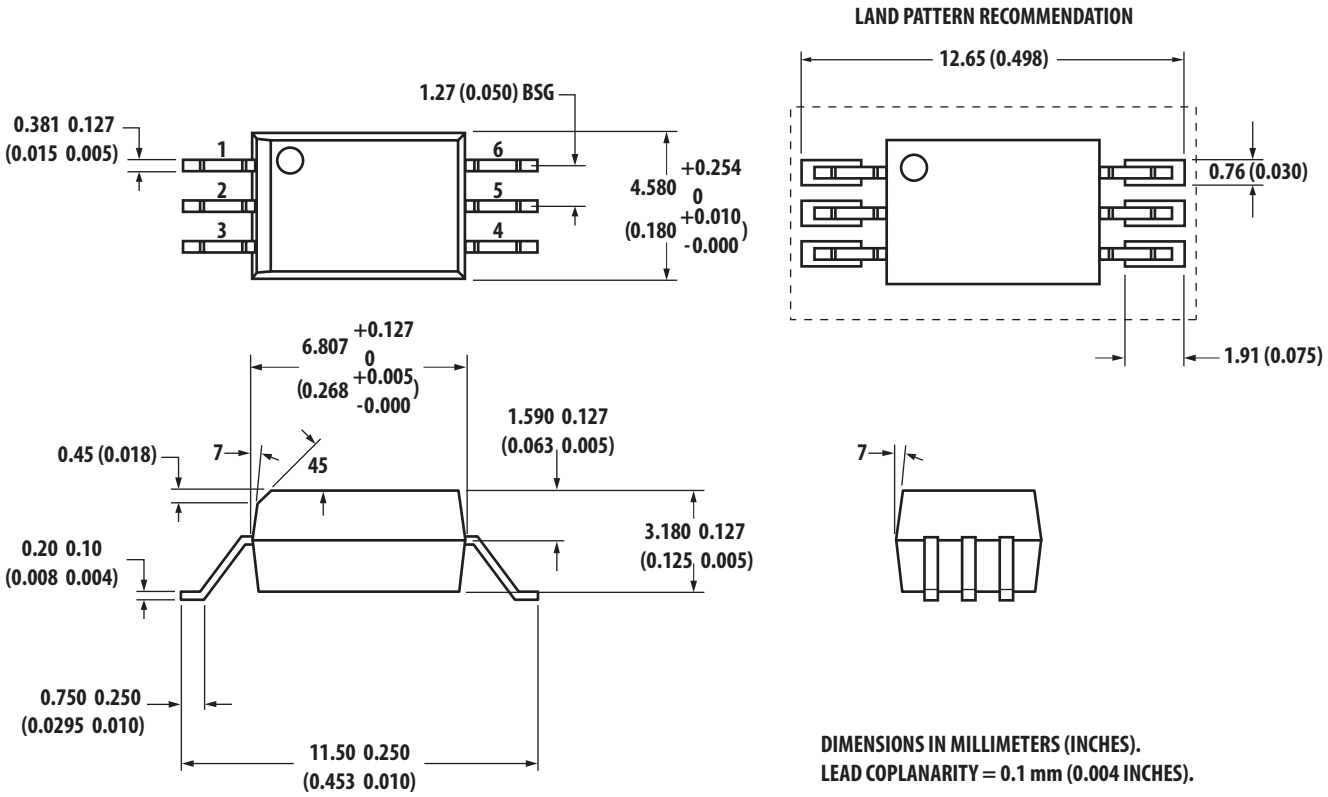
Example 1:

ACPL-W70L-500E to order product of stretched SO-6 package in Tape and Reel packaging in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

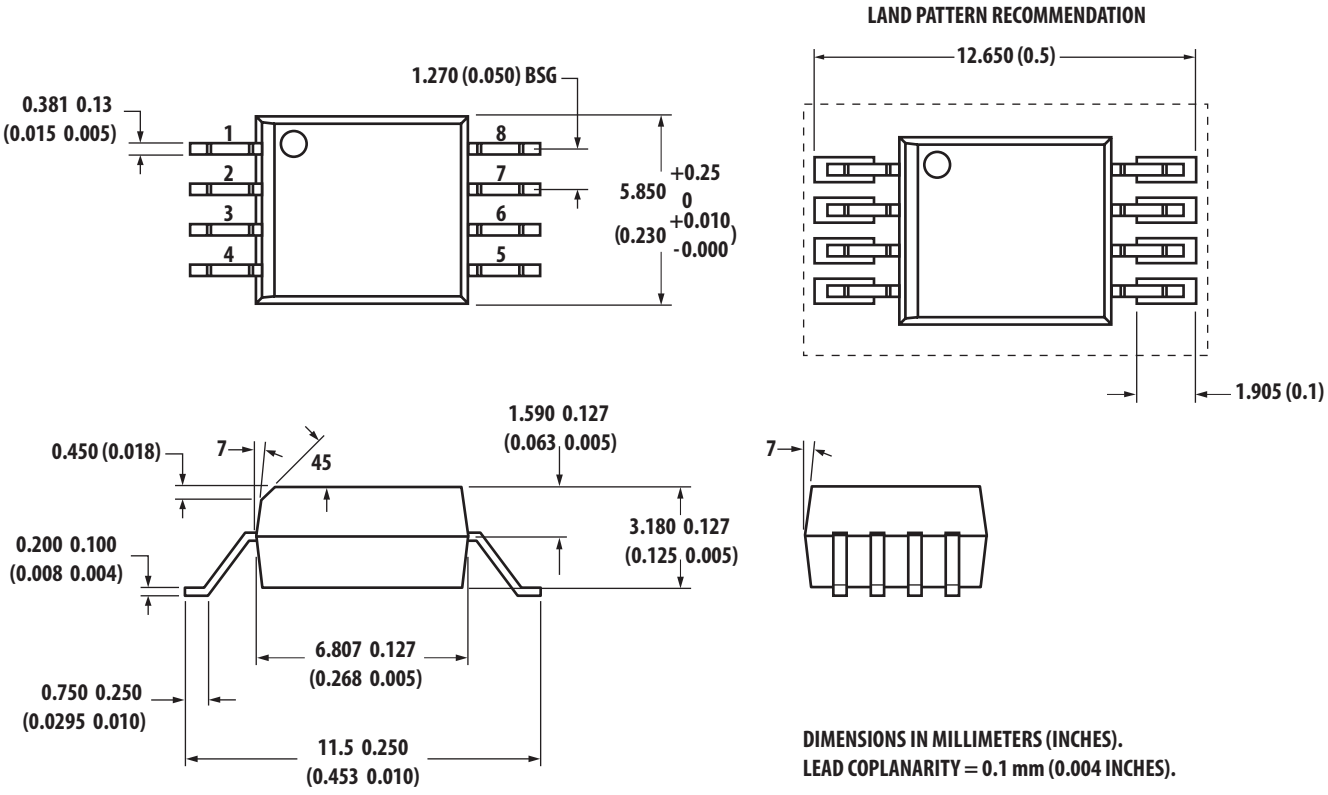
Package Dimensions

ACPL-W70L (Stretched SO-6 Package)



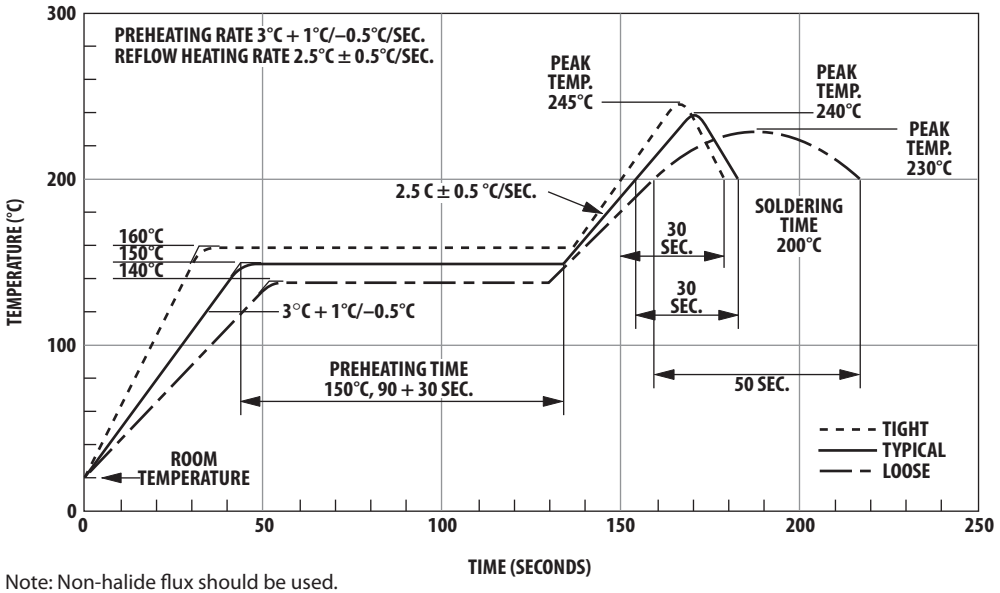
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.1 mm (0.004 INCHES).

ACPL-K73L (Stretched SO-8 Package)



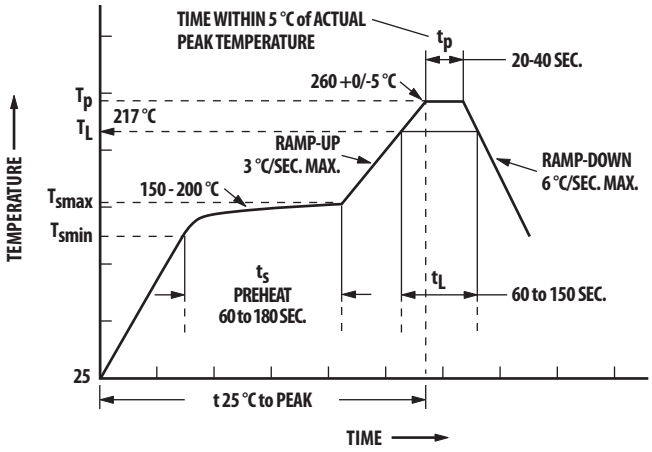
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.1 mm (0.004 INCHES).

Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



Notes:
The time from 25 °C to peak temperature = 8 minutes max.
T_{smax} = 200 °C, T_{smin} = 150 °C
Non-halide flux should be used

Regulatory Information

The ACPL-W70L and ACPL-K73L are approved by the following organizations:

UL

Recognized under UL 1577, component recognition program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA88324.

IEC/EN/DIN EN 60747-5-2

Approval under:

IEC 60747-5-2:1997 + A1:2002

EN 60747-5-2:2001 + A1:2002

DIN EN 60747-5-2 (VDE 0884Teil 2):2003-01 (Option 060 only)

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago Technologies data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered.

There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics*

Description	Symbol	Option 060	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage 150 V_{rms}		I – IV	
for rated mains voltage 300 V_{rms}		I - III	
for rated mains voltage 450 V_{rms}		I – III	
for rated mains voltage 600 V_{rms}		I – III	
for rated mains voltage 1000 V_{rms}		I – III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a** V_{IORM} x 1.5=V_{PR}, Type and Sample Test, t_m=60 sec, Partial discharge < 5 pC	V_{PR}	1710	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure, also see Figure 2.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_{IO}	>109	Ω

Note:

* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

** Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description of Method a and Method b partial discharge test profiles.

These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. The surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	0	6	Volts
Output Voltage	V_O	–0.5	V_{DD} +0.5	Volts
Average Forward Input Current	I_F	-	10	mA
Average Output Current	I_o	-	10	mA
Lead Solder Temperature		260°C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		See Solder Reflow Temperature Profile Section		

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Input Current (ON)	I_F	4	8	mA
Supply Voltage Slew Rate[1]	SR	0.5	500	V/ms

Electrical Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V≤V_{DD} ≤ 3.6V and 4.5 V ≤V_{DD} ≤ 5.5 V.

All typical specifications are at T_A=+25°C , V_{DD}= +3.3V.

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Units	Test Conditions
Input Forward Voltage	V_F		1.2	1.5	1.85	V	I_F = 6 mA
Input Reverse Breakdown Voltage	BV_R		5.0			V	I_R = 10 µA
Logic High Output Voltage	V_{OH}		V_{DD}-1	VDD-0.3		V	I_F = 6 mA, I_O = -4 mA, V_{DD}=3.3 V
			V_{DD}-1	VDD-0.2		V	I_F = 6 mA, I_O = -4 mA, V_{DD}=5 V
Logic Low Output Voltage	V_{OL}			0.2	0.8	V	I_F = 0 mA, I_O = 4 mA, V_{DD}=3.3 V
				0.2	0.8	V	I_F = 0 mA, I_O = 4 mA, V_{DD}=5 V
Input Threshold Current	I_{TH}			1	3	mA	I_{OL} = 20 µA
Logic Low Output Supply Current	I_{DDL}	ACPL-W70L		4.1	6.5	mA	I_F = 0 mA
		ACPL-K73L		8.2	13	mA	I_F = 0 mA
Logic Low Output Supply Current	I_{DDH}	ACPL-W70L		3.8	6	mA	I_F = 6 mA
		ACPL-K73L		7.6	12	mA	I_F = 6 mA

Switching Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V≤V_{DD} ≤ 3.6V and 4.5 V ≤V_{DD} ≤ 5.5 V.

All typical specifications are at T_A=+25°C, V_{DD} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output[2]	t_{PHL}		23	55	ns	I_F = 6 mA, C_L= 15pF CMOS Signal Levels
Propagation Delay Time to Logic High Output[2]	t_{PLH}		27	55	ns	I_F = 6 mA, C_L= 15pF CMOS Signal Levels
Pulse Width	t_{PW}	66.7			ns	
Pulse Width Distortion[3]	|PWD|	0	4	25	ns	I_F = 6 mA, C_L= 15pF CMOS Signal Levels
Propagation Delay Skew[4]	t_{PSK}			40	ns	I_F = 6 mA, C_L= 15pF CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R		3.5		ns	I_F = 6 mA, C_L= 15pF CMOS Signal Levels
Output Fall Time (90% - 10%)	t_F		3.5		ns	I_F = 0 mA, C_L= 15pF CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output[5]	| CM_H |	10	15		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 6 mA
Common Mode Transient Immunity at Logic Low Output[6]	| CM_L |	10	15		kV/µs	V_{CM} = 1000 V, T_A = 25°C, I_F = 0 mA

Package Characteristics

All Typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Insulation	I_{I-O}			1.0	µA	45% RH, t = 5 s V_{I-O} = 3 kV DC, T_A = 25°C
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, T_A = 25°C

Notes:
1. Slew rate of supply voltage ramping is recommended to ensure no glitch more than 1V to appear at the output pin.
2. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level on the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level on the rising edge of the V_O signal.
3. PWD is defined as $|t_{PHL} - t_{PLH}|$.
4. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
5. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
6. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

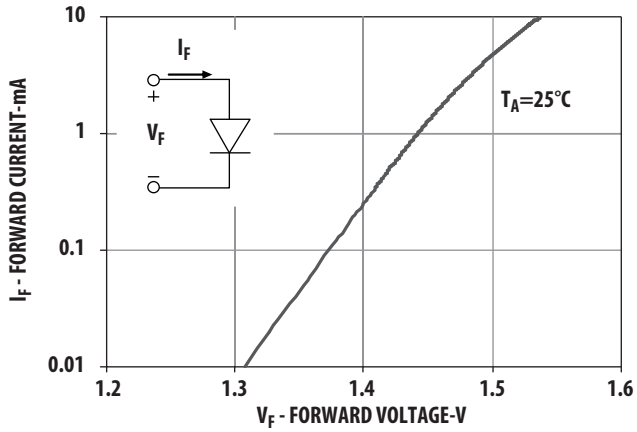


Figure 1. Typical input diode forward characteristic

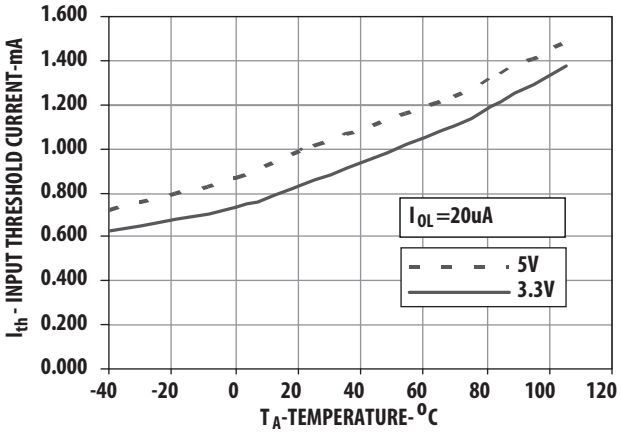


Figure 2. Typical input threshold current vs. temperature

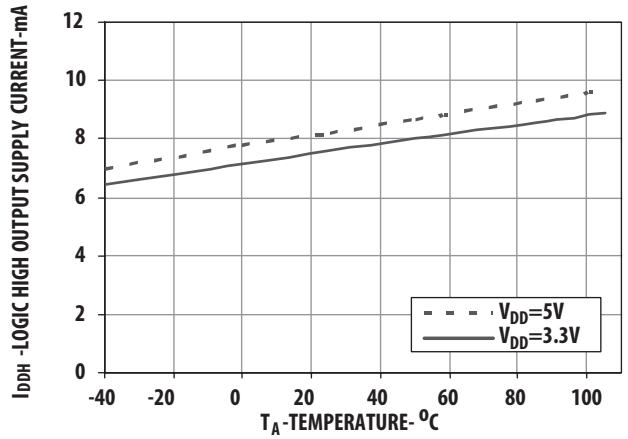


Figure 3. Typical logic high output supply current vs. temperature for dual channel (ACPL-K73L)

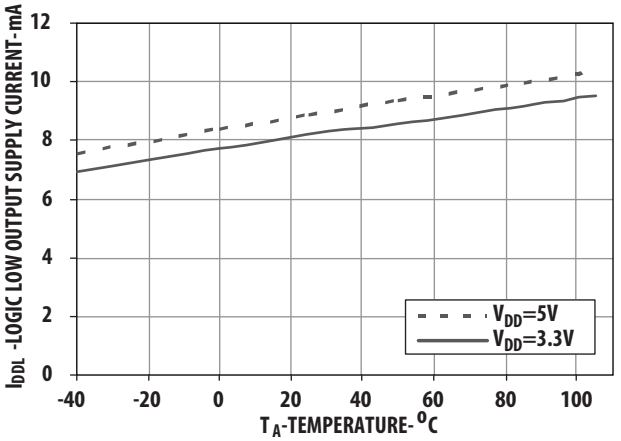


Figure 4. Typical logic low output supply current vs. temperature for dual channel (ACPL-K73L)

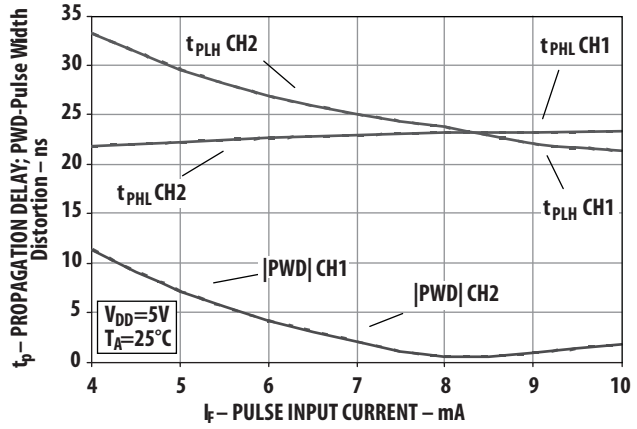


Figure 5. Typical switching speed vs. pulse input current at 5V supply voltage

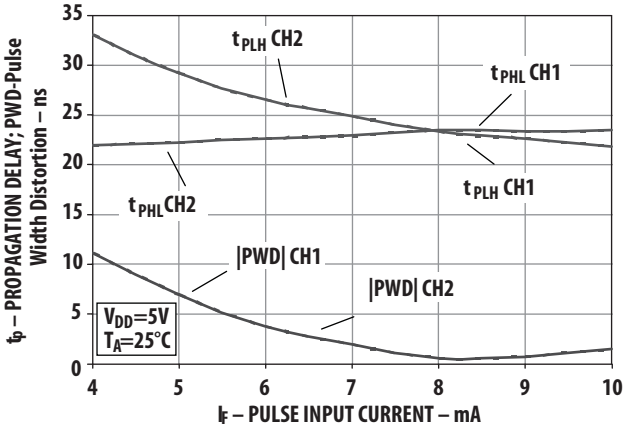


Figure 6. Typical switching speed vs. pulse input current at 3.3V supply voltage

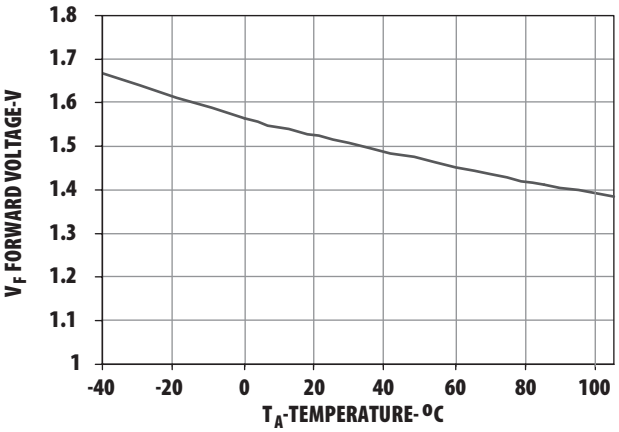


Figure 7. Typical V_F vs. temperature.

Application Information

Bypassing and PC Board Layout

The ACPL-W70L and ACPL-K73L optocouplers are extremely easy to use. ACPL-W70L and ACPL-K73L provide CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistor and the output bypass capacitor. Capacitor values should be between 0.01 µF and 0.1 µF.

For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 9).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern.

If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same

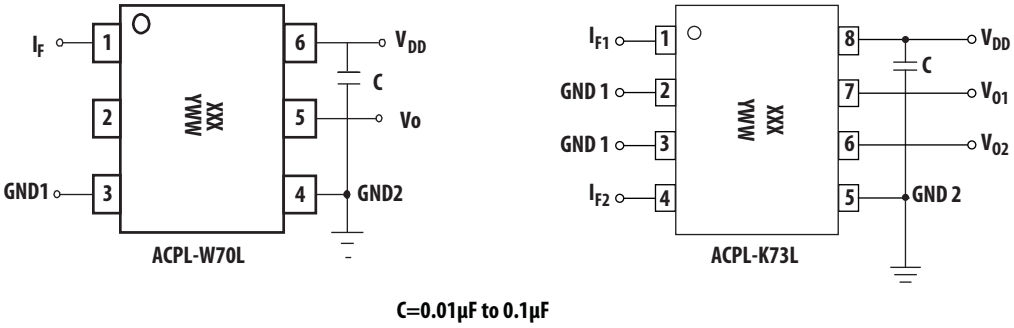


Figure 8. Recommended printed circuit board layout

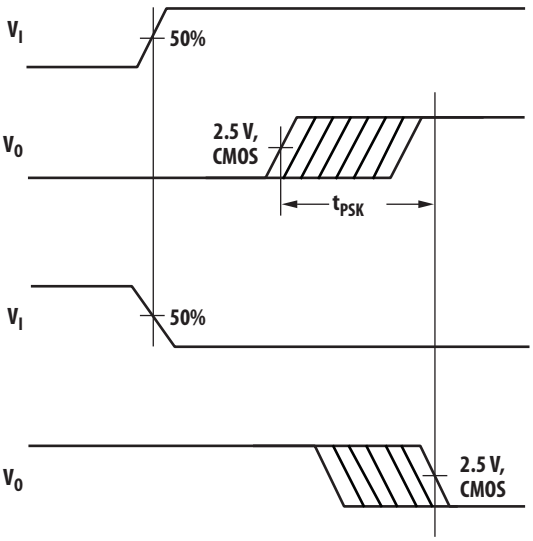


Figure 9. Propagation delay skew waveform

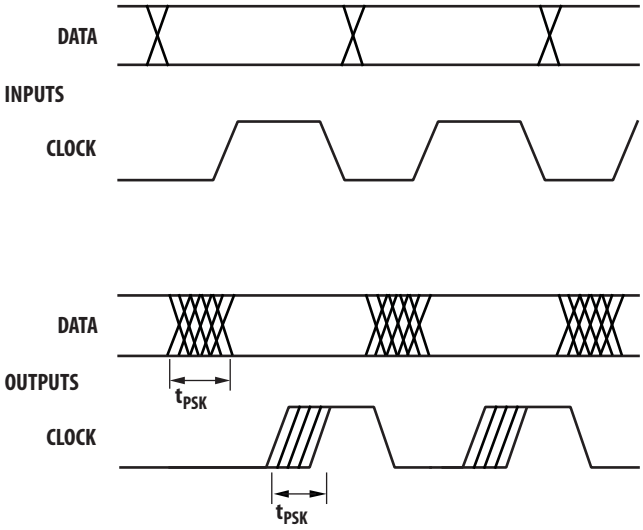


Figure 10. Parallel data transmission example.

time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PHL} or t_{PHL}. As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler.

Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

Powering Sequence

V_{DD} needs to achieve a minimum level of 4.5V before powering up the output connecting component.

Input Limiting Resistor

ACPL-W70L and ACPL-K73L are direct current driven (Figure 8), and thus eliminate the need for input power supply. To limit the amount of current flowing through the LED, it is recommended that a 530ohm resistor is connected in series with anode of LED (i.e. Pin 1 for ACPL-W70L, Pin 1 and P4 for ACPL-K73L) at 5V input signal. At 3.3V input signal, it is recommended to connect 250ohm resistor in series with anode of LED. The recommended limiting resistors is based on the assumption that the driver output impedence is 50Ω (as shown in Figure 11).

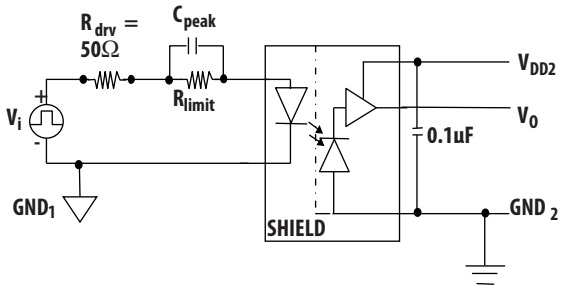
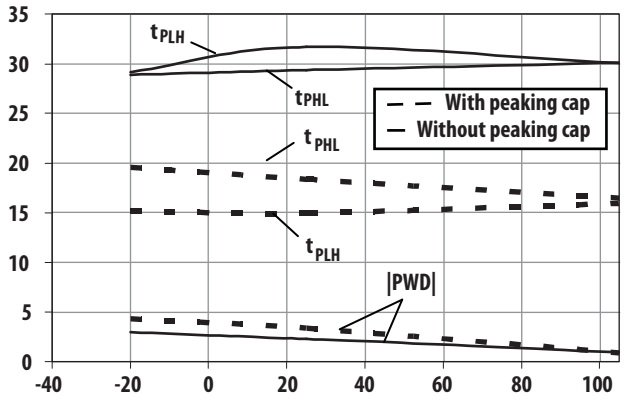


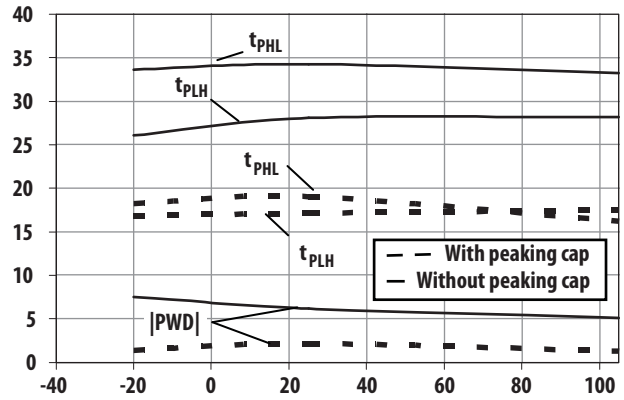
Figure 11. Connection of peaking capacitor (C_{peak}) in parallel of the input limiting resistor (R_{llimit}) to improve speed performance

Speed Improvement

A peaking capacitor can be placed across the input current limit resistor (Figure 11) to achieve enhanced speed performance. The value of the peaking cap is dependent to the rise and fall time of the input signal and supply voltages and LED input driving current (I_f). Figure 12 shows significant improvement of propagation delay and pulse with distortion with added 100pF peak capacitor at driving current of 6mA and 5V power supply.



(i) V_{DD2}=5V, C_{peak}=100pF, R_{limit}=530Ω



(ii) V_{DD2}=3.3V, C_{peak}=100pF, R_{limit}=250Ω

Figure 12. Improvement of t_p and PWD with added 100pF peaking capacitor in parallel of input limiting resistor.

Common Mode Rejection for ACPL-W70L AND ACPL-K73L

Figure 13 shows the recommended driving circuit for the ACPL-W70L and ACPL-K73L for optimal common-mode rejection performance. Two LED-current setting resistors are used instead of one. This is to balance the common mode impedance at LED anode and cathode. Common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure14 shows the parasitic capacitances which exists between LED anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 14 on the input side is an AC-equivalent circuit.

Table 1 indicates the directions of I_{LP} and I_{LN} flow depending on the direction of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_L, since the output is in the "low" state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CM_L also depends on the extent which I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F (i.e. when $dV_{CM}/dt>0$ and $|I_{FP}| > |I_{FN}|$, referring to Table 1) will cause common-mode failure for transients which are fast enough.

Likewise for common-mode transients which occur when the LED is off (i.e. CM_H, since the output is "high"), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike below 2V (which constitutes a CM_H failure).

By using the recommended circuit in Figure 13, good CM_R can be achieved. The resistors recommended in Figure 13 include both the output impedence of the logic driver circuit and the external limiting resistor. The balanced I_{LED}-setting resistors help equalize the common mode voltage change at anode and cathode to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

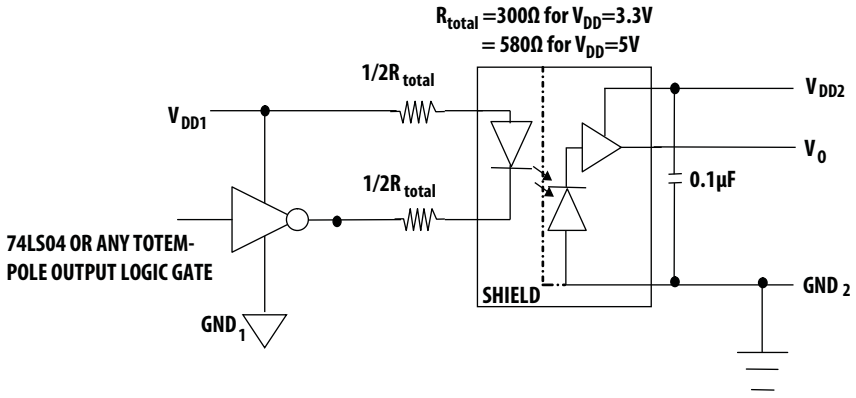


Figure 13. Recommended drive circuit for ACPL-W70L and ACPL-K73L for high-CMR

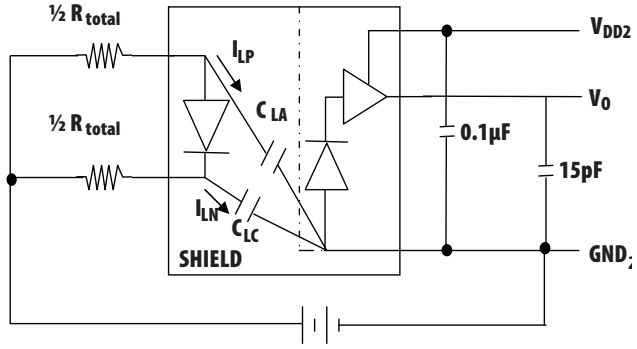


Figure 14. AC equivalent of ACPL-W70L and ACPL-K73L

Table 1. Effects of Common Mode Pulse Direction on Transient I_{LED}

If dV_{CM}/dt Is:	then I_{LP} Flows:	and I_{LN} Flows:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:
positive (>0)	away from LED anode through C_{LA}	away from LED cathode through C_{LC}	increased	decreased
negative (<0)	toward LED anode through C_{LA}	toward LED cathode through C_{LC}	decreased	increased

CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 13 may be enhanced by following these guidelines:

1. Use of drive circuits where current is shunted from the LED in the LED "off" state (as shown in Figures 15 and 16). This is beneficial for good CM_H.
2. Use of typical I_{FH} = 6mA per datasheet recommendation.

Using any one of the drive circuits in Figures 15-17 with I_F = 6 mA will result in a typical CMR of 10 kV/µs for ACPL-W70L AND ACPL-K73L, as long as the PC board layout practices are followed. Figure 15 shows a circuit which can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices which have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

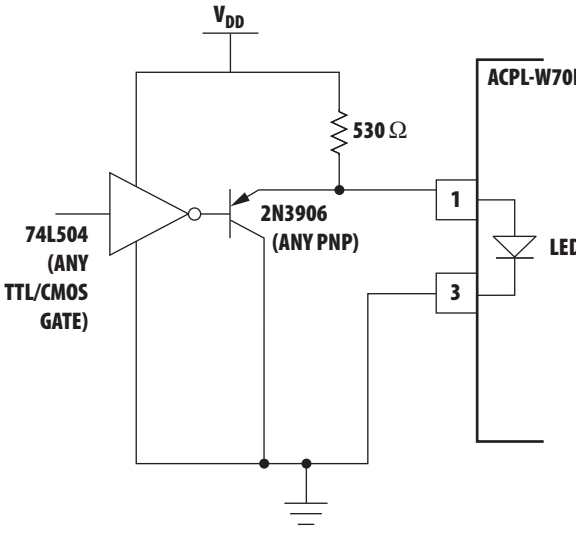


Figure 15. TTL interface circuit for the ACPl-W70L families.

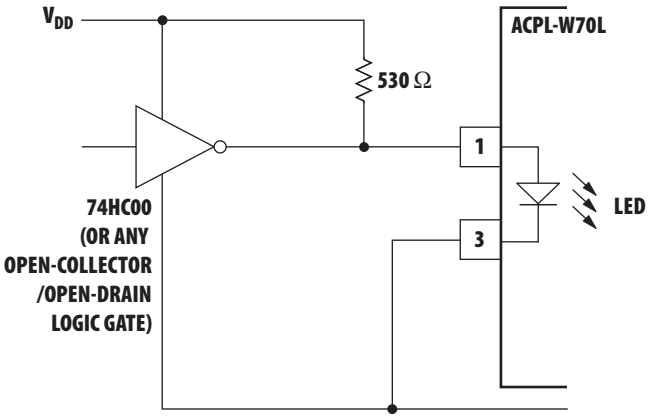


Figure 16. TTL open-collector/open drain gate drive circuit for ACPL-W70L families.

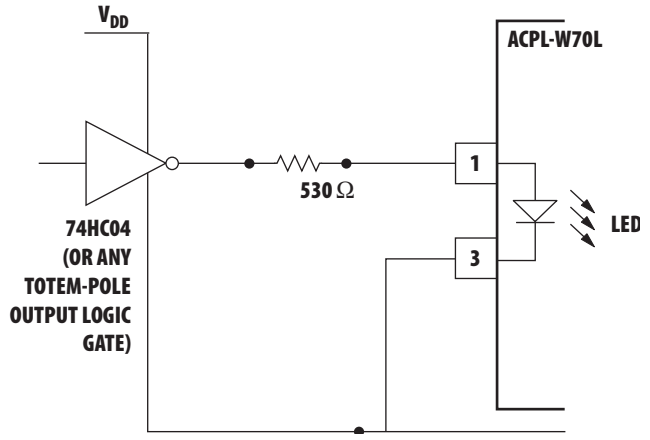


Figure 17. CMOS gate drive circuit for ACPL-W70L families.

When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 16 may be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 17, where the resistor is recommended to connect to the anode of the LED, may be used.

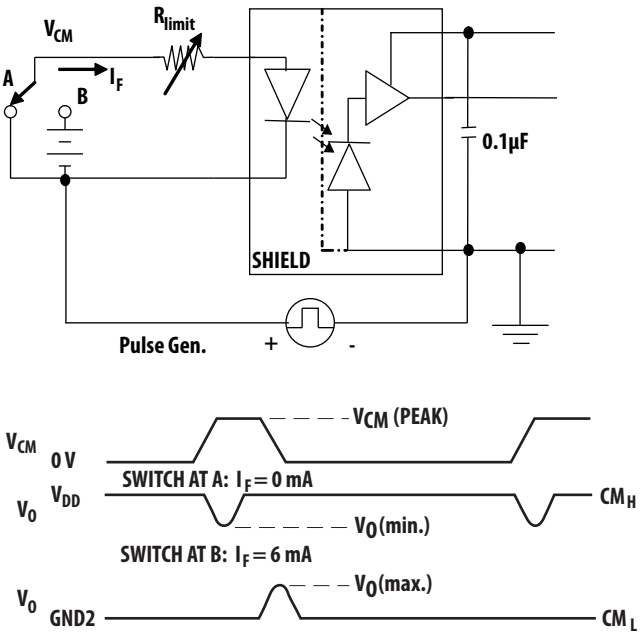


Figure 18. Test circuit for common mode transient immunity and typical waveforms.

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