ACPL-W611/ACPL-P611

High CMR, High Speed TTL Compatible Optocoupler

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

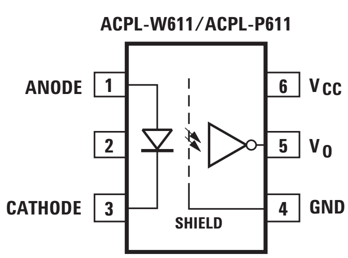
Description

The ACPL-W611/ACPL-P611 is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 10,000 V/µs for the ACPL-W611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing trouble-free system performance.

The ACPL-W611/ACPL-P611 is suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Functional Diagram



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins V_{CC} and GND.

Features

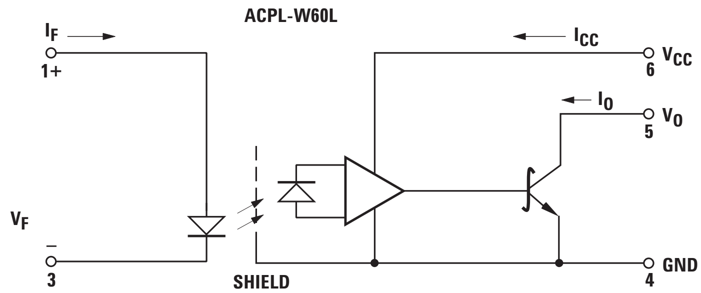
- 10 kV/µs minimum Common Mode Rejection (CMR) at VCM = 1000 V
- High speed: 10 MBd typical
- LSTTL/TTL compatible
- Low input current capability: 5 mA
- Guaranteed ac and dc performance over temperature: -40°C to +85°C
- Stretched SO-6 package
- Safety Approval:
  - UL Recognized:
    5000Vrms for 1 minute for ACPL-W611 and ACPL-P611-020E per UL1577
  - CSA
  - IEC/EN/DIN EN 60747-5-2

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Power transistor isolation in motor drives
- Isolation of high speed logic systems

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Schematic Diagram



Ordering Information

ACPL-P611 is UL Recognized with 3750Vrms for 1 minute and ACPL-W611 is UL recognized with 5000Vrms for 1 minute per UL1577. They are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-P611	-000E	Stretched SO-6	X				100 per tube
	-020E		X		X		100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1000 per reel
	-520E		X	X	X		1000 per reel
	-560E		X	X		X	1000 per reel
ACPL-W611	-000E	Stretched S0-6	X		X		100 per tube
	-060E		X		X	X	100 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

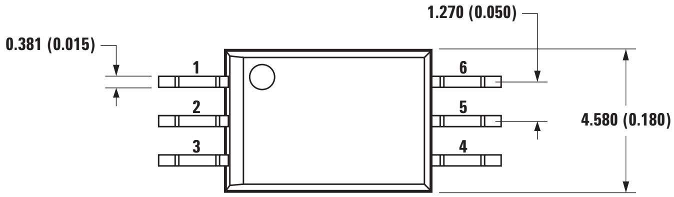
Example 1:

HCPL-P611-500E to order product of Surface Mount Stretched SO-6 package in Tape and Reel packaging with RoHS compliant.

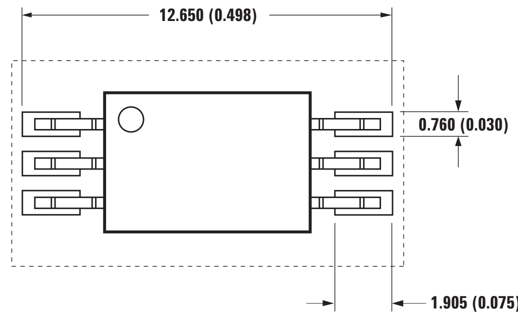
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

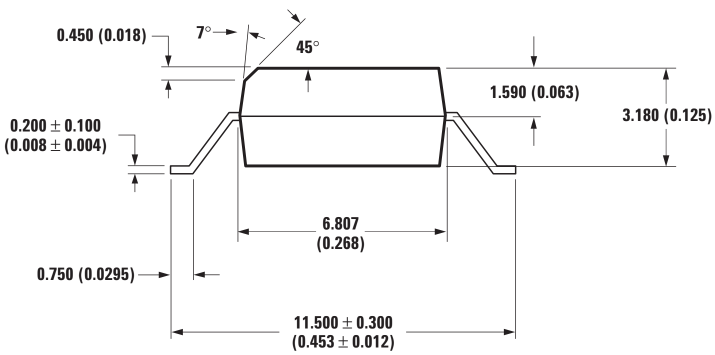
Package Outline Drawings

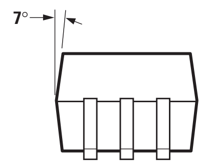
ACPL-W611 Stretched SO-6 Package



LAND PATTERN RECOMMENDATION

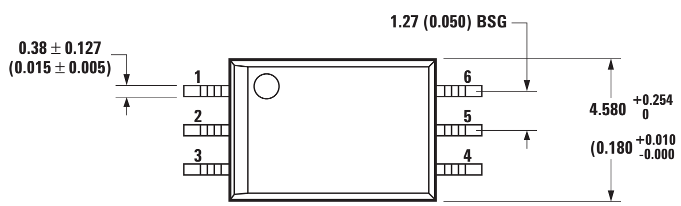




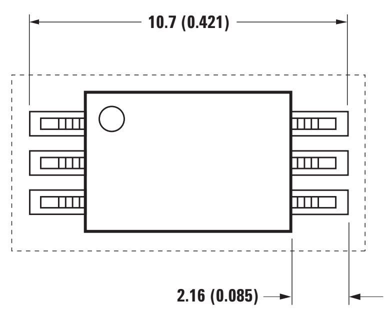


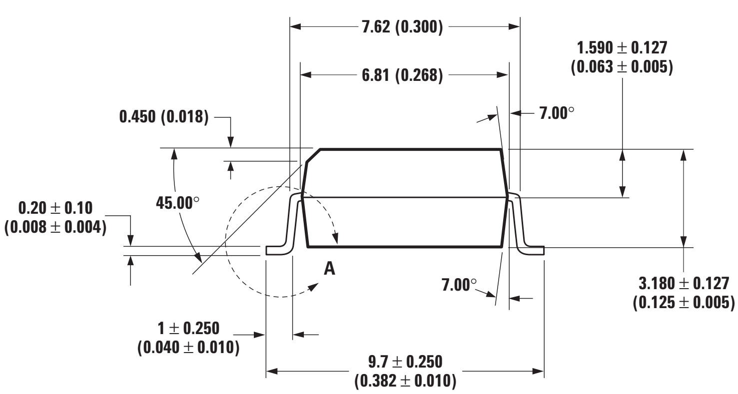
DIMENSIONS IN MILLIMETERS AND (INCHES).
COPLANARITY = 0.10 mm (0.004 INCHES).

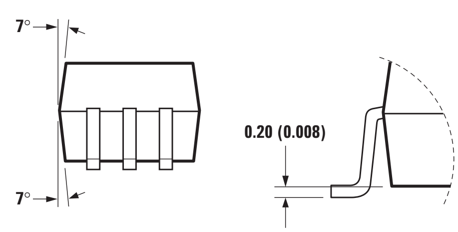
ACPL-P611 Stretched SO-6 Package



LAND PATTERN RECOMMENDATION



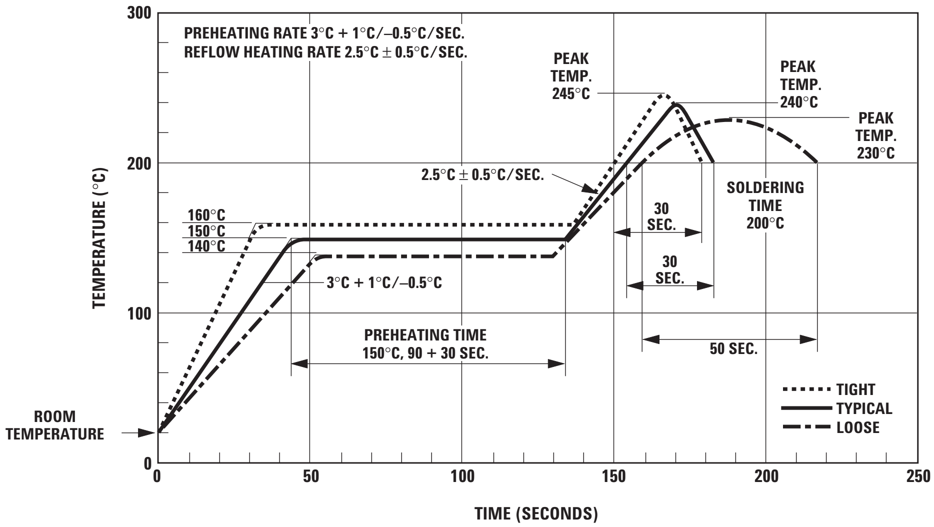




DETAIL A

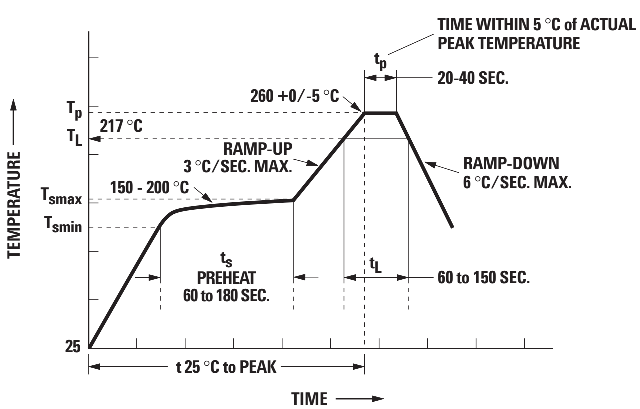
DIMENSIONS IN MILLIMETERS AND (INCHES).
COPLANARITY = 0.10 mm (0.004 INCHES).

Recommended Solder Reflow Thermal Profile



Note: Use of non chlorine-activated fluxes is highly recommended.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Use of non chlorine-activated fluxes is highly recommended.

Regulatory Information

The ACPL-W611 and ACPL-P611 is approved/pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-2 (Option 060 only)

Approval under:
IEC 60747-5-2 :1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

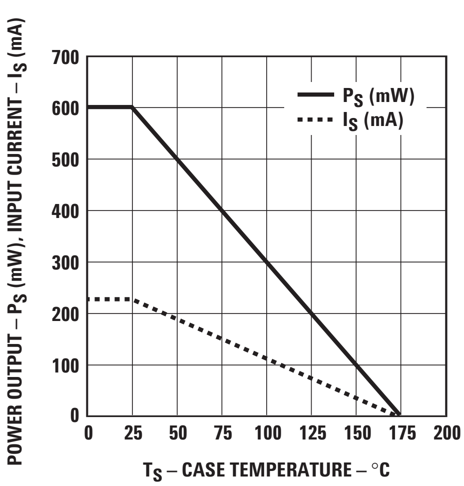
Parameter	Symbol	ACPL-P611	ACPL-W611	Units	Conditions
Minimum External Air Gap Clearance)	L(101)	7	8	mm	Measured from input (External terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics* (ACPL-W611/ ACPL-P611 Option 060)

Description	Symbol	ACPL-P611 Option 060	ACPL-W611 Option 060	Unit
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – III	I – III	
for rated mains voltage ≤ 600 V_{rms}		I – III	I – III	
for rated mains voltage ≤ 1000 V_{rms}			I – III	
Climatic Classification		55/85/21	55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1670	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5=V_{PR}, Type and Sample Test, t_m=60 sec, Partial discharge < 5 pC	V_{PR}	1425	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	175	°C
Input Current**	$I_{S, INPUT}$	230	230	mA
Output Power**	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Average Input Current	$I_{F(AVG)}$		20	mA
Reverse Input Voltage	V_R		5	V
Input Power Dissipation	P_I		45	mW
Supply Voltage (1 Minute Maximum)	V_{CC}		7	V
Output Collector Current	I_O		50	mA
Output Collector Voltage	V_O		7	V
Output Collector Power Dissipation	P_O		85	mW
Lead Solder Temperature	T_{LS}		260°C for 10 sec.	
Solder Reflow Temperature Profile	See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature	T_A	- 40	85	°C
Fan Out (at R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified. All typicals at V_{CC} = 5 V, T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	1	
Input Threshold Current	I_{TH}		2.0	5.0	mA	V_{CC} = 5.5 V, V_O = 0.6 V, I_{OL} > 13 mA	13	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, $I_{OL(Sinking)}$ = 13 mA	2, 4, 5,13	
High Level Supply Current	I_{CCH}		4	7.5	mA	V_{CC} = 5.5 V, I_F = 0 mA,		
Low Level Supply Current	I_{CCL}		6	10.5	mA	V_{CC} = 5.5 V, I_F = 10 mA,		
Input Forward Voltage	V_F	1.4 1.3	1.5	1.75 1.8	V	T_A = 25 °C I_F = 10 mA	3	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA	12	

All typicals at T_A = 25°C, V_{CC} = 5 V

Switching Specifications (AC)

Over recommended operating conditions T_A = -40°C to 85°C, V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified. All typicals at V_{CC} = 5 V, T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75 100	ns	T_A = 25°C	R_L = 350 Ω, C_L = 15 pF		5
Propagation Delay Time to Low Output Level	t_{PHL}	25	50	75 100	ns	T_A = 25°C			6
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$		3.5	35	ns	R_L = 350 Ω, C_L = 15 pF			10
Propagation Delay Skew	t_{PSK}			40	ns				10, 11
Output Rise Time (10%-90%)	t_R		24		ns				
Output Fall Time (10%-90%)	t_F		10		ns				
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	10	15		kV/μs	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V		7, 9	
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	10	15		kV/μs	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C, V_{CM} = 1000 V			8, 9

Package Characteristics

All typicals at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	V_{ISO}	3750			V_{rms}	RH < 50% for 1 min. T_A = 25°C		3, 4
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, T_A = 25 °C		3

Notes:

1. Bypassing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2 and 3 shorted together, and pins 4, 5 and 6 shorted together.
4. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (Leakage detection current limit, I_{I-O} ≤ 5 μA).
5. The t_{PLH} propagation delay is measured from 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{PHL} propagation delay is measured from 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} > 0.8 V).
9. For sinusoidal voltages, $(|dV_{CM}|/dt)_{max} = \pi f_{CM} V_{CM(p-p)}$.
10. See application section; "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
11. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the worst case operating condition range.

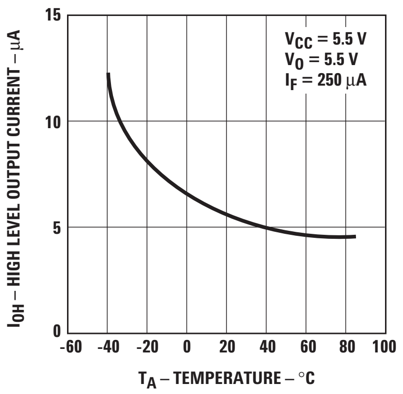


Figure 1. High level output current vs. temperature

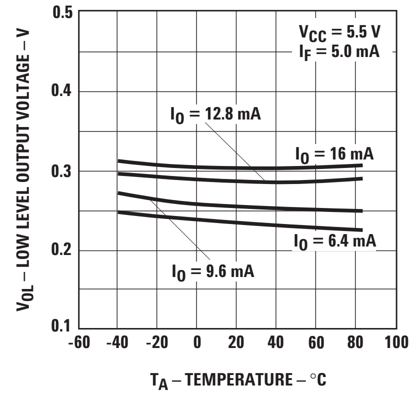


Figure 2. Low level output voltage vs. temperature

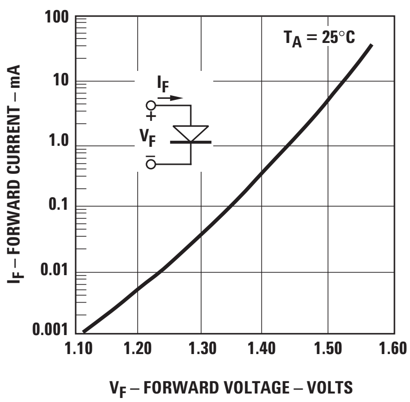


Figure 3. Input diode forward characteristic

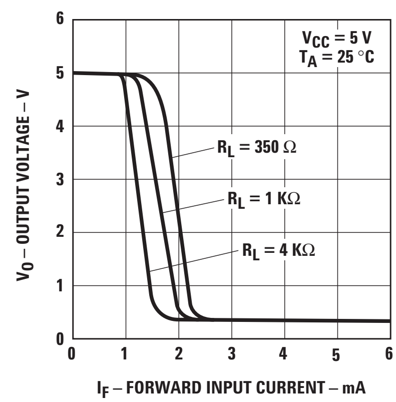


Figure 4. Output voltage vs. forward input current

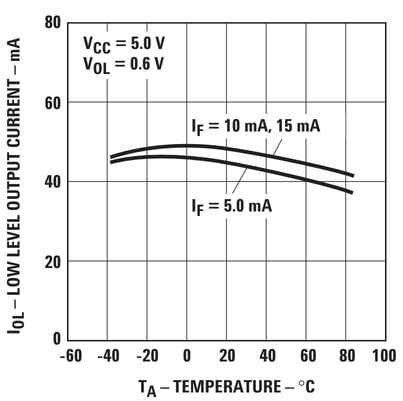


Figure 5. Low level output current vs. temperature

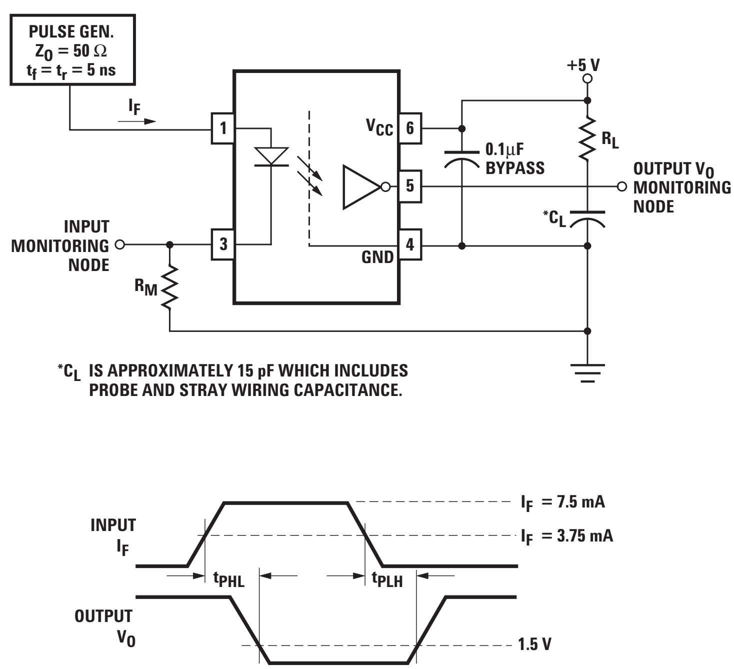


Figure 6. Test circuit for t_{PHL} and t_{PLH}

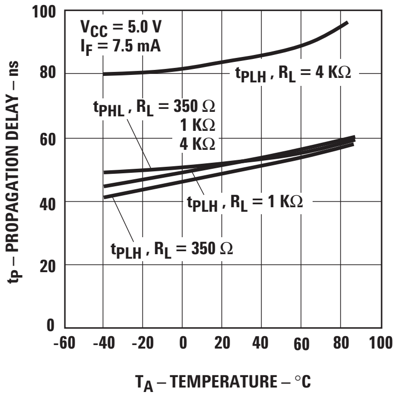


Figure 7. Propagation delay vs. temperature

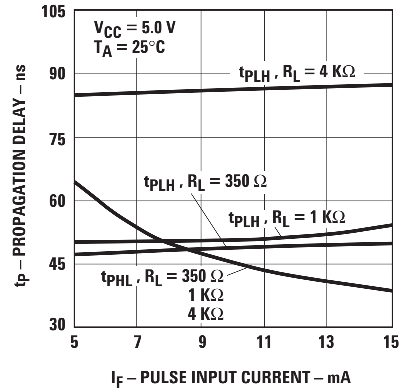


Figure 8. Propagation delay vs. pulse input current

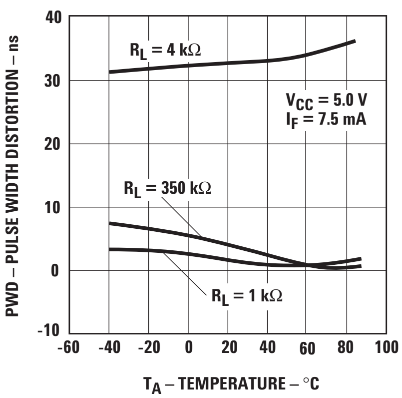


Figure 9. Pulse width distortion vs. temperature

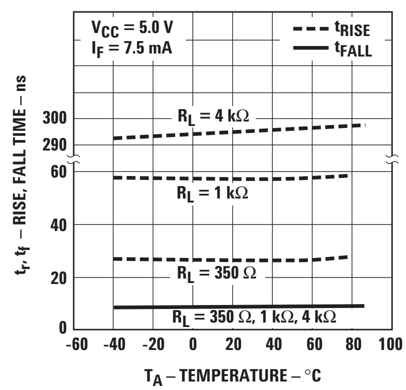


Figure 10. Rise and fall time vs. temperature

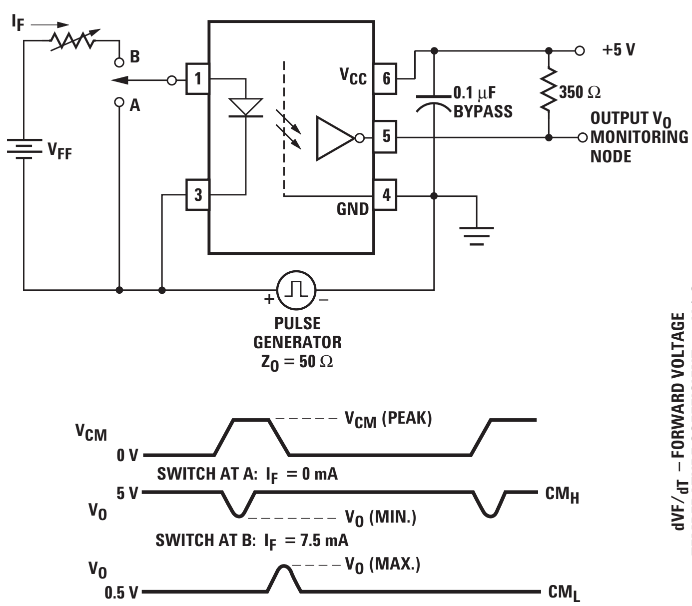


Figure 11. Test circuit for common mode transient immunity and typical waveforms

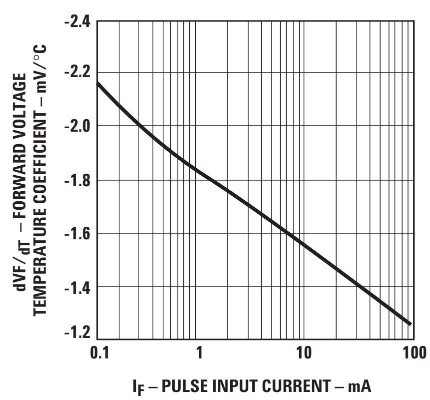


Figure 12. Temperature coefficient for forward voltage vs. input current

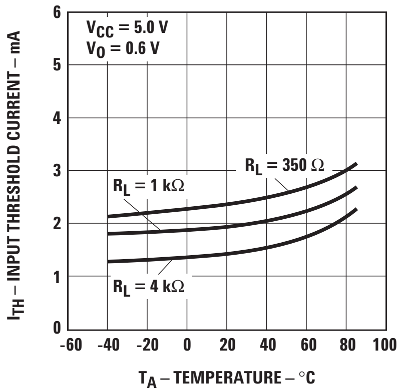


Figure 13. Input threshold current vs. temperature

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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