Intel® TXN31011 Tri-rate LC SFF Optical Transceiver

Datasheet

The LC Small Form Factor (SFF) optical transceivers are high performance modules for bi-directional communication over multi-mode optical fiber. The Intel® TXN31011 Tri-rate LC SFF Optical Transceiver (hereafter called the TXN31011 Optical Transceiver) is specifically designed for high-speed multi-rate operation. The TXN31011 Optical Transceiver is provided with an LC receptacle that is compatible with the industry standard LC connector. The TXN31011 Optical Transceiver, with a single 3.3 V supply, provides double port densities by enabling twice the number of transceivers to fit onto the same board as compared to a 1x9 transceiver. The TXN31011 Optical Transceiver is Class 1 Laser Product compliant with FDA Radiation Performance Standards, 21 CFR Subchapter J.

Product Features

- Compliant with 1x and 2x Fibre Channel (1.0625/2.125 Gbps) FC-PI standard
- Compliant with 1.25 Gbps Gigabit Ethernet standard
- Compliant with 2.5 Gbps Infiniband standard
- Compliant with SFF MSA specification
- 850 nm VCSEL emitter
- TTL Signal Detect Output termination
- Transmitter Disable Input
- AC-coupled CML level Input/Output
- Single +3.3 V Power Supply
- Class 1 Laser Product
- UL 60950 Approved

Applications

- Fibre Channel Host Bus Adapters
- iSCSI Host Bus Adapters
- Ethernet Network Interface Cards

Order Number: 280050, Revision: 003
07 Feb 2005

Contents

Figures

Tables

Revision History

Date	Revision	Description
07 Feb 2005	003	Modified Table 3 “Electrical Characteristics” on page 5: added Power Dissipation values.
19 Aug 2004	002	Updated the Transceiver Electrical Characteristics Table by removing Inrush Current dataTable 3 “Electrical Characteristics” on page 5 Updated the CML Maximum Values: Table 4 “Transmitter - Electrical” on page 6 • Single Ended, was 1100 • Differential, was 2200 Updated the CML Maximum Values: Table 5 “Receiver - Electrical” on page 6 • Single Ended, was 600 • Differential, was 1200 • Output rise/fall time, was 140 CML Minimum Values: • Single Ended, was 300 • Differential, was 600 Total Jitter (pk-pk): • Typical, was <65 • Max, was 130 Adjusted Note, was 500 Waveforms Updated the Transmitter - Optical Table:Table 7 “Transmitter - Optical” on page 7 • Note was Average Launch Power Total Jitter: • Typical, was <65 • Max, was 130 • Note was 500 Waveforms Updated the Receiver - Optical Table: Table 7 “Transmitter - Optical” on page 7 • Reversed values for Typical • Removed Jitter Row Removed extraneous information from CML Termination Section 3.1, “CML Termination” on page 9
20 Jul 2004	001	Initial release.

1.0 Specifications

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	°C	–
Relative Humidity	R_H	5	95	%	–
Soldering Temperature	–	–	260	°C	10 seconds on leads only
Module Supply Voltage	V_{CC}T, R	-0.5	4	V	–
Data AC Voltage	TD+, TD-	–	2.6	V_{PP}	Differential
Control Input Voltage	V_I	-0.5	V_{CC} + 0.3	V	–

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Case Temperature	T_C	-10	–	70	°C
Module Supply Voltage	V_{CC}T, R	2.97	3.3	3.63	VDC
Data Rate	–	1.0625	–	2.5	Gb/s

Table 3. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}	–	150	180	mA	Tc = 25 °C, V_{CC} = 3.3 V
	I_{CC}	–	–	200	mA	0° C < T_C < 70° C, 2.97 V < Vcc < 3.63 V
Power Dissipation	Pdiss	–	450	726	mW	0° C < TC < 70° C, 2.97 V < Vcc < 3.63 V
Supply Noise Rejection	–	100	–	–	mV	10 kHz to 4 MHz with supply filter
Time from de-assertion of TX_OFF	–	–	–	500	µs	Stable laser power at >90% average output power
Time from optical input assertion to Signal Detect asserted	–	–	–	100	µs	–
Time from optical input assertion to stable Rx output	–	–	–	50	µs	–

1.1 Specifications - Electrical

0C < Tc < 70C, 2.97 V < Vcc < 3.63 V

Table 4. Transmitter - Electrical

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
CML Input (Single Ended)	–	200	–	1000	mVpp	AC Coupled Input
CML Input (Differential)	–	400	–	2000	mVpp	AC Coupled Input
Input Impedance (differential)	Z_{IN}	85	100	115	Ω	–
TX_DISABLE input voltage - High	V_{IH}	2	–	Vcc + 0.3	V	–
TX_DISABLE input voltage - Low	V_{IL}	0	–	0.8	V	–

Table 5. Receiver - Electrical

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
CML Output (Single Ended)	–	275	350	450	mVpp	AC Coupled Output, 50 Ω load
CML Output (Differential)	–	550	700	900	mVpp	AC Coupled Output
CML Output (Rise/Fall Time)	–	–	110	150	ps	–
Output Impedance (Differential)	Zout	110	120	130	Ω	–
Total Jitter (pk-pk)	TJ	–	–	65	Ps	See Note
TTL Signal Detect Output - Low	SDoutL	0	–	0.8	V	IOL = -1.2 mA, internal 8 k Ω load to V_{cc}
TTL Signal Detect Output - High	SDoutH	2.0	–	Vcc + 0.3	V	IO = 30 µA
NOTE: Peak-to-peak jitter measured by Agilent* DCA with 2.7 GHz plug-in. 2^7-1 PRBS pattern. 100 waveforms at -12 dBm optical input power.						

Table 6. Fiber Length

Parameter	Symbol	Min	Typ.	Max.	Units	Notes
50 µm/125 µm MMF	–	300 550	500 1000	–	m	BER < 1.0E -12 @ 2.125 Gbps BER < 1.0E -12 @ 1.0625 Gbps
62.5 µm/125 µm MMF	–	200 300	300 500	–	m	BER < 1.0E -12 @ 2.125 Gbps BER < 1.0E -12 @ 1.0625 Gbps

Table 7. Transmitter - Optical

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Optical Transmit Power	Popt	-8	-5	-4	dBm	Average Launch Power, Beginning of Life -4 to -6 dBm
Optical Center	l	830	850	860	nm	–
Spectral Width	△λ	–	–	0.85	nm	RMS
Optical Modulation Amplitude	OMA	250	–	–	µW	pk-pk
Extinction Ratio	ER	9	–	–	dB	–
Relative Intensity Noise	RIN	–	–	-118	dB/Hz	–
Total Jitter	TJ	–	–	65	ps	pk-pk jitter measured by Agilent DCA. 100 Waveforms 2^7 - 1 PRBS
Output Rise/Fall Time	t_R, t_F	–	–	150	ps	20 - 80% values, measured unfiltered

Table 8. Receiver - Optical

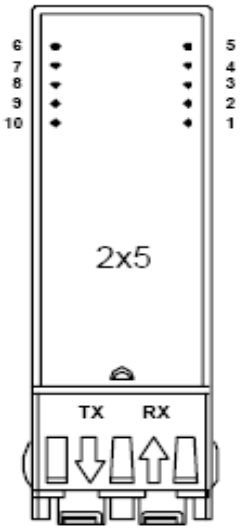
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Optical Input Wavelength	l	770		860	nm	–
Receiver Sensitivity	Pr	-19 -17	-22 -20	–	dBm	1.0625Gb/s 2.125Gb/s Test condition: 10^{-12} BER, 9dB ER input, 2^7 - 1 PRBS.
Receiver Overload	–	0	–	–	dBm	–
Optical Return Loss	ORL	12	30	–	dB	–
Signal Detect - Asserted	Pa	–	–	-17	dB	Measured on transition - low to high
Signal Detect - De-asserted	Pd	-29	–	–	dBm	Measured on transition - high to low
Signal Detect - Hysteresis	Pa - Pd	1	–	5	dB	–

2.0 Electrical Interface

Table 9. Pin Assignment

Pin No.	Description	Interface Type
1	Receiver Ground	Signal ground
2	Receiver +3.3 V Power	Power
3	Signal Detect	TTL output
4	Receiver Data Inverted	CML output
5	Receiver Data	CML output
6	Transmitter +3.3 V Power	Power
7	Transmitter Ground	Signal ground
8	Transmit Disable	TTL input
9	Transmit Data	CML input
10	Transmit Data Inverted	CML input

Figure 1. Pin Layout



TOP VIEW

3.0 Termination

The TXN31011 Optical Transceiver has the following two types of I/O interfaces:

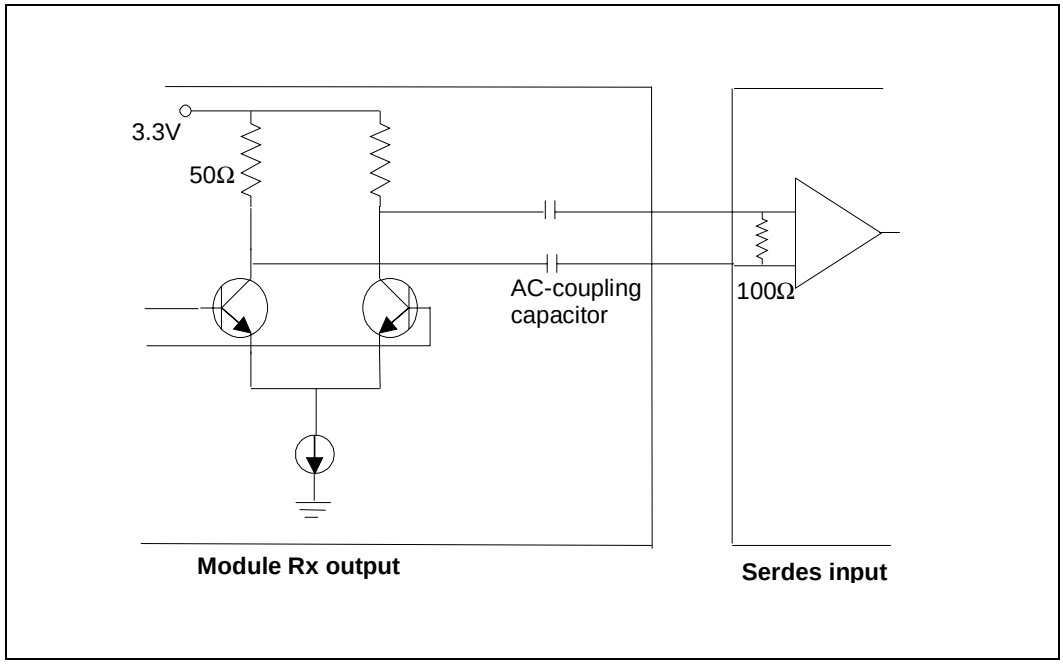
- CML Interface
- TTL Interface

The high speed I/Os use the CML interface, while the control signals use the TTL interface. Proper termination is critical to ensure good signal integrity. Without the proper termination (particularly on the CML I/Os), jitter increases significantly due to reflection from the impedance mismatches.

3.1 CML Termination

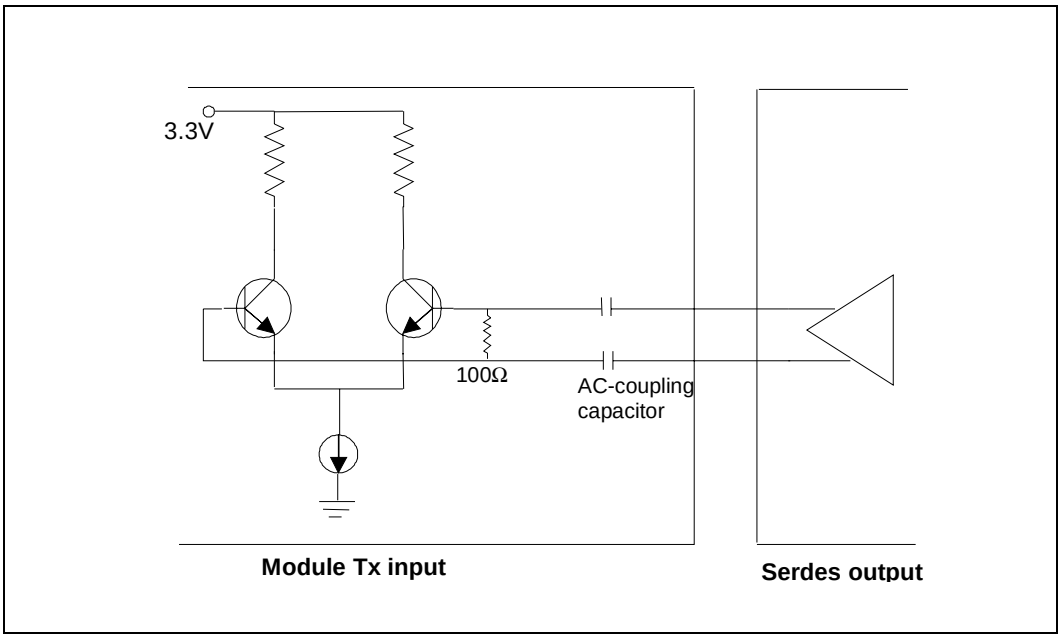
AC-coupling capacitors are built into the TXN31011 Optical Transceiver.

Figure 2. Circuit Diagram for CML Termination on Receiver Output



Most of the SerDes comes with the internal termination resistor. Please check the SerDes specification sheet for proper external termination.

Figure 3. Circuit Diagram for CML Termination on Transmitter Input



The TXN31011 Optical Transceiver Tx input has an internal 100 Ω termination between two inputs. AC-coupling capacitors are also built into the TXN31011 Optical Transceiver.

Note: Make sure the SerDes output has the proper termination. If not, follow the suggestion of the SerDes Datasheet for proper external termination.

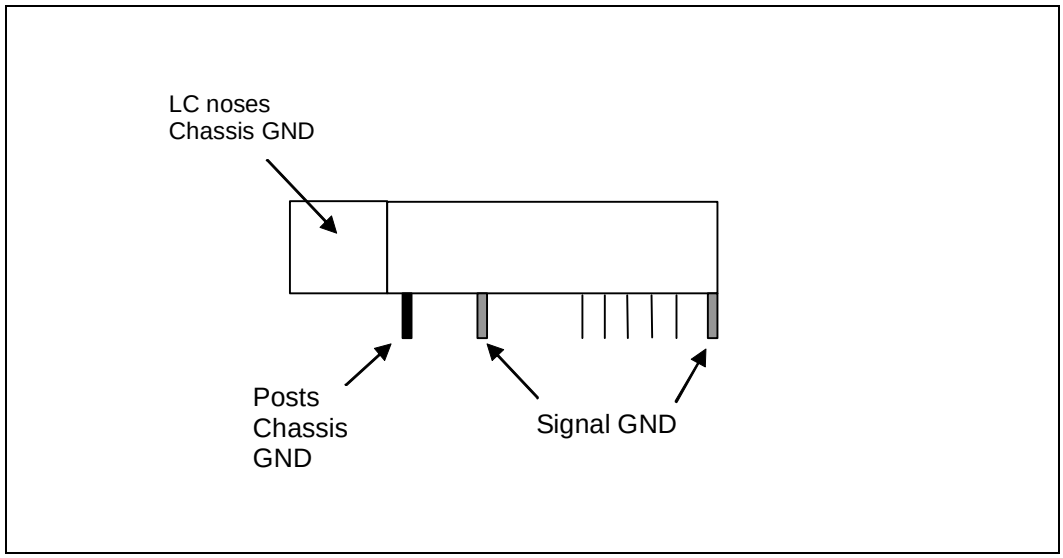
4.0 EMI and Grounding Scheme

Proper grounding is critical to ensure good EMI performance. There are two types of ground on the TXN31011 Optical Transceiver housing as follows (see Figure 4):

- Chassis ground
- Signal ground

The LC nose and the front posts form the chassis ground. This ground is used to connect to the Bezel/Chassis. In addition, there are four taps on the body of the TXN31011 Optical Transceiver, and these taps are used to connect the signal ground. Separating the signal ground from the chassis ground allows the chassis to take the static discharge. If both grounds are connected together, the static charge can move directly to the signal ground. This sometimes affects proper operation of ICs on the motherboard. The signal ground on the TXN31011 Optical Transceiver housing is connected to the ground plane of PCB inside the TXN31011 Optical Transceiver.

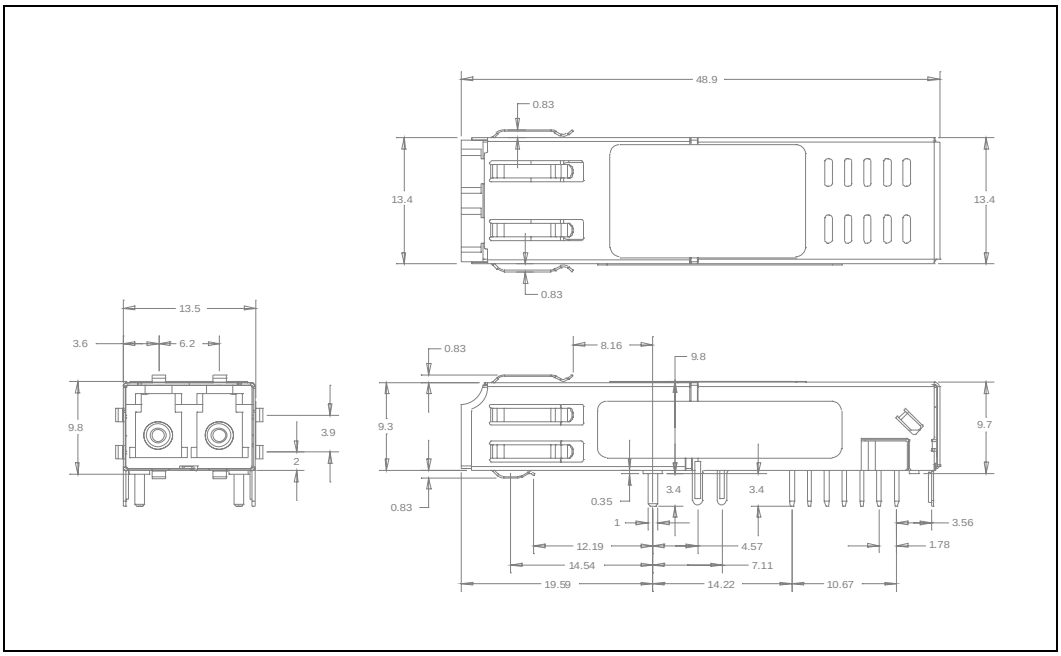
Figure 4. Proper Grounding



5.0 Mechanical Specification

Figure 5 illustrates the TXN31011 Optical Transceiver mechanical specifications. Dimensions comply with the SFF Multi-Source Agreement (MSA). All dimensions are in millimeters.

Figure 5. SFF Mechanical Specifications



6.0 Regulatory Compliance

The TXN31011 Optical Transceiver meets the relevant regulations described in Table 10.

Table 10. Regulatory Compliance

Regulatory Requirement	Applicable Standards	Performance
Electrostatic Discharge (ESD)	EN 61000-4-2 (Human Body Model)	Discharge to the pins: ± 500 V 15 kV air discharge and 8 kV contact discharge to the faceplate
Radio Frequency Immunity (RFI)	EN 61000-4-3	10 V/m from 10 kHz to 10 GHz
Electromagnetic Interference (EMI)	FCC Class B EN 55022 Class B	6 dB margin

7.0 Safety

The TXN31011 Optical Transceiver meets the fire resistance requirements of Telcordia* GR-63 Section 4.2. The device also complies with FDA 21, CFR 1040.10 and 1040.11, and IEC 825-1.

8.0 Ordering Information

When ordering, please specify the complete TXN31011 Optical Transceiver part number as defined in Table 11.

Table 11. Ordering Information

Part Number	Description
Intel® TXN310110000xxx[1]	Tri-rate 2/1 GFC, 1 GE 850 nm SFF optical transceiver
1. The last 3 characters of the part number ("xxx") are used to designate customer-specific customizations. The Intel standard part has "000" as the last three characters.	

§ §