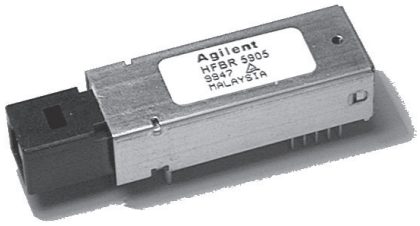
AFBR-5905Z/5905AZ

ATM Multimode Fiber Transceivers
in 2 x 5 Package Style

Data Sheet



Description

The AFBR-5905Z family of transceivers from Avago provide the system designer with products to implement a range of solutions for multimode fiber SONET OC-3 (SDH STM-1) physical layers for ATM and other services. These transceivers are all supplied in the new industry standard 2 x 5 DIP style with a MT-RJ fiber connector interface.

ATM 2 km Backbone Links

The AFBR-5905Z is a 1300 nm product with optical performance compliant with the SONET STS-3c (OC-3) Physical Layer Interface Specification. This physical layer is defined in the ATM Forum User-Network Interface (UNI) Specification Version 3.0. This document references the ANSI T1E1.2 specification for the details of the interface for 2 km multimode fiber backbone links. The ATM 100 Mb/s-125 MBd Physical Layer interface is best implemented with the AFBR- 5903Z family of FDDI Transceivers which are specified for use in this 4B/5B encoded physical layer per the FDDI PMD standard.

Transmitter Sections

The transmitter section of the AFBR-5905Z utilizes a 1300 nm InGaAsP LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V supply, into an analog LED drive current.

Features

- Multisourced 2 x 5 package style with MT-RJ receptacle
- Single +3.3 V power supply
- Wave solder and aqueous wash process compatibility
- Full compliance with ATM Forum UNI SONET OC-3 multimode fiber physical layer specification
- RoHS compliant
- Receiver output squelch function enabled

Applications

- Multimode fiber ATM backbone links
- Multimode fiber ATM wiring closet to desktop links

Ordering Information

The AFBR-5905Z 1300 nm product is available for production orders through the Avago Component Field Sales Offices and Authorized Distributors world wide.

AFBR-5905Z = 0°C to +70°C

AFBR-5905AZ = -40°C to +85°C.

Receiver Sections

The receiver section of the AFBR-5905Z utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. It is packaged in the optical subassembly portion of the receiver. This PIN/preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. The Data output is differential. The Signal Detect output is singleended. Both Data and Signal Detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3 V power supply. The receiver outputs, Data Out and Data Out Bar, are squelched at Signal Detect Deassert. That is, when the light input power decreases to a typical -38 dBm or less, the Signal Detect Deasserts, i.e. the Signal Detect output goes to a PECL low state. This forces the receiver outputs, Data Out and Data Out Bar to go to steady PECL levels High and Low respectively.

Package

The overall package concept for the Avago transceiver consists of three basic elements; the two optical subassemblies, an electrical subassembly, and the housing as illustrated in the block diagram in Figure 1.

The package outline drawing and pin out are shown in Figures 2 and 3. The details of this package outline and pin out are compliant with the multisource definition of the 2 x 5 DIP. The low profile of the Avago transceiver design complies with the maximum height allowed for the MT-RJ connector over the entire length of the package.

The optical subassemblies utilize a high-volume assembly process together with low-cost lens elements which result in a cost-effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC and various surface-mounted passive circuit elements are attached.

The receiver section includes an internal shield for the electrical and optical subassemblies to ensure high immunity to external EMI fields.

The outer housing is electrically conductive and is at reciever signal ground potential. The MT-RJ ports is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Avago design are isolated from the internal circuit of the transceiver.

The transceiver is attached to a printed circuit board with the ten signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the MT-RJ connectored fiber cables.

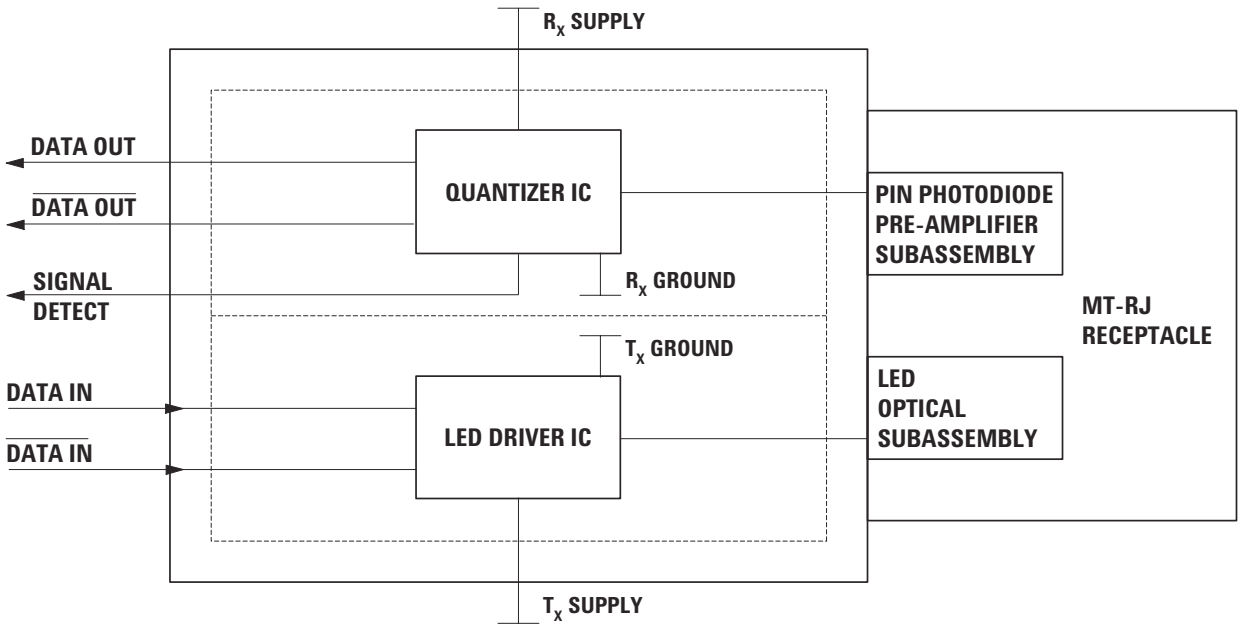
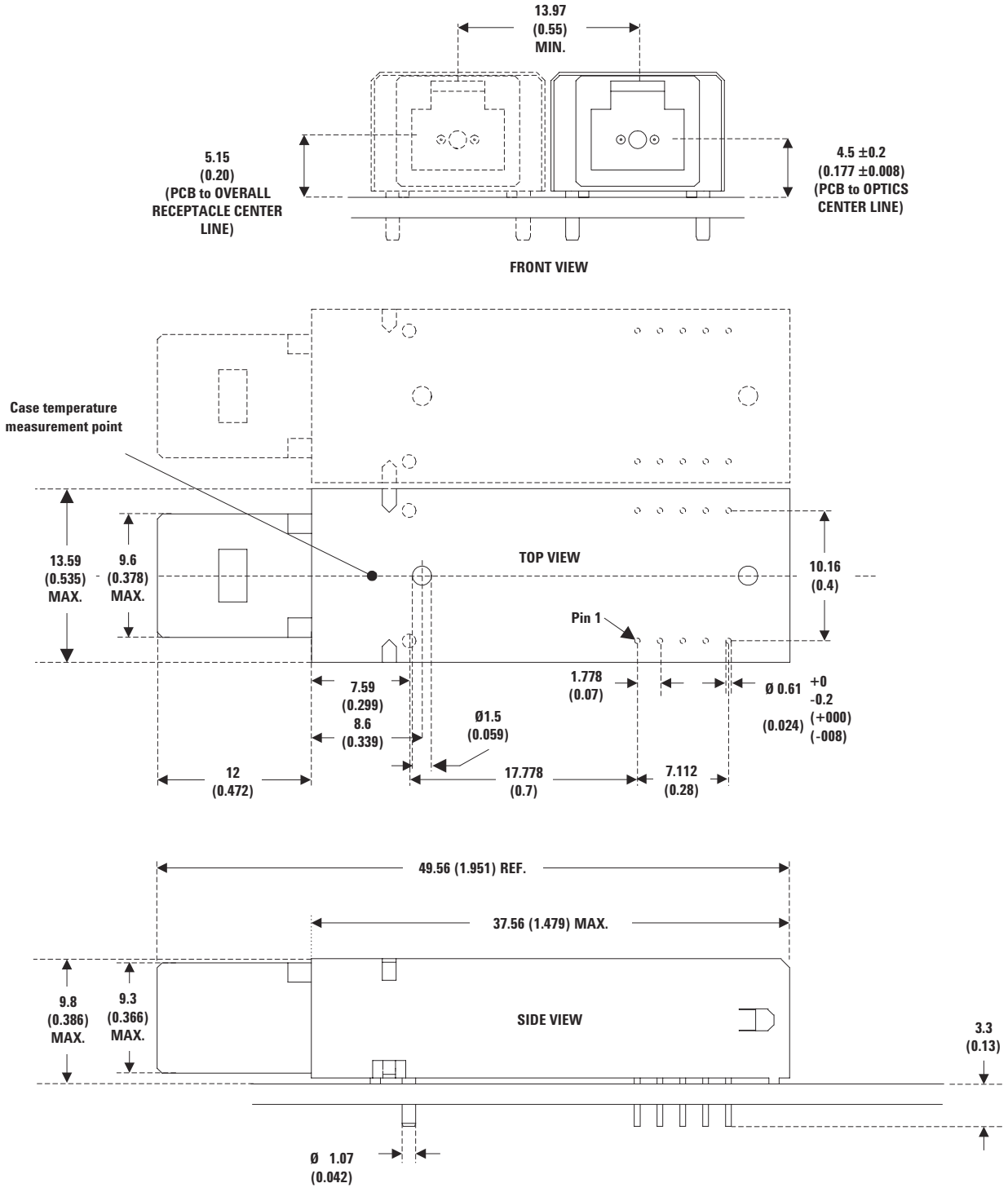


Figure 1. Block Diagram.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:

1. THIS PAGE DESCRIBES THE MAXIMUM PACKAGE OUTLINE, MOUNTING STUDS, PINS AND THEIR RELATIONSHIPS TO EACH OTHER.
2. TOLERANCED TO ACCOMMODATE ROUND OR RECTANGULAR LEADS.
3. ALL 12 PINS AND POSTS ARE TO BE TREATED AS A SINGLE PATTERN.
4. THE MT-RJ HAS A 750 µm FIBER SPACING.
5. THE MT-RJ ALIGNMENT PINS ARE IN THE MODULE.
6. FOR SM MODULES, THE FERRULE WILL BE PC POLISHED (NOT ANGLED).
7. SEE MT-RJ TRANSCEIVER PIN OUT DIAGRAM FOR DETAILS.

Figure 2. Package Outline Drawing

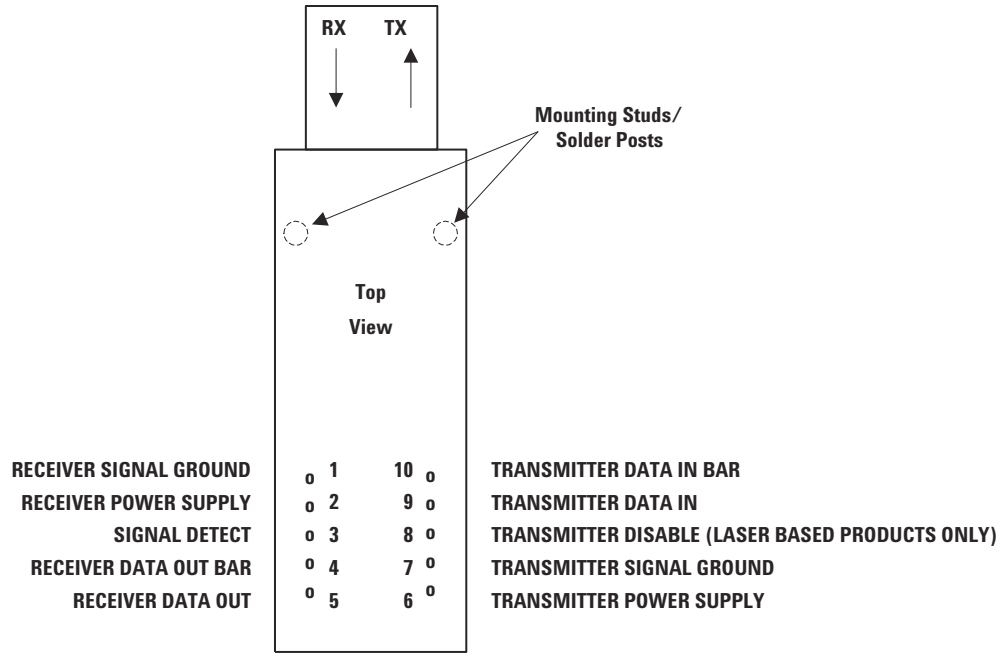


Figure 3. Pin Out Diagram.

Pin Descriptions:

Pin 1 Receiver Signal Ground VEE RX:

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply VCC RX:

Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the VCC RX pin.

Pin 3 Signal Detect SD:

Normal optical input levels to the receiver result in a logic "1" output. Low optical input levels to the receiver result in a fault condition indicated by a logic "0" output. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 4 Receiver Data Out Bar RD-:

No internal terminations are provided. See recommended circuit schematic.

Pin 5 Receiver Data Out RD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 6 Transmitter Power Supply VCC TX:

Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the VCC TX pin.

Pin 7 Transmitter Signal Ground VEE TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 Transmitter Disable TDIS:

No internal connection. Optional feature for laser based products only. For laser based products connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 9 Transmitter Data In TD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 10 Transmitter Data In Bar TD-:

No internal terminations are provided. See recommended circuit schematic.

Mounting Studs/Solder Posts

The mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Application Information

The Applications Engineering group is available to assist you with the technical understanding and design tradeoffs associated with these transceivers. You can contact them through your Avago sales representative. The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transceiver specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 µm and 50/ 125 µm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming nonfiber cable related losses. Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The 1300 nm Avago LEDs are specified to experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago sales representative for additional details.

Figure 4 was generated for the 1300 nm transceivers with a Avago fiber optic link model containing the current industry conventions for fiber cable specifications and the draft ANSI T1E1.2. These optical parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI T1E1.2 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

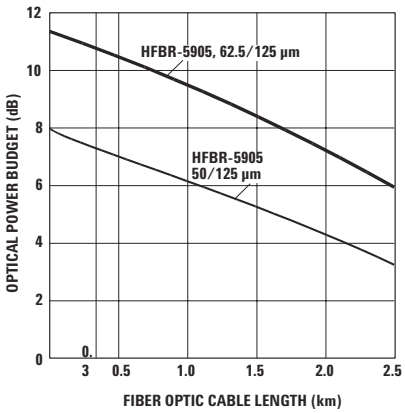


Figure 4. Typical Optical Power Budget at BOL versus Fiber Optic Cable Length.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol (Baud) rate, also called signaling rate, is the reciprocal of the symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit). When used in 155 Mb/s SONET OC-3 applications the performance of the 1300 nm transceivers, AFBR-5905 is guaranteed to the full conditions listed in product specification tables. The transceivers may be used for other applications at signaling rates different than 155 Mb/s with some variation in the link optical power budget. Figure 5 gives an indication of the typical performance of these products at different rates.

These transceivers can also be used for applications which require different Bit Error Rate (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receivers input optical power level.

Transceiver Jitter Performance

The Avago 1300 nm transceivers are designed to operate per the system jitter allocations stated in Table B1 of Annex B of the draft ANSI T1E1.2 Revision 3 standard. The Avago 1300 nm transmitters will tolerate the worst case input electrical jitter allowed in Annex B without violating the worst case output optical jitter requirements. The Avago 1300 nm receivers will tolerate the worst case input optical jitter allowed in Annex B without violating the worst case output electrical jitter allowed. The jitter specifications stated in the following 1300 nm transceiver specification tables are derived from the values in Table B1 of Annex B. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex B allocation example. In practice, the typical contribution of the Avago transceivers is well below these maximum allowed amounts.

Recommended Handling Precautions

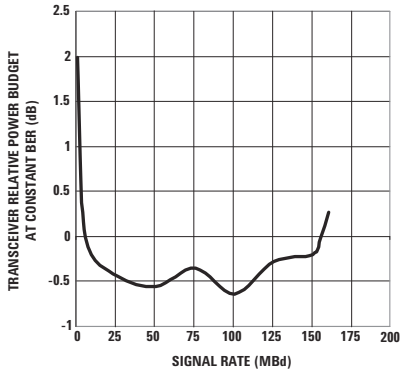
Avago recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The AFBR-5905Z series of transceivers meet MIL-STD- 883C Method 3015.4 Class 2 products. Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the MT-RJ receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping. These transceivers are compatible with either industry standard wave or hand solder processes.

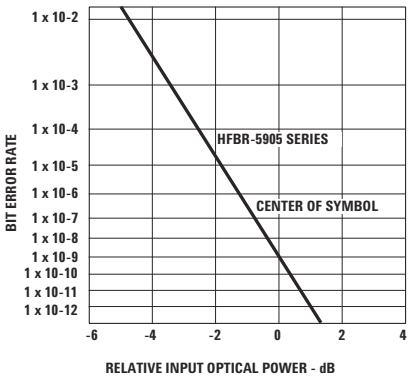
Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.



CONDITIONS:
1. PRBS 2^7-1
2. DATA SAMPLED AT CENTER OF DATA SYMBOL.
3. BER = 10^{-6}
4. T_A = +25 C
5. V_{CC} = 3.3 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 5. Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate.



CONDITIONS:
1. 125 MBd
2. PRBS 2^7-1
3. CENTER OF SYMBOL SAMPLING
4. T_A = +25C
5. V_{CC} = 3.3 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 6. Bit Error Rate vs. Relative Receiver Input Optical Power.

Board Layout - Decoupling Circuit, Ground Planes and Termination Circuits

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Figures 7 and 8 show two recommended termination schemes.

Board Layout - Hole Pattern

The Avago transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 2 x 5 package style. This drawing is reproduced in Figure 9 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

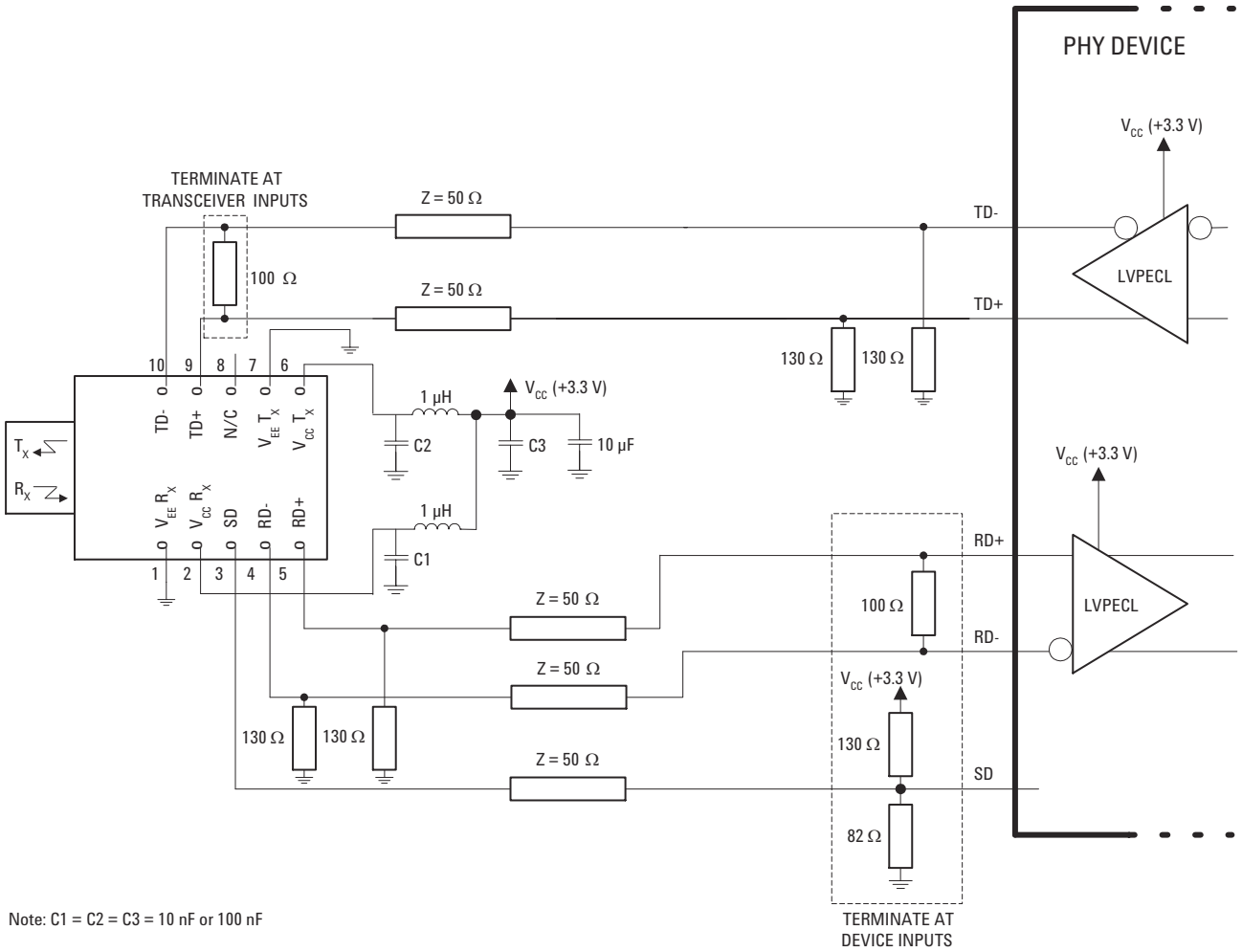


Figure 7. Recommended Decoupling and Termination Circuits

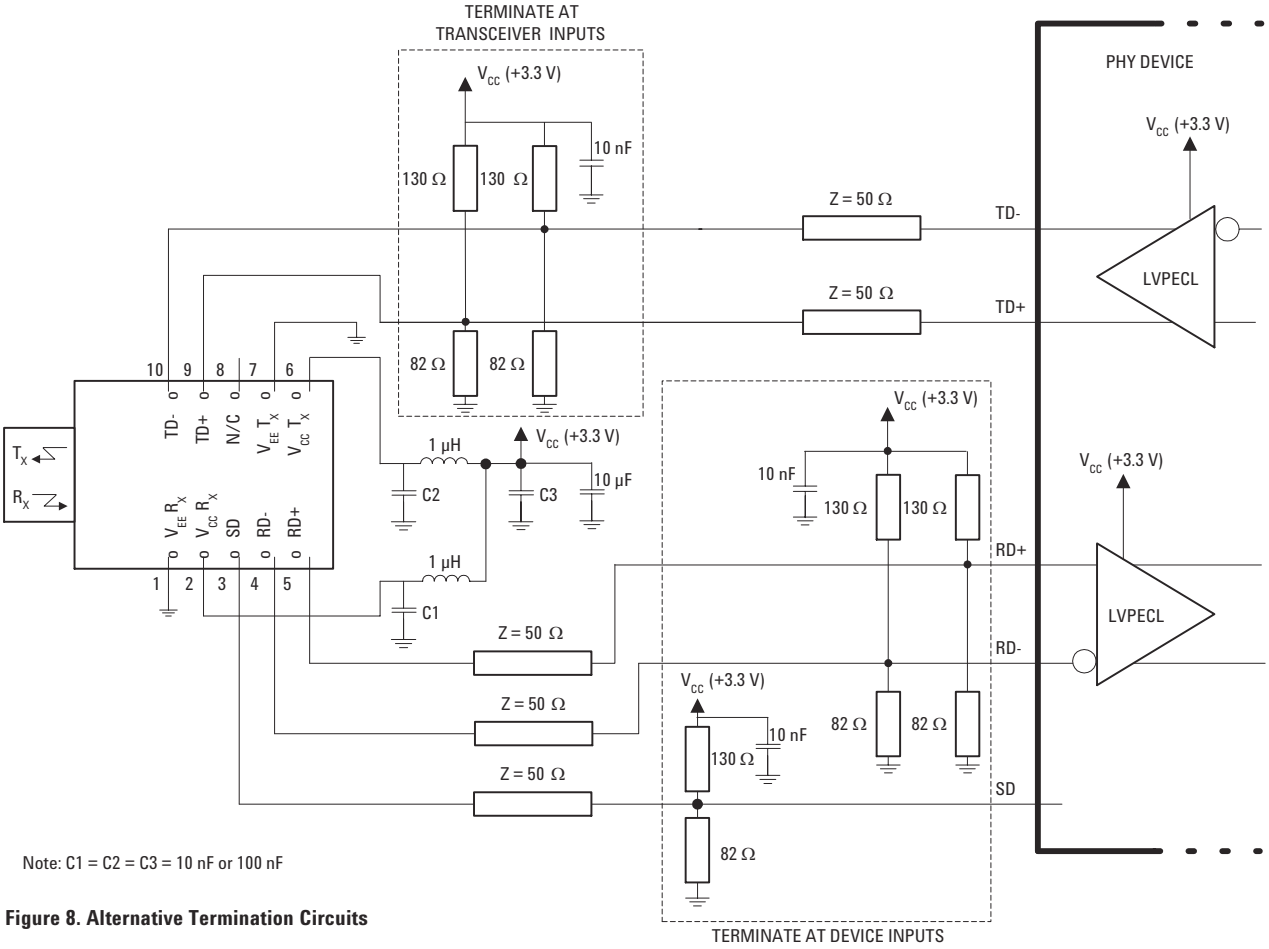
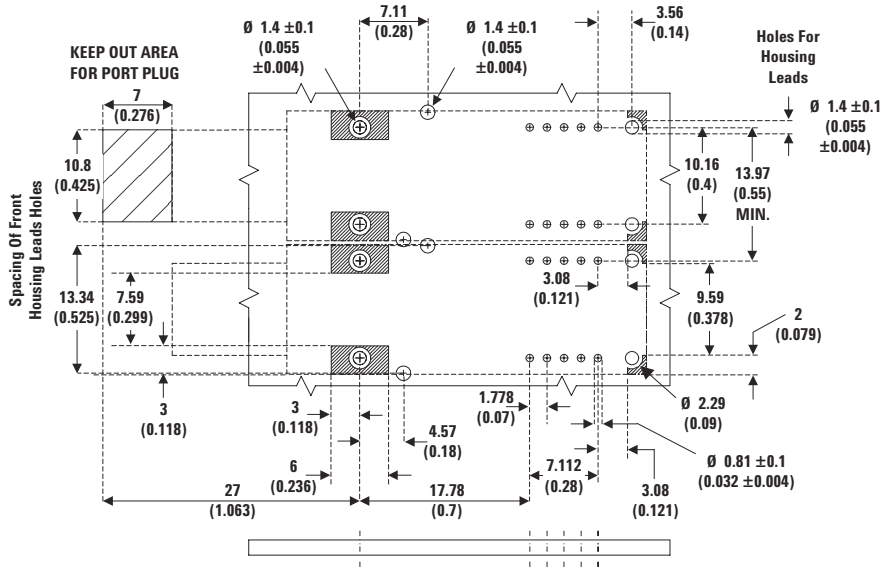


Figure 8. Alternative Termination Circuits



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:

1. **THIS FIGURE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT FOR THE MT-RJ TRANSCEIVER PLACED AT .550 SPACING.**
2. **THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.**
3. **10 PIN MODULE REQUIRES ONLY 16 PCB HOLES, INCLUDING 4 PACKAGE GROUNDING TAB HOLES CONNECTED TO SIGNAL GROUND.**
4. **THE SOLDER POSTS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY AND TO ENSURE FOOTPRINT COMPATIBILITY WITH OTHER SFF TRANSCEIVERS.**

Figure 9. Recommended Board Layout Hole Pattern

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important. The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These pre-cautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the MT-RJ connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Transceiver Reliability and Performance Qualification Data

The 2 x 5 transceivers have passed Avago reliability and performance qualification testing and are undergoing ongoing quality and reliability monitoring. Details are available from your Avago sales representative.

Applications Support Materials

Contact your local Avago Component Field Sales Office for information on how to obtain evaluation boards for the 2 x 5 transceivers.

Electromagnetic Interference (EMI)

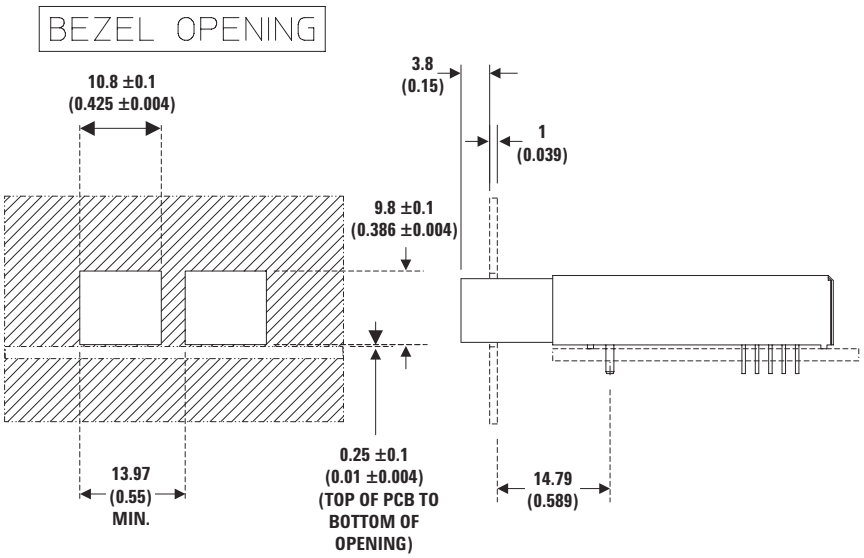
Most equipment designs utilizing this high speed transceiver from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. This product is suitable for use in designs ranging from a desktop computer with a single transceiver to a concentrator or switch product with a large number of transceivers.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

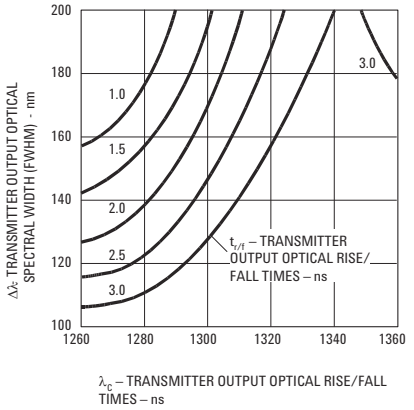
Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C	Meets Class 2 (2000 to 3999 Volts). Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the MT-RJ Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the MT-RJ Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 VCCI Class 2	Typically provide a 10 dB margin to the noted standards, however, it should be noted that final margin depends on the customer's board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	AEL Class 1 EN60825-1 (+A11)	Compliant per Agilent testing under single fault conditions. TUV Certification: LED Class 1



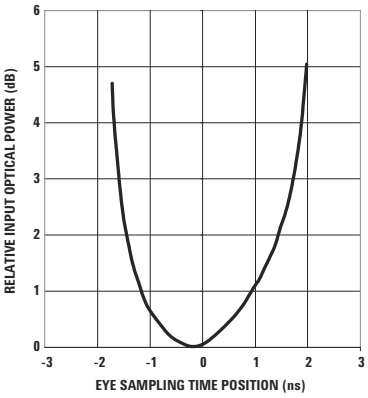
DIMENSIONS IN MILLIMETERS (INCHES)

Figure 10. Recommended Panel Mounting



HFBR-5905 TRANSMITTER TEST RESULTS OF λ_c, $\Delta\lambda$ AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 11. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



CONDITIONS:
1. T_A = +25 C
2. V_{CC} = 3.3 V dc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 15 AND 16 APPLY.

Figure 12. Relative Input Optical Power vs. Eye Sampling Time Position.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Storage Temperature	T_S	-40		+100	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		3.6	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage (p-p)	V_D			2.0	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Ambient Operating Temperature	AFBR-5905	T_A	0		+70	°C	Note A
	AFBR-5905A	T_A	-40		+85	°C	Note B
Supply Voltage		V_{CC}	3.135		3.465	V	
Data Input Voltage - Low		V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage - High		V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load		R_L		50		Ω	Note 2
Differential Input Voltage (p-p)		V_D		0.800		V	

Notes:

A. Ambient Operating Temperature corresponds to transceiver case temperature of 0 °C mininum to +85 °C maximum with necessary airflow applied. Recommanded case temperature measurement point can be found in Figure 2.

B. Ambient Operating Temperature corresponds to transceiver case temperature of -40 °C mininum to +100 °C maximum with necessary airflow applied. Recommanded case temperature measurement point can be found in Figure 2.

Transmitter Electrical Characteristics

AFBR-5905Z (T_A= 0°C to +70°C, V_{CC}=3.135V to 3.465V)
AFBR-5905AZ (T_A= -40°C to +85°C, V_{CC}= 3.135V to 3.465V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CC}		133	175	mA	Note 3
Power Dissipation	P_{DISS}		0.45	0.60	W	Note 5a
Data Input Current - Low	I_{IL}	-350	-2		µA	
Data Input Current - High	I_{IH}		18	350	µA	

Receiver Electrical Characteristics

AFBR-5905Z (T_A= 0°C to +70°C, V_{CC}= 3.135V to 3.465V)
AFBR-5905AZ(T_A= -40°C to +85°C, V_{CC}= 3.135V to 3.465V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CC}		65	120	mA	Note 4
Power Dissipation	P_{DISS}		0.225	0.415	W	Note 5b
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.83		-1.55	V	Note 6
Data Output Voltage - High	V_{OH} - V_{CC}	-1.085		-0.88	V	Note 6
Data Output Rise Time	t_r	0.35		2.2	ns	Note 7
Data Output Fall Time	t_f	0.35		2.2	ns	Note 7
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.83		-1.55	V	Note 6
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.085		-0.88	V	Note 6
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 7
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 7
Power Supply Noise Rejection	PSNR		50		mV	

Transmitter Optical Characteristics

AFBR-5905Z (T_A= 0°C to +70°C, V_{CC}= 3.135V to 3.465V)
AFBR-5905AZ (T_A= -40°C to +85°C, V_{CC}= 3.135V to 3.465V)

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Output Optical Power	BOL	P_O	-19	-15.7	-14	dBm avg	Note 8
62.5/125 µm, NA = 0.275 Fiber	EOL		-20				
Output Optical Power	BOL	P_O	-22.5	-20.3	-14	dBm avg	Note 8
50/125 µm, NA = 0.20 Fiber	EOL		-23.5				
Optical Extinction Ratio			10			dB	Note 9
Output Optical Power at Logic Low "0" State		P_O ("0")			-45	dBm avg	Note 10
Center Wavelength		λ_C	1270	1308	1380	nm	Note 23 Figure 11
Spectral Width - FWHM		$\Delta\lambda$		147		nm	Note 23
- RMS				63			Figure 11
Optical Rise Time		t_r	0.6	1.2	3.0	ns	Note 12, 23 Figure 11
Optical Fall Time		t_f	0.6	2.0	3.0	ns	Note 12, 23 Figure 11
Systematic Jitter Contributed by the Transmitter		SJ		0.21	1.2	ns p-p	Note 13
Random Jitter Contributed by the Transmitter		RJ		0.14	0.52	ns p-p	Note 14

Receiver Optical and Electrical Characteristics

AFBR-5905Z (T_A= 0°C to +70°C, V_{CC}= 3.135V to 3.465V)
AFBR-5905AZ (T_A= -40°C to +85°C, V_{CC}= 3.135V to 3.465V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min}$ (W)			-30	dBm avg	Note 15 Figure 12
Input Optical Power Minimum at Eye Center	$P_{IN\ Min}$ (C)			-31	dBm avg	Note 16 Figure 12
Input Optical Power Maximum	$P_{IN\ Max}$	-14			dBm avg	Note 15
Operating Wavelength	λ	1270		1380	nm	
Systematic Jitter Contributed by the Receiver	SJ		0.15	1.2	ns p-p	Note 17
Random Jitter Contributed by the Receiver	RJ		0.11	1.91	ns p-p	Note 18
Signal Detect - Asserted	P_A	P_D + 1.5 dB		-31	dBm avg	Note 19
Signal Detect - Deasserted	P_D	-45			dBm avg	Note 20
Signal Detect - Hysteresis	P_A - P_D	1.5			dB	
Signal Detect Assert Time (off to on)		0	2	100	µs	Note 21
Signal Detect Deassert Time (on to off)		0	5	350	µs	Note 22

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to VCC -2 V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to VCC - 2 V and an Input Optical Power level of -14 dBm average.

5a. The power dissipation of the transmitter is calculated as the sum of the products of supply voltage and current.

5b. The power dissipation of the receiver is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.

6. This value is measured with respect to VCC with the output terminated into 50 Ω connected to VCC - 2 V.
7. The output rise and fall times are measured between 20% and 80% levels with the output connected to VCC -2 V through 50 Ω. 8. These optical power values are measured with the following conditions: • The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago's 1300 nm LED products is < 1 dB, as specified in this data sheet. • Over the specified operating voltage and temperature ranges. • With 25 MBd (12.5 MHz square-wave), input signal. • At the end of one meter of noted optical fiber with cladding modes removed. The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request. Please consult with your local Avago sales representative for further details.
9. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "1" output optical power is compared to the data "0" peak output optical power and expressed in decibels. With the transmitter driven by a 25 MBd (12.5 MHz square-wave) input signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "1" level compared to the optical power at the "0" level expressed in decibels.
10. The transmitter will provide this low level of Output Optical Power when driven by a logic "0" input. This can be useful in link troubleshooting.
11. The relationship between Full Width Half Maximum and RMS values for Spectral Width is derived from the assumption of a Gaussian shaped spectrum which results in a 2.35 X RMS = FWHM relationship.
12. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 25 MBd (12.5 MHz square-wave) input signal. The ANSI T1E1.2 committee has designated the possibility of defining an eye pattern mask for the transmitter optical output as an item for further study. Avago will incorporate this requirement into the specifications for these products if it is defined. The HFBR-5905 products typically comply with the template requirements of CCITT (now ITU-T) G.957 Section 3.2.5, Figure 2 for the STM-1 rate, excluding the optical receiver filter normally associated with single mode fiber measurements which is the likely source for the ANSI T1E1.2 committee to follow in this matter.
13. Systematic Jitter contributed by the transmitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), 27 - 1 psuedorandom data pattern input signal.
14. Random Jitter contributed by the transmitter is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
15. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Rate (BER) better than or equal to 1×10^{-10}.
    - At the Beginning of Life (BOL)
    - Over the specified operating temperature and voltage ranges
    - Input is a 155.52 MBd, 223 - 1 PRBS data pattern with 72 "1"s and 72 "0"s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix I.
    - Receiver data window time-width is 1.23 ns or greater for the clock recovery circuit to operate in. The actual test data window time-width is set to simulate the effect of worst case optical input jitter based on the transmitter jitter values from the specification tables. The test window time-width is AFBR-5905Z 3.32 ns.
    - Transmitter operating with a 155.52 MBd, 77.5 MHz square-wave, input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
16. All conditions of Note 15 apply except that the measurement is made at the center of the symbol with no window time-width.
17. Systematic Jitter contributed by the receiver is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), 27 - 1 psuedorandom data pattern input signal. 18. Random Jitter contributed by the receiver is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
19. This value is measured during the transition from low to high levels of input optical power.
20. This value is measured during the transition from high to low levels of input optical power. At Signal Detect Deassert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.
21. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power.
22. Signal detect output shall be de-asserted within 350 µs after a step decrease in the Input Optical Power. At Signal Detect Deassert, the receiver outputs Data Out and Data Out Bar go to steady PECL levels High and Low respectively.
23. The AFBR-5905Z transceiver complies with the requirements for the trade-offs between center wavelength, spectral width, and rise/ fall times shown in Figure 11. This figure is derived from the FDDI PMD standard (ISO/IEC 9314-3 : 1990 and ANSI X3.166 - 1990) per the description in ANSI T1E1.2 Revision 3. The interpretation of this figure is that values of Center Wavelength and Spectral Width must lie along the appropriate Optical Rise/ Fall Time curve.

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