M0220SD-202SDAR1-1G

Vacuum Fluorescent Display Module

RoHS Compliant

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⚠ Important Safety Notice

Please read this note carefully before using the product.

Warning

- The module should be disconnected from the power supply before handling.
- The power supply should be switched off before connecting or disconnecting the power or interface cables.
- The module contains electronic components that generate high voltages which may cause an electrical shock when touched.
- Do not touch the electronic components of the module with any metal objects.
- The VFD used on the module is made of glass and should be handled with care. When handling the VFD, it is recommended that cotton gloves be used.
- The module is equipped with a circuit protection fuse.
- Under no circumstances should the module be modified or repaired.
  Any unauthorized modifications or repairs will invalidate the product warranty.
- The module should be abolished as the factory waste.

CONTENTS PAGE

1. FEATURE

This vacuum fluorescent display (VFD) module consists of a 20 character by 2 line5×8 dot matrix display, DC-DC/AC converter, and controller/driver circuitry.

The module can be configured for a Motorola M68-type parallel interface, an Intel I80-type parallel interface, or a synchronous serial interface.

A character generator ROM with 240 5×8 characters is provided along with RAM for the user to program an additional 8 characters. The luminance level of the VFD can be varied by setting two bits in the function set instruction.

Two hundred and forty character fonts consisting of a alphabets, numerals and other symbols can be displayed.

This module has a dual-port RAM that allows data and instructions to be the module continuously. Thus, the busy flag is always 0 and the host never has to read the busy flag bit to determine if the module is busy.

Due to this feature, the execution times for each instruction are not specified.

2 SPECIFICATIONS

2-1. GENERAL SPECIFICATIONS

Table-1

Item	Value	
Number of characters	20 characters× 2 lines	
Character configuration	5×8 dot matrix	
Character Height	5.34 mm	
Character Width	2.35 mm	
Character Pitch	3.60 mm	
Line Pitch	6.16 mm	
Dot Size	0.39 × 0.58 mm	
Dot Pitch	0.49 × 0.68 mm	
Peak Wavelength of Illumination	Green (λp=505nm) x=0.235, y=0.405	
Luminance	Minimum 350 cd/m^2, 102 fL	Typical 500 cd/m^2, 146 fL

2-2. ENVIRONMENTAL SPECIFICATIONS

Table-2

Item	Symbol	Min.	Max.	Unit	Comment
Operating Temperature	Topr	-40	+85	°C	
Storage Temperature	Tstg	-50	+95	°C	
Operating Humidity	Hopr	20	85	%RH	Without condensation
Storage Humidity	Hstg	20	90	%RH	Without condensation
Vibration	–	–	4	G	Total amplitude: 1.5mm Freq: 10-55 Hz sine wave Sweep time: 1 min./cycle Duration: 2hrs./axis (X,Y,Z)
Shock	–	–	40	G	Duration: 11ms Wave form: half sine wave 3 times/axis (X,Y,Z,-X,-Y,-Z)

2-3. ABSOLUTE MAXIMUM SPECIFICATIONS

Table-3

Item	Symbol	Min.	Max.	Unit
Supply Voltage	*Vcc*	-0.3	6.5	V
Input signal Voltage	V_{IN}	-0.3	*Vcc*+0.3	V

2-4. DC ELECTRICAL SPECIFICATIONS

Table-4

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	*Vcc*	4.5	5.0	5.5	V
Supply Current	*Icc*	–	140	190	mA
Power Consumption	–	–	0.7	1.045	W
High - Level Input Voltage(see Note)	V_{IH}	0.7**Vcc*	–	*Vcc*	V
Low - Level Input Voltage	V_{IL}	0	–	0.2* *Vcc*	V
High - Level Output Voltage (I_{OH} = -0.1mA)	V_{OH}	*Vcc*-0.5	–	–	V
Low - Level Output Voltage (I_{OL} = 0.1mA)	V_{OL}	–	–	0.5	V
Input Current (see Note)	I_I	-500	–	1.0	μA

Note: A 10K ohm pull-up resistor is provided on each input line.

2-5. AC ELECTRICAL SPECIFICATIONS

2-5-1. MOTOROLA M68-TYPE PARALLEL INTERFACE TIMING

(See Fig. 1 and 2)

Table-5

Item	Symbol	Min.	Max.	Unit
RS, R/W Setup Time	t_{AS}	20	–	ns
RS, R/W Hold Time	t_{AH}	10	–	ns
Input Signal rise Time	t_r	–	15	ns
Input Signal Fall Time	t_f	–	15	ns
Enable Pulse Width High	PW_{EH}	230	–	ns
Enable Pulse Width Low	PW_{EL}	230	–	ns
Write Data Setup Time	t_{DS}	80	–	ns
Write Data Hold Time	t_{DH}	10	–	ns
Enable Cycle Time	t_{CYCLE}	500	–	ns
Read Data Delay Time	t_{DD}	–	160	ns
Read Data Hold Time	t_{DHR}	5	–	ns

Note: All timing is specified using 20% and 80% of *Vcc* as the reference points.

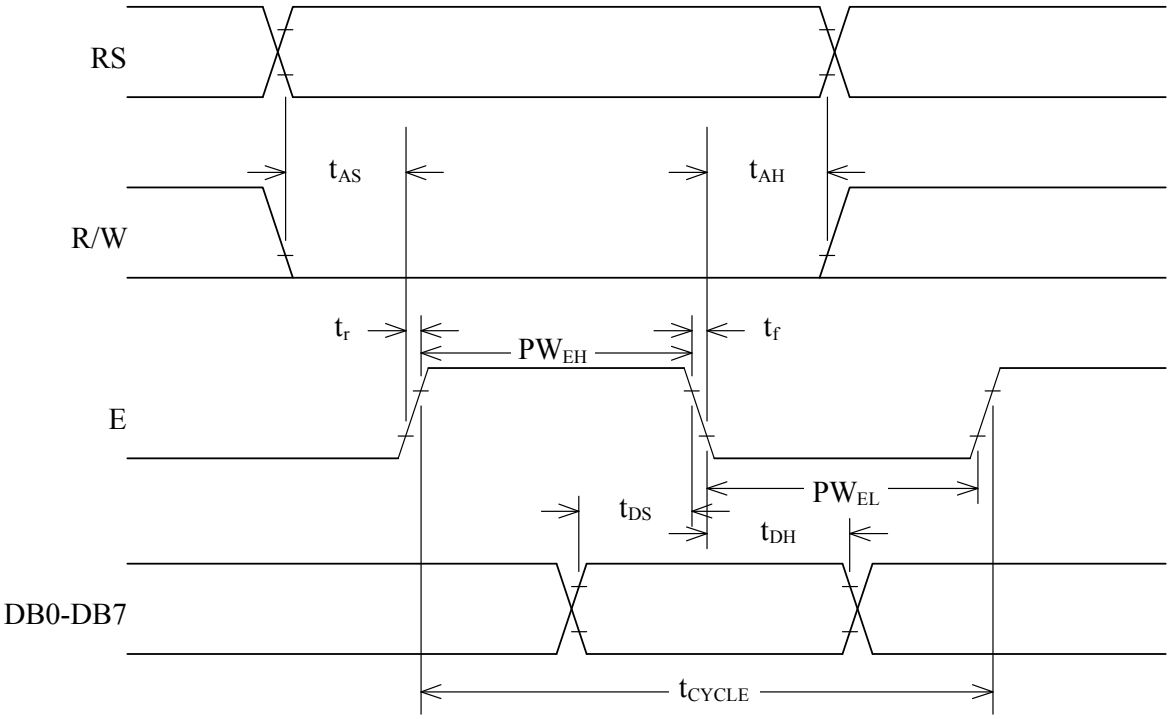


Fig. 1. Motorola M68-Type Parallel Interface Write Cycle Timing

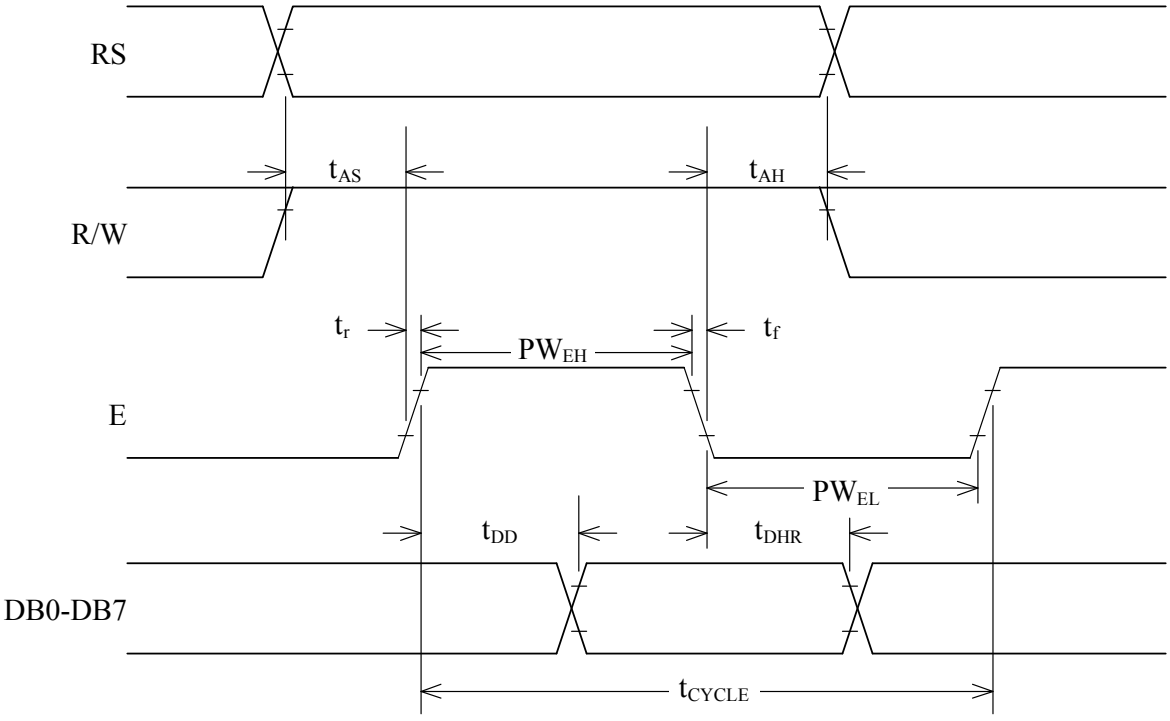


Fig. 2. Motorola M68-Type Parallel Interface Read Cycle Timing

2-5-2. INTEL I80-TYPE PARALLEL INTERFACE TIMING
(See Fig. 3 and 4)

Table-6

Item	Symbol	Min.	Max.	Unit
RS Setup Time	t_{RSS}	10	–	ns
RS Hold Time	t_{RSH}	10	–	ns
Input Signal Fall Time	t_f	–	15	ns
Input Signal Rise Time	t_r	–	15	ns
WR/ Pulse Width Low	t_{WRL}	30	–	ns
WR/ Pulse Width High	t_{WRH}	100	–	ns
Write Data Setup Time	t_{DSi}	30	–	ns
Write Data Hold Time	t_{DHi}	10	–	ns
WR/ Cycle Time	t_{CYCWR}	166	–	ns
RD/Cycle Time	t_{CYCRD}	166	–	ns
RD/ Pulse Width Low	t_{RDL}	70	–	ns
RD/ Pulse Width High	t_{RDH}	70	–	ns
Read Data Delay Time	t_{DDi}	–	70	ns
Read Data Hold Time	t_{DHRi}	5	50	ns

Note: All timing is specified using 20% and 80% of *Vcc* as the reference points.

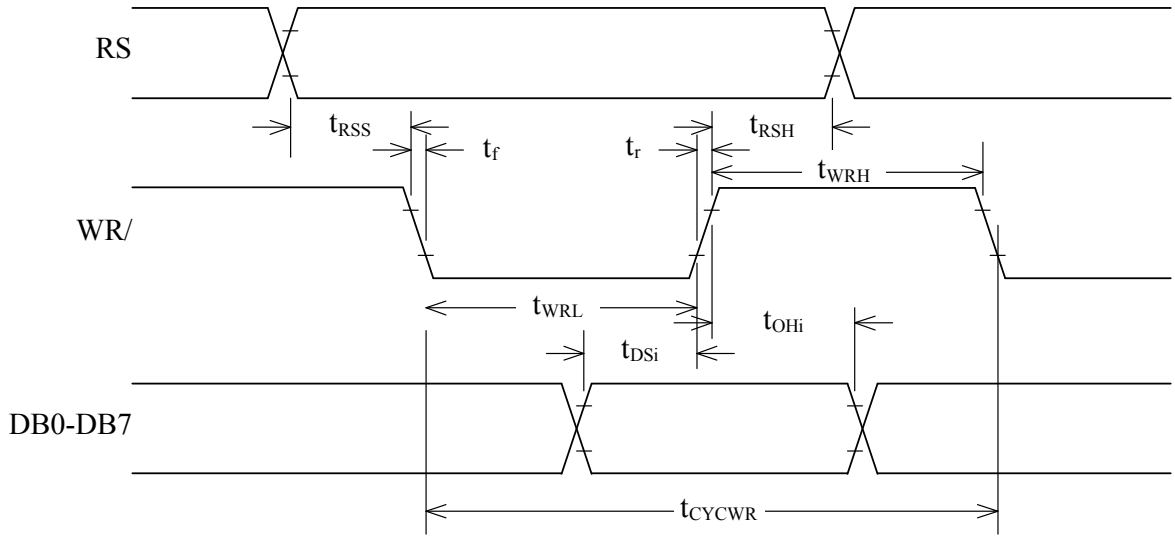


Fig. 3. Intel I80-Type Parallel Interface Write Cycle Timing

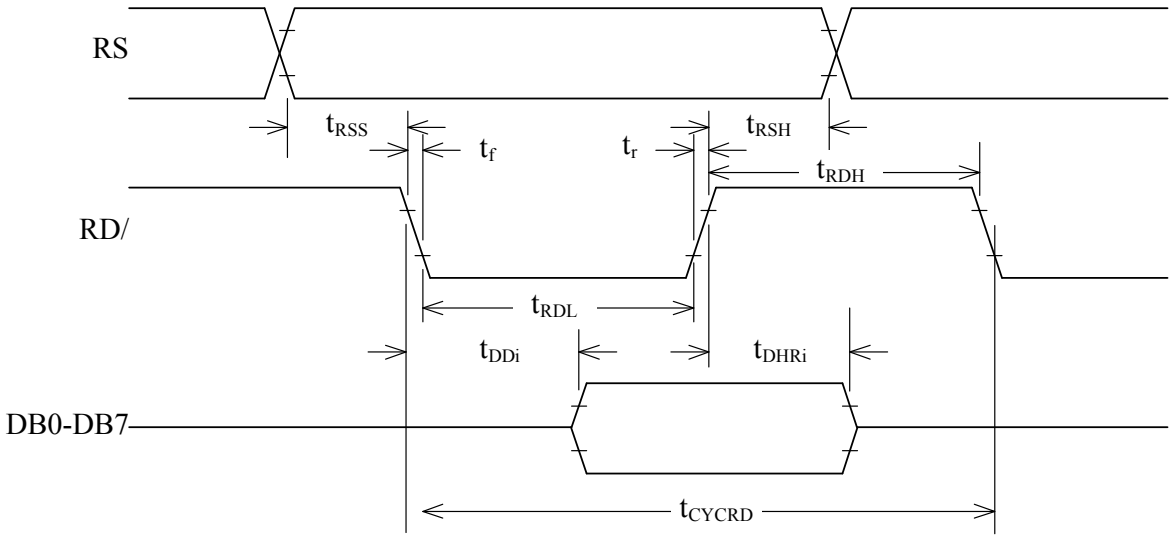


Fig. 4. Intel I80-Type Parallel Interface Read Cycle Timing

2-5-3. SYNCHRONOUS SERIAL INTERFACE TIMING
(See Fig. 5, 6, 10, and 11)

Table-7

Item	Symbol	Min.	Max.	Unit
STB Setup Time	t_{STBS}	100	–	ns
STB Hold Time	t_{STBH}	500	–	ns
Input Signal Fall Time	t_f	–	15	ns
Input Signal Rise Time	t_r	–	15	ns
STB Pulse Width High	t_{WSTB}	500	–	ns
SCK Pulse Width High	t_{SCKH}	200	–	ns
SCK Pulse Width Low	t_{SCKL}	200	–	ns
SI Data Setup Time	t_{DSs}	100	–	ns
SI Data Hold Time	t_{DHs}	100	–	ns
SCK Cycle Time	t_{CYCSCK}	500	–	ns
SCK Wait Time Between Bytes	t_{WAIT}	1	–	us
SO Data Delay Time	t_{DDs}	–	150	ns
SO Data Hold Time	t_{DHRs}	5	–	ns

Note: All timing is specified using 20% and 80% of *Vcc* as the reference points.

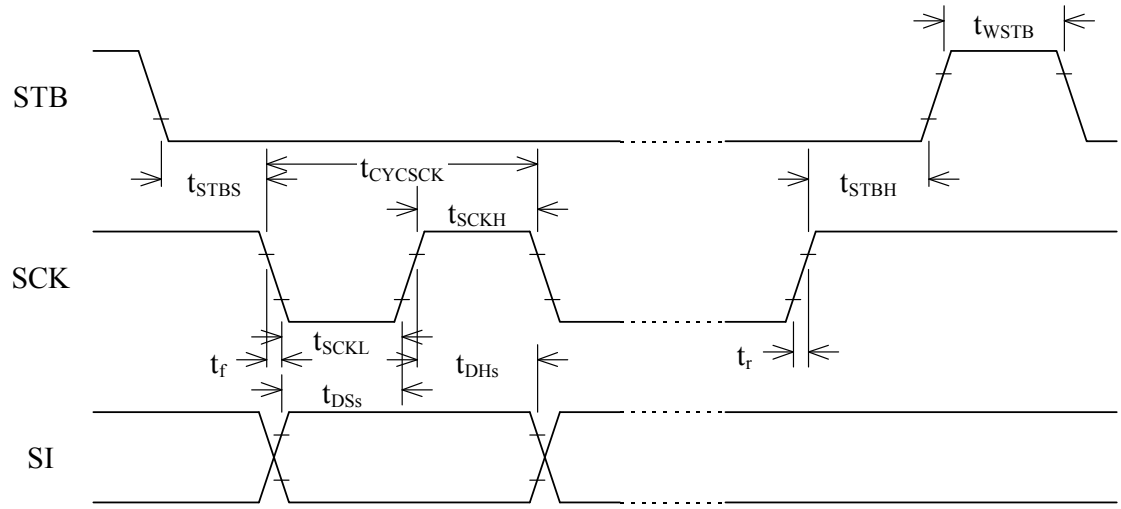


Fig. 5. Synchronous Serial Interface Write Cycle Timing

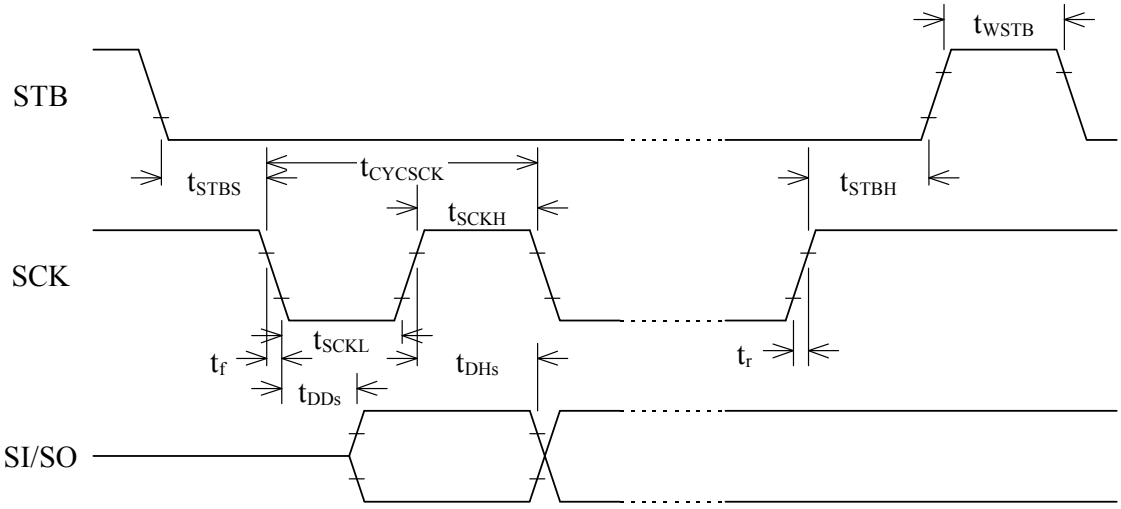


Fig. 6. Synchronous Serial Interface Read Cycle Timing

2-5-4. RESET TIMING
(See Fig. 7)

Table-8

Item	Symbol	Min.	Max.	Unit
Delay Time After Reset	t_{BSTD}	100	–	us
*V*cc Off Time	t_{OFF}	1	–	ms
RST/ Pulse Width Low	t_{RSTL}	500	–	ns

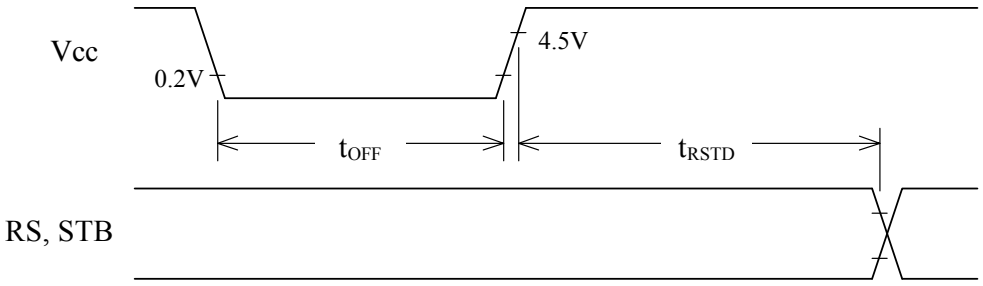


Fig. 7. Power-Up Internal Reset Timing

3. MODE OF OPERATION

The following modes of operation are selectable via jumpers (see section 6. jumper Settings).

3-1. PARALLEL INTERFACE MODES

In the parallel interface mode, 8-bit instructions and data are sent between the host and the module using either 4-bit nibbles or 8-bit bytes. Nibbles are transmitted high nibble first on DB4-DB7 (DB0-DB3 are ignored) whereas bytes are transmitted on DB0-DB7. The Register Select (RS) control signal is used to identify DB0-DB7 as an instruction (low) or data (high).

3-1-1. MOTOROLA M68-TYPE MODE

This mode uses the Read/Write (R/W) and Enable (E) control signals to transfer information.

Instructions/data are written to the module on the falling edge of E when R/W is low and are read from the module after the rising edge of E when R/W is high.

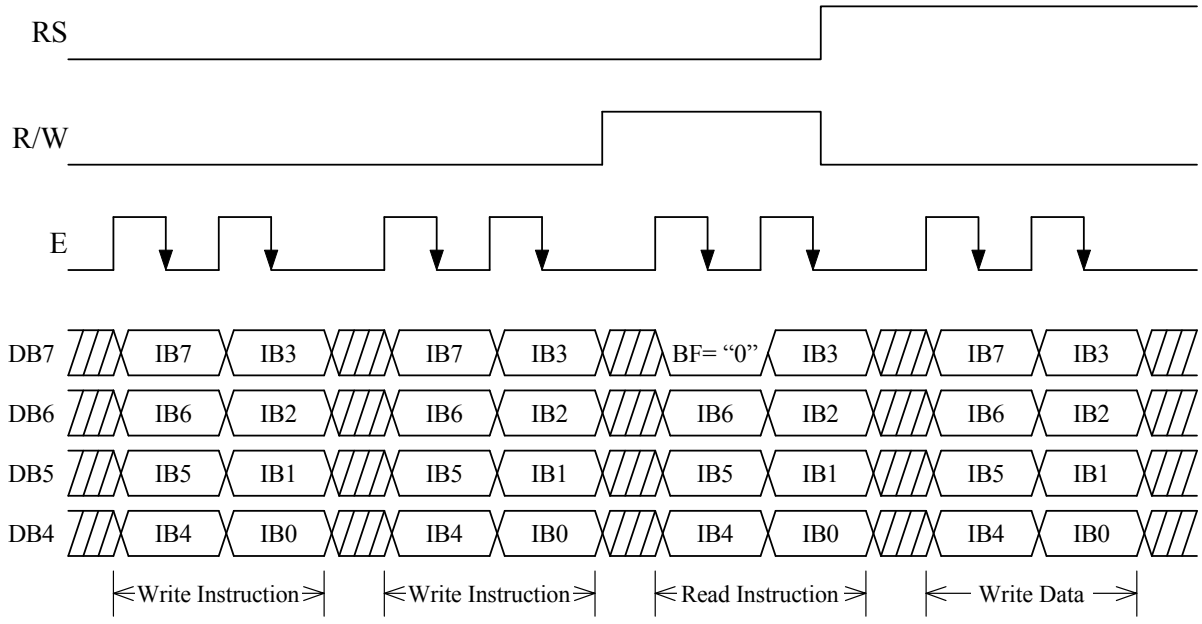


Fig. 8. Typical 4-Bit Interface Sequence Using M68-Type Mode

3-1-2. INTEL I80-TYPE MODE

This mode uses the Read (RD/) and Write (WR/) control signals to transfer information. Instructions/data are written to the module on the rising edge of WR/ and are read from the module after the falling edge of RD/.

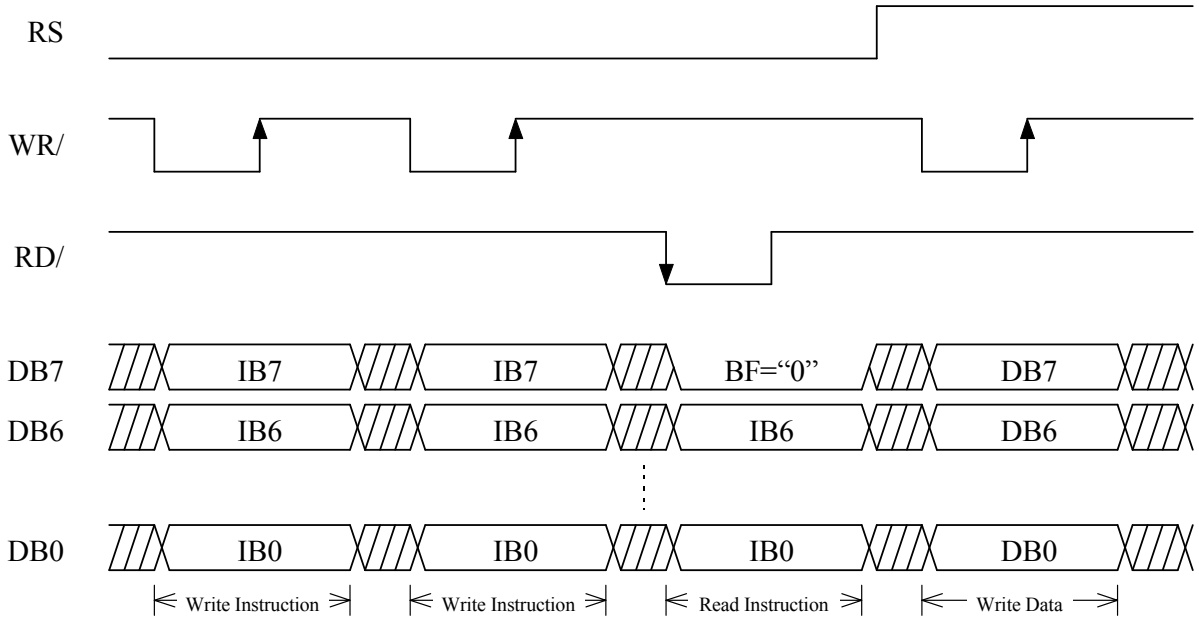


Fig. 9. Typical 8-Bit Parallel Interface Sequence Using I80-Type Mode

3-2. SYNCHRONOUS SERIAL INTERFACE MODE

In the synchronous serial interface mode, instructions and data are sent between the host and the module using 8-bit bytes. Two bytes are required per read/write cycle and are transmitted MSB first. The start byte contains 5 high bits, the Read/Write (R/W) control bit, the Register Select (RS) control bit, and a low bit. The following byte contains the instruction/data bits. The R/W bit determines whether the cycle is a read (high) or a write (low) cycle. The RS bit is used to identify the second byte as an instruction (low) or data (high).

This mode uses the Strobe (STB) control signal, Serial Clock (SCK) input, and Serial I/O (SI/SO) line to transfer information. In a write cycle, bits are clocked into the module on the rising edge of SCK. In a read cycle, bits in the start byte are clocked into the module on the rising edge of SCK. After the minimum wait time, each bit in the instruction/data byte can be read from the module after each falling edge of SCK. Each read/write cycle begins on the falling edge of STB and ends on the rising edge. To be a valid read/write cycle, the STB must go high at the end of the cycle.

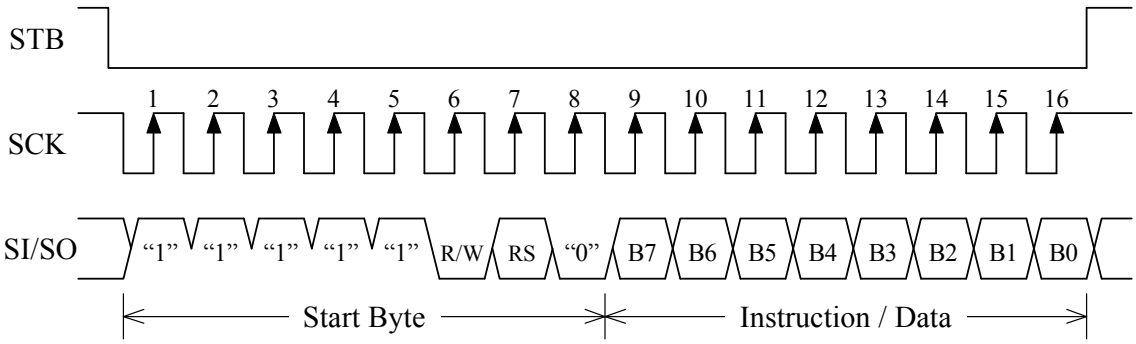


Fig. 10. Typical Synchronous Serial Interface Write Cycle

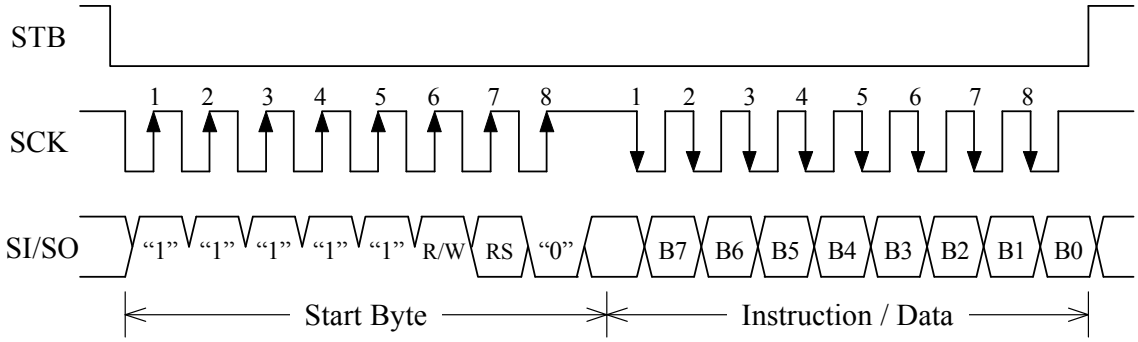


Fig. 11. Typical Synchronous Serial Interface Read Cycle

3-3. RESET MODE

The module is reset automatically at power-up by internal R-C circuit. However, an external reset mode can also be selected when using one of the parallel interface modes (this option is not available when using the synchronous serial interface mode) which allows the module to be reset by setting the Reset (RST/) input low.

4. FUNCTIONAL DESCRIPTION

4-1. ADDRESS COUNTER (AC)

The AC stores the address of the data being written to and from DDRAM or CGRAM. The AC increments by 1 (overflows from 27H to 40H and from 67H to 00H) or decrements by 1 (underflows from 40H to 27H and from 00H to 67H) after each DDRAM access. The AC increments by 1 (overflows from 3FH to 00H) or decrements by 1 (underflows from 00H to 3FH) after each CGRAM access. When addressing DDRAM, the value in the AC also represents the cursor position.

4-2. DISPLAY DATA RAM (DDRAM)

The DDRAM stores the character code of each character being displayed on the VFD. Valid DDRAM addresses are 00H to 27H and 40H to 67H. DDRAM not being used for display characters can be used as general purpose RAM. The tables below show the relationship between the DDRAM address and the character position on the VFD before and after a display shift (with the number of display lines set to 2).

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

Relationship after a display shift to the left:

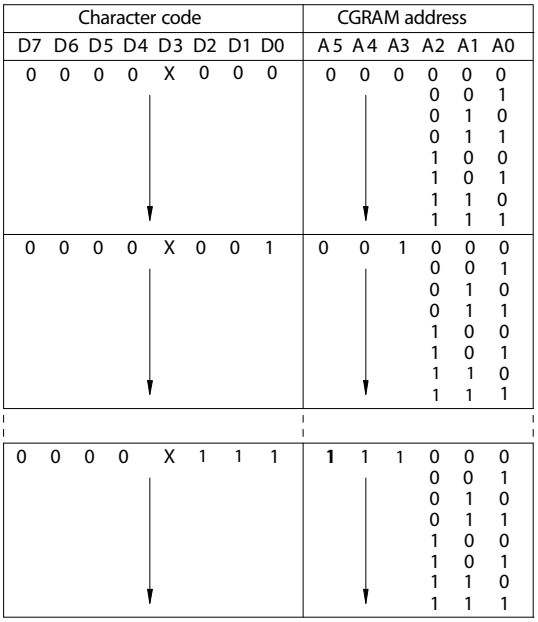
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52

4-3-1 CHARACTER GENERATOR RAM (CGRAM)

The CGRAM stores the pixel information (1 = pixel on, 0 = pixel off) for the eight user-definable 5x8 characters. Valid CGRAM addresses are 00H to 3FH. CGRAM not being used to define characters can be used as general purpose RAM (lower 5 bits only). Character codes 00H to 07H (or 08H to 0FH) are assigned to the user-definable characters (see section 5.0 Character Font Tables). The table below shows the relationship between the character codes, CGRAM addresses, and CGRAM data for each user-definable character.



x = don't care

4-3-2 INSTRUCTIONS

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear display	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	x
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	x	x
Function set	0	0	0	0	1	DL	N	x	BR1	BR0
CGRAM address set	0	0	0	1	CGRAM address					
DDRAM address set	0	0	1	DDRAM address						
Address counter read	0	1	BF=0	AC contents						
DDRAM or CGRAM write	1	0	Write data							
DDRAM or CGRAM read	1	1	Read data							

x = don't care

4-4-1. CLEAR DISPLAY

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction clears the display (without affecting the contents of CGRAM) by performing the following.

1) Fills all DDRAM locations with character code 20H (character code for a space).
2) Sets the AC to DDRAM address 00H (i.e. sets cursor position to 00H).
3) Returns the display to the non-shifted position.
4) Sets the I/D bit to 1.

4-4-2. CURSOR HOME

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	×

×=don't care

This instruction returns the cursor to the home position (without affecting the contents of DDRAM or CGRAM) by performing the following.

1) Sets the AC to DDRAM address 00H (i.e. sets cursor position to 00H).
2) Returns the display to the non-shifted position.

4-4-3. ENTRY MODE SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

This instruction selects whether the AC (cursor position) increments or decrements after each DDRAM or CGRAM access and determines the direction the information on the display shifts after each DDRAM write. The instruction also enables or disables display shifts after each DDRAM write (information on the display does not shift after a DDRAM read or CGRAM access). DDRAM, CGRAM, and AC contents are not affected by this instruction.

I/D = 0 : The AC decrements after each DDRAM or CGRAM access. If S=1, the information on the display shifts to the right by one character position after each DDRAM write.
I/D = 1 : The AC increments after each DDRAM or CGRAM access. If S=1, the information on the display shifts to the left by one character position after each DDRAM write.

S = 0 : The display shift function is disabled.
S = 1 : The display shift function is enabled.

4-4-4. DISPLAY ON/OFF CONTROL

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

This instruction selects whether the display and cursor are on or off and selects whether or not the character at the current cursor position blinks. DDRAM, CGRAM, and AC contents are not affected by this instruction.

D = 0 : The display is off (display blank).
D = 1 : The display is on (contents of DDRAM displayed).

C = 0 : The cursor is off.
C = 1 : The cursor is on (8^{th} row of pixels).

B = 0 : The blinking character function is disabled.
B = 1 : The blinking character function is enabled (a character with all pixels on will alternate with the character displayed at the current cursor position at about a 1Hz rate with a 50% duty cycle).

4-4-5. CURSOR/DISPLAY SHIFT

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	×	×

×=don't care

This instruction increments or decrements the AC (cursor position) and shifts the information on the display one character position to the left or right without accessing DDRAM or CGRAM.
DDRAM and CGRAM contents are not affected by this instruction. If the AC was addressing CGRAM prior to this instruction, the AC will be addressing DDRAM after this instruction.
However, if the AC was addressing DDRAM prior this instruction, the AC will still be addressing DDRAM after this instruction.

Table-10

S/C	R/L	AC Contents (cursor position)	Information on the display
0	0	Decrements by one	No change
0	1	Increments by one	No change
1	0	Decrements by one	Shifts on character position to the left
1	1	Increments by one	Shifts on character position to the right

4-4-6. FUNCTION SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	×	BR1	BR0

×=don't care

This instruction sets the width of the data bus for the parallel interface modes, the number of display lines, and the luminance level (brightness) of the VFD. DDRAM, CGRAM, and AC contents are not affected by this instruction.

DL = 0 : Sets the data bus width for the parallel interface modes to 4-bit (DB7-DB4).
DL = 1 : Sets the data bus width for the parallel interface modes to 8-bit (DB7-DB0).

N = 0 : Sets the number of display lines to 1 (this setting is not recommended).
N = 1 : Sets the number of display lines to 2

BR1, BR0 = 0,0: Sets the luminance level to 100%.
0,1: Sets the luminance level to 75%.
1,0: Sets the luminance level to 50%.
1,1: Sets the luminance level to 25%.

4-4-7. CGRAM ADDRESS SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	CG RAM Address					

This instruction places the 6-bit CGRAM address specified by DB5-DB0 into the AC (cursor position). Subsequent data writes (reads) will be to (from) CGRAM. DDRAM and CGRAM contents are not affected by this instruction.

4-4-8. DDRAM ADDRESS SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	DD RAM Address						

This instruction places the 7-bit DDRAM address specified by DB6-DB0 into the AC (cursor position). Subsequent data writes (reads) will be to (from) DDRAM. DDRAM and CGRAM contents are not affected by this instruction.

4-4-9. ADDRESS COUNTER READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF=0	AC Contents						

This instruction reads the current 7-bit address from the AC on DB6-DB0 and the busy flag (BF) bit (always 0) on DB7. DDRAM, CGRAM, and AC contents are not affected by this instruction. Because the BF is always 0, the host never has to read the BF bit to determine if the module is busy before sending data or instructions. Therefore, data and instructions can be sent to the module continuously according to the E, WR/, and SCK cycle times specified in section 2.5 AC Timing Specifications. Due to this feature, the execution times for each instruction are not specified.

4-4-10. DDRAM OR CGRAM WRITE

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

This instruction writes the 8-bit data byte on DB7-DB0 into the DDRAM or CGRAM location addressed by the AC. The most recent DDRAM or CGRAM Address Set instruction determines whether the write is to DDRAM or CGRAM. This instruction also increments or decrements the AC and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction.

4-4-11. DDRAM OR CGRAM READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

This instruction reads the 8-bit data byte from the DDRAM or CGRAM location addressed by the AC on DB7-DB0. The most recent DDRAM or CGRAM Address Set instruction determines whether the read is from DDRAM or CGRAM. This instruction also increments or decrements the AC and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction. Before sending this instruction, a DDRAM or CGRAM Address Set instruction should be executed to set the AC to the desired DDRAM or CGRAM address to be read.

4-5. RESET CONDITIONS

After a power-up reset, the module initializes to the following conditions:

1) All DDRAM locations are set to 20H (character code for a space).
2) The AC is set to DDRAM address 00H (i.e. sets cursor position to 00H).
3) The relationship between DDRAM addresses and character positions on the VFD is set to the non-shifted position.
4) Entry Mode Set instruction bits:
   - I/D = 1: The AC increments after each DDRAM or CGRAM access. If S=1, the information on the display shifts to the left by one character position after each DDRAM write.
   - S = 0: The display shift function is disabled.
5) Display On/Off Control instruction bits:
   - D = 0: The display is off (display blank).
   - C = 0: The cursor is off.
   - B = 0: The blinking character function is disabled.
6) Function Set instruction bits:
   - DL = 1: Sets the data bus width for the parallel interface modes to 8-bit (DB7-DB0).
   - N = 1: Number of display lines set to 2.
   - BR1,BR0=0,0: Sets the luminance level to 100%.

5. CONNECTOR INTERFACE

Table-11

Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)	Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)
1	GND	GND	GND	2	Vcc	Vcc	Vcc
5	NC	WR/	R/W	6	SCK	RD/	E
7	NC	DB0	DB0	8	NC	DB1	DB1
9	NC	DB2	DB2	10	NC	DB3	DB3
11	NC	DB4	DB4	12	NC	DB5	DB5
13	NC	DB6	DB6	14	NC	DB7	DB7

NC = No Connection

6. JUMPER SETTING

Table-12

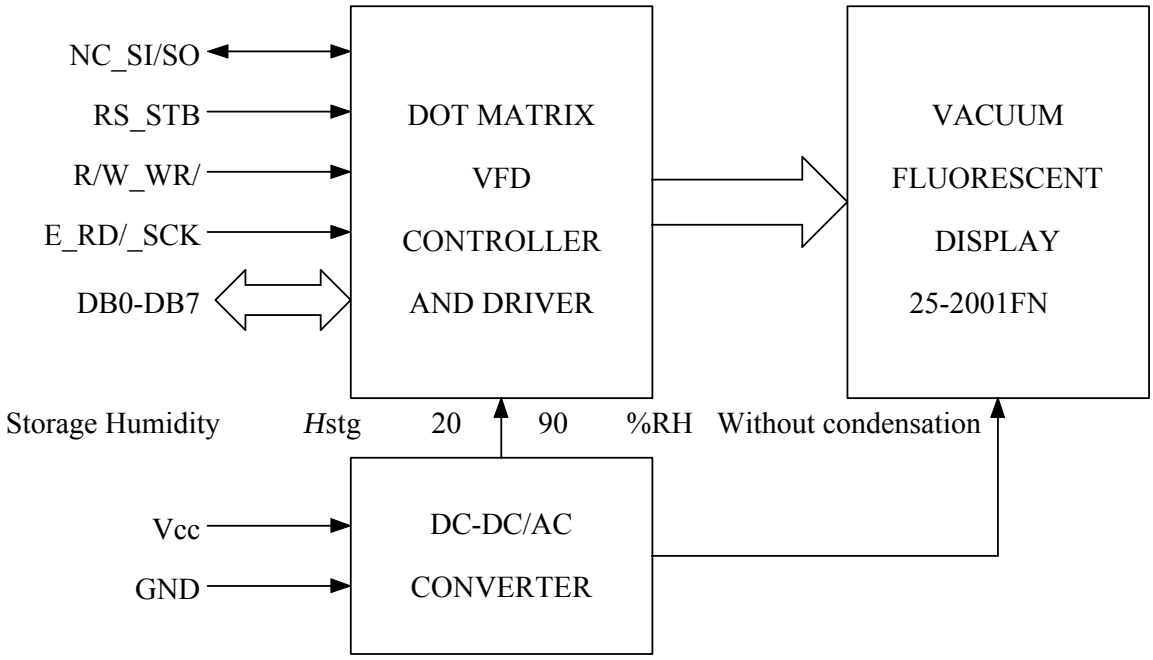
Mode	J3	J4	J5	J6	J7
Parallel (Motorola)	open	shorted	open	shorted	open
Parallel (Intel)	open	shorted	open	open	shorted
Serial	shorted	open	shorted	shorted	open

Note : JP3~JP7 must be set as shown above for either one of the parallel modes or for the serial mode.
When the module is shipped , the parallel (Motorola) mode is set.

M0220SD-202SDAR1-1G using Parallel Transfer mode. Jumper setting:J6 shorted and J2,J3,J5,J7 open.

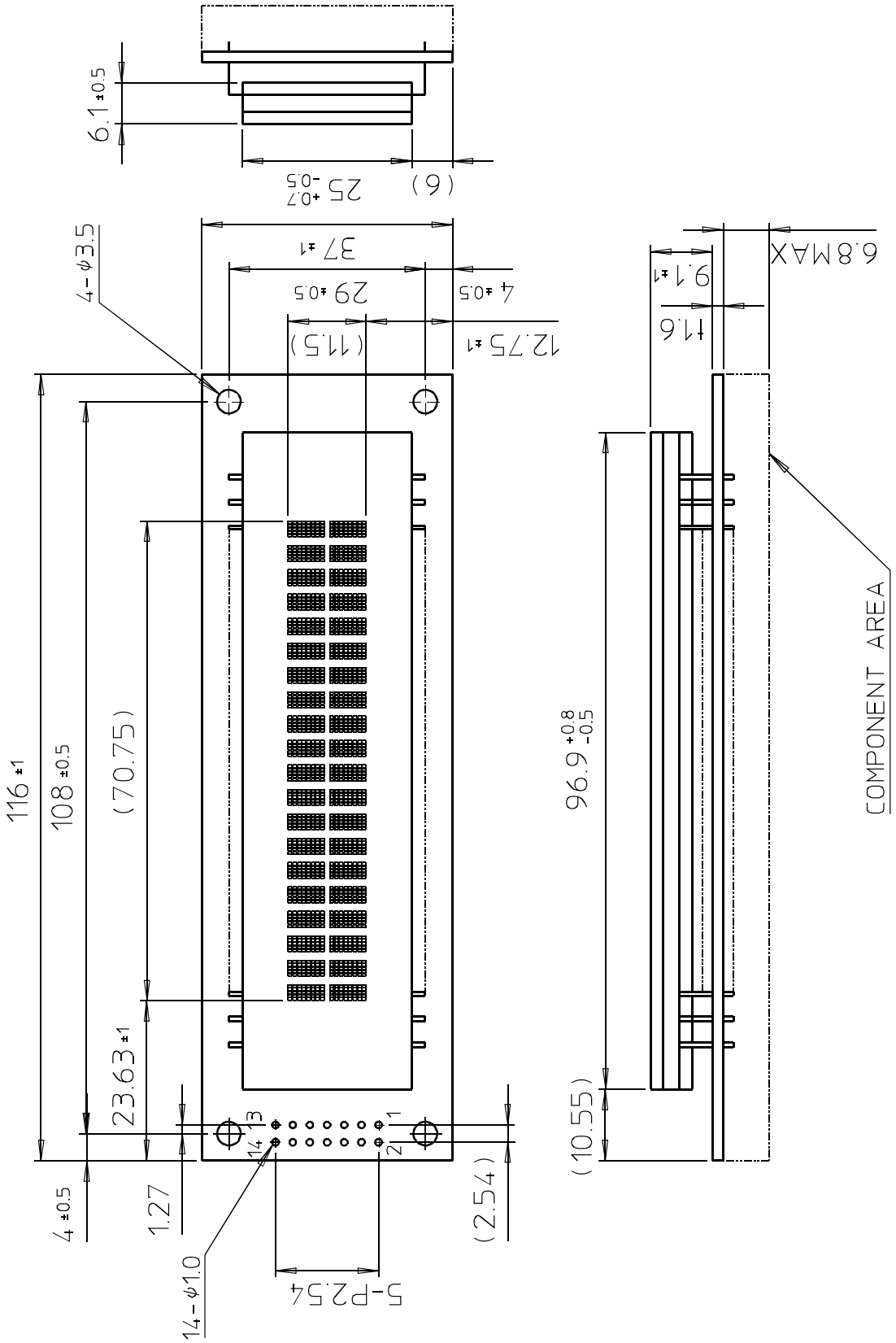
M0220SD-202SDAR1-S using Serial Data Transfer mode. Jumper setting:J3,J5,J6 shorted and J2,J7 open
Pin NO. 1,2,3,4,5 using a linker connected.

7. CIRCUIT BLOCK DIAGRAM



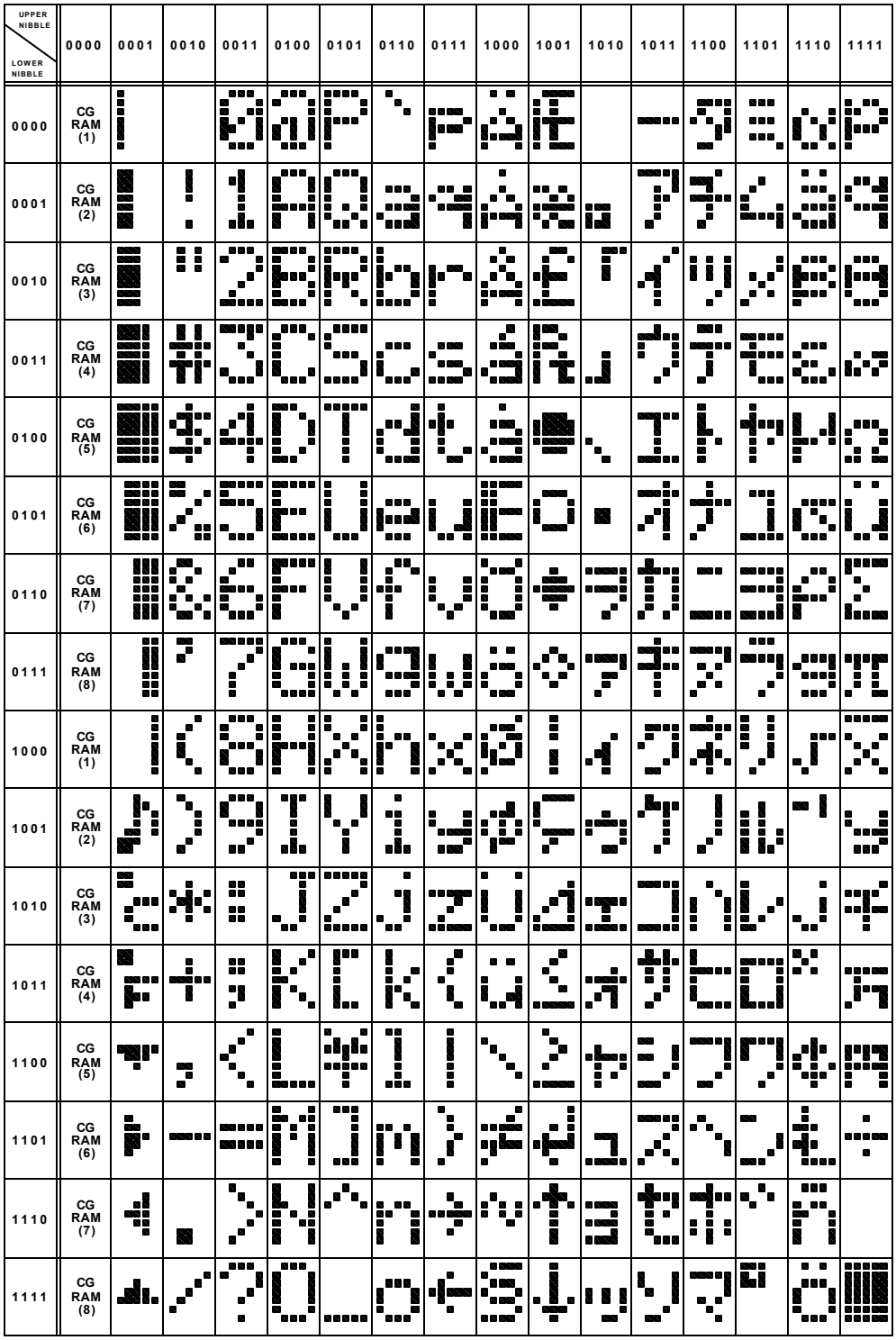
MECHANICAL DRAWING

FIGURE-1



CHARACTER FONT TABLES

FIGUER-2



8. WARRANTY

This display module is guaranteed for 1 year after a shipment from Newhaven Display.

9. OPERATING RECOMMENDATION

9-1. Since VFDs are made of glass material.
Avoid applying excessive shock or vibration beyond the specification for the module.
Careful handing is essential.

9-2. Applying lower voltage than the specified may cause non activation for selected pixels.
Conversely, higher voltage may cause may non-selected pixel to be activated.
If such a phenomenon is observed, check the voltage level of the power supply.

9-3. Avoid plugging or unplugging the interface connection with the power on.

9-4. If the start up time of the supply voltage is slow, the controller may not be reset.
The supply voltage must be risen up to the specified voltage level within 30msec.

9-5. Avoid using the module where excessive noise interference is expected. Noise affects the interface signal and causes improper operation.
Keep the length of the interface cable less than 50cm (When the longer cable is required, please contact Newhaven Display engineering).

9-6. When power supply is turned off, the capacitor does not discharge immediately.
The high voltage applied to the VFD must not contact the controller IC.
(The shorting of the mounted components within 30 seconds after power off may cause damage.)

9-7. The fuse is mounted on the module as circuit protection.
If the fuse blown, the problem shall be solved first and change the fuse.

9-8. When fixed pattern is displayed for long time, you may see uneven luminance.
It is recommended to change the display patterns sometimes in order to keep best display quality.

REMARKS

This specification is subject to change without prior notice in order to improve the design and quality.
Your consultation with Newhaven Display sales office is recommended for the use of this module.