

# User's Guide

# NHD-12864EZ-FL-YBW

# LCM

(Liquid Crystal Display Graphic Module)

RoHS Compliant

NHD-	Newhaven Display
12864-	128 x 64 pixels
EZ-	Version Line
F-	Transflective
L-	Yellow/Green LED B/L
Y-	STN- Yellow/Green
B-	6:00 View
W-	Wide Temperature (-20 ~ +70c)

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For product support, contact

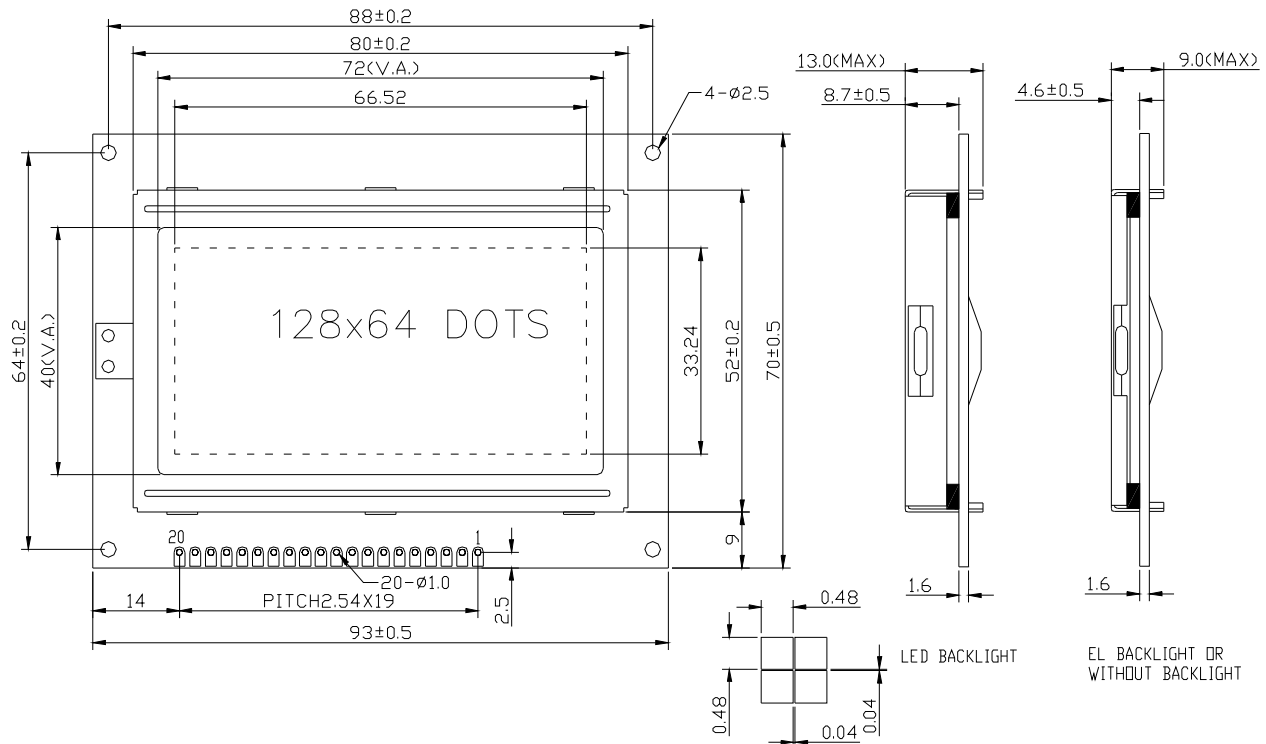
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**Elgin, IL 60124**

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February 29, 2008

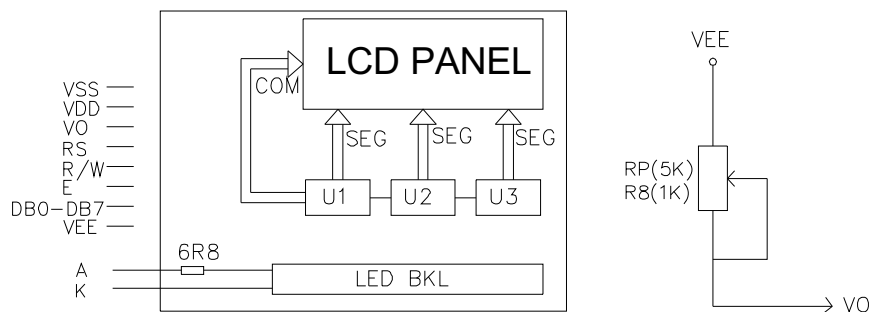
**NHD-12864EZ**
**◆ Feature**

1. 128X64 dots with 8192 chinese character fonts (16x16)
2. 128 alpha-numerical fonts (16x8)
3. 64X256 bit graphic display RAM
4. Strong display control fuctions: Vertical scroll, horizontal bit scroll, line reverse etc
5. +2.7~ +5.5V power supply
4. STN; 1/64 duty; LED BKL or EL BKL
7. 4bit, 8bit, serial interface

**◆ Mechanical diagram**

**◆ Mechanical data**

ITEM	STANDARD	UNIT
MODULE DIMENSION	93X70.0/9.0(EL)/13.0(LED)	mm
VIEWING AREA	72.0X40	mm
DOT SIZE	0.48X0.48	mm
DOT PITCH	0.52X0.52	mm

◆ **Block diagram**



◆ **Absolute Maximum Ratings**

ITEM	SYMBOL	MIN	MAX	UNIT
Power Voltage	$V_{DD}-V_{SS}$	0	5.5	V
Input Voltage	$V_I$	$V_{SS}$	$V_{DD}$	
LCD Voltage	$V_{LCD}$	4.5	7.0	
Operating temperature range	$V_{OP}$	-20	+70	°C
Storage temperature range	$T_{ST}$	-30	+80	

**DESCRIPTION OF TERMINALS**

PIN NO.	PIN NAME	INPUT/OUTPUT	EXTERNAL CONNECTION	FUNCTION
1	VSS	INPUT	POWER SUPPLY	VSS: GND
2	VDD	INPUT		VDD: +5V
3	VO	INPUT		$V_{LCD}$ ADJUSTMENT
4	RS(CS*)	INPUT	MPU	REGISTER SELECT SIGNAL “0”:INSTRUCTION REGISTER (WHEN WRITING) BUSY FLAG & ADDRESS COUNTER (WHEN READING) “1”:DATA REGISTER (WHEN WRITING & READING)
5	R/W(SID*)	INPUT	MPU	READ/WRITE SELECT SIGNAL “0” FOR WRITING , “1” FOR READING
6	E(SCLK*)	INPUT	MPU	OPERATION (DATA READ/WRITE) ENABLE SIGNAL
7 / 10	DB0-DB3	INPUT	MPU	LOW-ORDER LINES OF DATA BUS WITH 3-STATE, BI-DIRECTIONAL FUNCTION FOR USE IN DATA TRANSACTION WITH THE MPU. THESE LINES ARE NOT USED WHEN INTERFACING WITH A 4-BIT MICROPROCESSOR.
11 / 14	DB4-DB7	INPUT	MPU	HIGH-ORDER LINES OF DATA BUS WITH 3-STATE, BI-DIRECTIONAL FUNCTION FOR USE IN DATA TRANSACTIONS WITH THE MPU. DB7 MAY ALSO BE USED TO CHECK THE BUSY FLAG.
15	A	INPUT	BACKLIGHT	RESET SIGNAL
16	K	INPUT		DOUBLE VOLTAGE BOOSTER OUTPUT
17	/RST	INPUT		
18	VEE	OUTPUT		
19	A	INPUT	BACKLIGHT	
20	K	INPUT		

## ◆ Optical Characteristics

### ● FOR STN TYPE DISPLAY MODULE ( $T_A=25^{\circ}\text{C}$ , $V_{DD}=5.0\text{V}\pm 0.25\text{V}$ )

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VIEWING ANGLE	$\Theta$	$C_R \geq 4$	-25	—	—	DEG
	$\Phi$		-30	—	30	
CONTRAST RATIO	$C_R$		—	2	—	—
RESPONSE TIME(RISE)	$T_R$	—	—	120	150	mS
RESPONSE TIME(FALL)	$T_R$	—	—	120	150	mS

### ● STN TYPE DISPLAY MODULE ( $T_A=25^{\circ}\text{C}$ , $V_{DD}=5.0\text{V}$ )

ITEM	SYMBOL	CONDITI ON	MIN.	TYP.	MAX.	UNIT
VIEWING ANGLE	$\Theta$	$C_R \geq 2$	-60	—	35	DEG
	$\Phi$		-40	—	40	
CONTRAST RATIO	$C_R$		—	6	—	—
RESPONSE TIME(RISE)	$T_R$	—	—	150	250	mS
RESPONSE TIME(FALL)	$T_R$	—	—	150	250	mS

## ◆ Electrical Characteristics

### ● DC Characteristics( $T_a=25^{\circ}\text{C}$ , $V_{DD}=5.0\text{V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LCD	$V_{DD}-V_O$	$T_A=25^{\circ}\text{C}$	—	6.5	—	V
INPUT VOLTAGE	$V_{DD}$		3.0	5.0	5.5	V
SUPPLY CURRENT	$I_{DD}$	$V_{DD}=5.0\text{V}; T_A=25^{\circ}\text{C}$	—	0.5	0.7	mA
INPUT LEAKAGE CURRENT	$I_{LKG}$		—	—	1.0	$\mu\text{A}$
“H” LEVEL INPUT VOLTAGE	$V_{IH}$		3.5	—	$V_{DD}$	V
“L” LEVEL INPUT VOLTAGE	$V_{IL}$	TWICE INITIAL VALUE OR LESS	-0.3	—	0.6	V
“H” LEVEL OUTPUT VOLTAGE	$V_{OH}$	LOH= -0.25mA	4.0	—	—	V
“L” LEVEL OUTPUT VOLTAGE	$V_{OL}$	LOL=1.6mA	0	—	—	V
BACKLIGHT SUPPLY VOLTAGE	$V_F$		—	4.2	5.0	V

### ● DC Characteristics( $T_a=25^{\circ}\text{C}$ , $V_{DD}=3.0\text{V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LCD	$V_{DD}-V_O$	$T_A=25^{\circ}\text{C}$	—	4.2	—	V
INPUT VOLTAGE	$V_{DD}$		—	3.0	3.3	V
SUPPLY CURRENT	$I_{DD}$	$V_{DD}=5.0\text{V}; T_A=25^{\circ}\text{C}$	—	0.4	0.7	mA
INPUT LEAKAGE CURRENT	$I_{LKG}$		—	—	1.0	$\mu\text{A}$
“H” LEVEL INPUT VOLTAGE	$V_{IH}$		3.5	—	$V_{DD}$	V
“L” LEVEL INPUT VOLTAGE	$V_{IL}$	TWICE INITIAL VALUE OR LESS	-0.3	—	0.6	V
“H” LEVEL OUTPUT VOLTAGE	$V_{OH}$	LOH= -0.25mA	4.0	—	—	V
“L” LEVEL OUTPUT VOLTAGE	$V_{OL}$	LOL=1.6mA	—	—	—	V
BACKLIGHT SUPPLY VOLTAGE	$V_F$		—	—	—	V

● **AC Characteristics (VDD=5V,TA=25°C) Parallel mode interface**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Internal clock operation						
f <sub>osc</sub>	OSC Frequency	R=33k	-	540	-	KHZ
External Clock Operation						
t <sub>EX</sub>	External Frequency	-	-	540	-	KHZ
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	us
Write Mode (writing data from MPU to LCM)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	
T <sub>r</sub> , T <sub>f</sub>	Enable rise/fall time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address setup time	Pins: RS, RW, E	10	-	-	
T <sub>AH</sub>	Address hold time	Pins: RS, RW, E	20	-	-	
T <sub>DDR</sub>	Data delay time	Pins; DB0-DB7	40	-	-	
T <sub>H</sub>	Data hold time	Pins DB0-DB7	20	-	-	
Read mode (writing data from MPU to LCM)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	
T <sub>r</sub> , T <sub>f</sub>	Enable rise/fall time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address setup time	Pins: RS, RW, E	10	-	-	
T <sub>AH</sub>	Address hold time	Pins: RS, RW, E	20	-	-	
T <sub>DDR</sub>	Data delay time	Pins; DB0-DB7	-	-	100	
T <sub>H</sub>	Data hold time	Pins DB0-DB7	20	-	-	

● **AC Characteristics (VDD=5V,TA=25°C) Serial mode interface**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Internal clock operation						
T <sub>osc</sub>	OSC Frequency	R=33k	470	540	590	KHZ
External Clock Operation						
T <sub>EX</sub>	External Frequency	-	470	530	590	KHZ
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	us
T <sub>SCYC</sub>	Enable Cycle Time	Pin E	600	-	-	ns
T <sub>SHW</sub>	Enable Pulse Width	Pin E	200	-	-	
T <sub>SLW</sub>	Enable rise/fall time	Pin E	200	-	-	
T <sub>SDS</sub>	Address setup time	Pin: RW	40	-	-	
T <sub>SDH</sub>	Address hold time	Pin: RW	40	-	-	
T <sub>CSS</sub>	Data delay time	Pin; RS	60	-	-	
T <sub>CSH</sub>	Data hold time	Pin: RS	60	-	-	

● **AC Characteristics (VDD=3.0V,TA=25°C) Parallel mode interface**

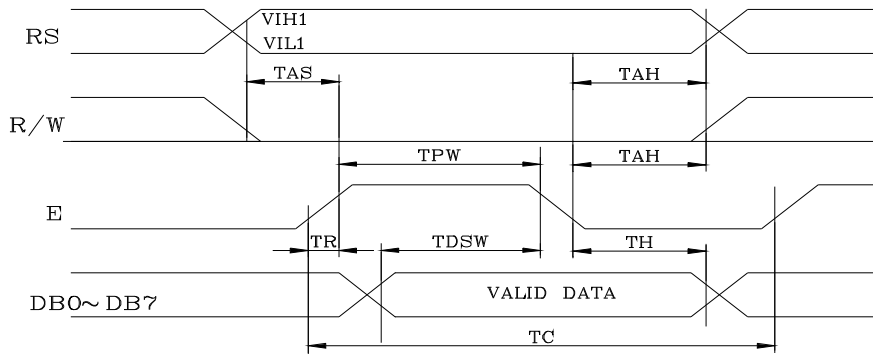
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Internal clock operation						
F <sub>osc</sub>	OSC Frequency	R=18k	-	530	-	KHZ
External Clock Operation						
T <sub>EX</sub>	External Frequency	-	-	530	-	KHZ
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	us
Write Mode (writing data from MPU to LCM)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1800	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	160	-	-	
T <sub>r</sub> , T <sub>f</sub>	Enable rise/fall time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address setup time	Pins: RS, RW, E	10	-	-	
T <sub>AH</sub>	Address hold time	Pins: RS, RW, E	20	-	-	
T <sub>DDR</sub>	Data delay time	Pins; DB0-DB7	40	-	-	
T <sub>H</sub>	Data hold time	Pins DB0-DB7	20	-	-	
Read mode (reading data form MPU to LCM)						
T <sub>C</sub>	Enable Cycle Time	Pin E	1800	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	320	-	-	
T <sub>r</sub> , T <sub>f</sub>	Enable rise/fall time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address setup time	Pins: RS, RW, E	10	-	-	
T <sub>AH</sub>	Address hold time	Pins: RS, RW, E	20	-	-	
T <sub>DDR</sub>	Data delay time	Pins; DB0-DB7	-	-	260	
T <sub>H</sub>	Data hold time	Pins DB0-DB7	20	-	-	

● **AC Characteristics (VDD=3.0V,TA=25°C) Serial mode interface**

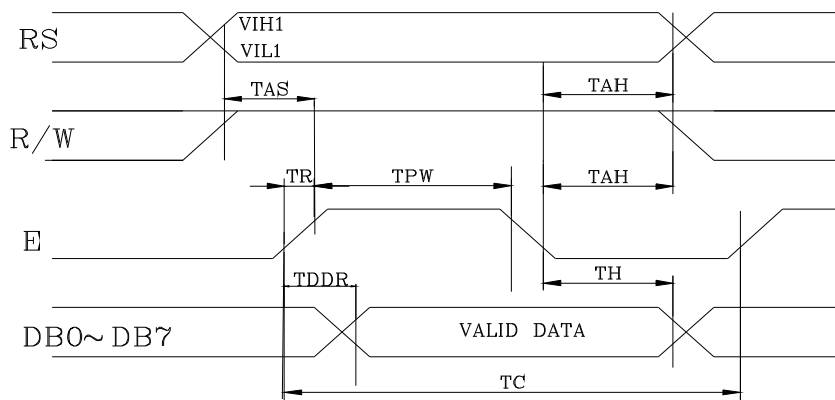
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Internal clock operation						
T <sub>osc</sub>	OSC Frequency	RF=18k	470	540	590	KHZ
External Clock Operation						
T <sub>EX</sub>	External Frequency	-	470	530	590	KHZ
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	us
T <sub>SCYC</sub>	Enable Cycle Time	Pin E	600	-	-	ns
T <sub>SHW</sub>	Enable Pulse Width	Pin E	300	-	-	
T <sub>SLW</sub>	Enable rise/fall time	Pin E	300	-	-	
T <sub>SDS</sub>	Address setup time	Pin: RW	40	-	-	
T <sub>SDH</sub>	Address hold time	Pin: RW	40	-	-	
T <sub>CSS</sub>	Data delay time	Pin; RS	60	-	-	
T <sub>CSH</sub>	Data hold time	Pin: RS	60	-	-	

◆ Timing Characteristics

● Writing data form MPU to LCM

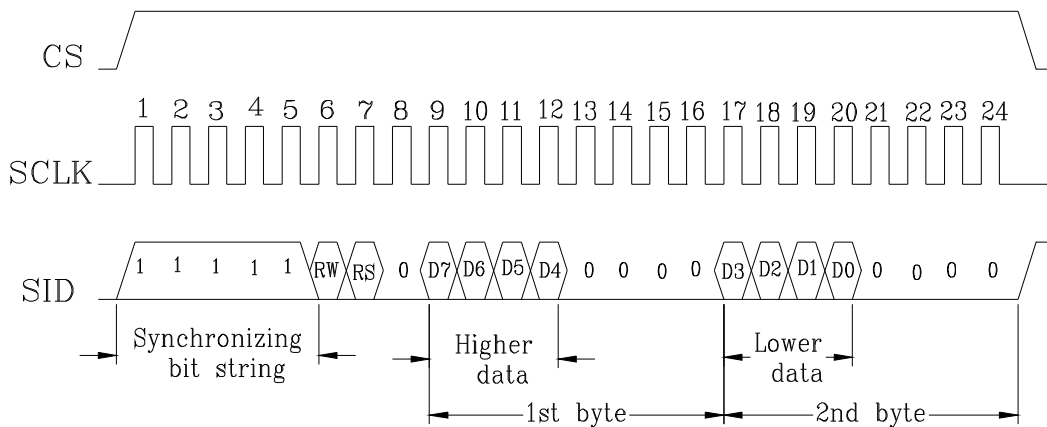


● Reading data from LCM to MPU



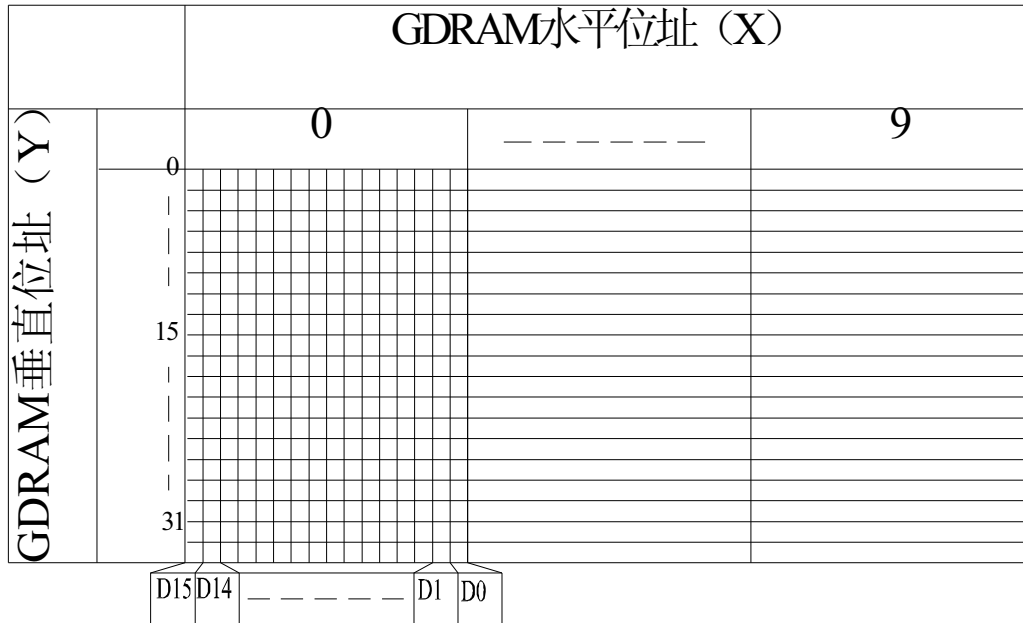
serial interface & transferring serial data

● Writing data form MPU to LCM



◆ **CGROM, CGRAM, ICON RAM, AND DDRAM, GDRAM**

● Graphic display data address map



**Table 1: 64 x 256-bit map display RAM (GDRAM) for graphic mode display**



**NHD-12864EZ**

● **Character generator ROM (CGROM)**

THE CHARACTER GENERATOR ROM GENERATES 16 X 16 DOT OR 16 X 8 DOT CHARACTER PATTERNS FROM TWO 8-BIT CHARACTER CODES. USER-DEFINED CHARACTER PATTERNS ARE ALSO AVAILABLE BY MASK-PROGRAMMED ROM.

● **Character generator RAM (CGRAM)**

IN THE CHARACTER GENERATOR RAM, THE USER CAN REWRITE CHARACTER PATTERNS BY PROGRAM. FOR 16 X 16 DOTS, FOUR CHARACTER PATTERNS CAN BE WRITTEN.

SEE TABLE 1 FOR THE RELATIONSHIP BETWEEN CGRAM ADDRESSES AND DATA AND DISPLAY PATTERNS. AREAS THEY ARE NOT USED FOR DISPLAY CAN BE USED AS GENERAL DATA RAM.

DDRAM DATA				CGRAM ADDRESS					CGRAM DATA HIGH BYTE								CGRAM DATA LOW BYTE																	
B15~B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0								
0	×	0	0	×	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0				
							0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
							0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
							0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
							0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
							0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
							0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
							1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
							1	0	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0
							1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0
							1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0
							1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0
							1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	×	0	1	×	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0				
							0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
							0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
							0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
							0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
							0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
							0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
							1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
							1	0	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0
							1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0
							1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	0
							1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0
							1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1

**Table 1: Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)**

**Notes:**

1. Character code bits 1 to 2 correspond to CGRAM address bits 4 to 5 (2 bits: 4 types).
2. CGRAM address bits 0 to 3 designate the character pattern line position. The 16th line is the cursor position and a logical OR with the cursor forms its display. Maintain the 16th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 16th line data is 1, 1 bits will light up the 16th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 15 (bit 15 being at the left).
- \*4. As shown Table, CGRAM character patterns are selected when character code bits 4 to 15 are all 0 and bit 0 and bit 3 are don't care (x).

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	X															
1	▶	◀	⚡	!!	¶	§	-	‡	↑	↓	→	←	L	↔	▼	▲
2		!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	ⓐ	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	ⓑ	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^
6	ⓓ	'	a	b	c	d	e	f	g	h	i	j	k	l	m	n
7	ⓔ	ⓕ	ⓖ	ⓗ	ⓙ	ⓚ	ⓛ	ⓜ	ⓝ	ⓞ	ⓟ	ⓠ	ⓡ	ⓢ	ⓣ	ⓤ

**Table 2: 16K-bit half-size character generator ROM (HCGROM) for a total of 128 alpha-numerical fonts(16x8 dots)**

◆ **Control and display command**

● **Basic instruction**

**Instruction Table: (RE=0: Enable basic instruction.)**

Instruction	Instruction Code											Description	Execution Time (450KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC	2.5 ms
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	2.5 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	60us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1: entire display on C=1: cursor on B=1: cursor position on	60 us
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	60 us
Function Set (Modify)	0	0	0	0	1	DL	N	0	G	X	RE	DL: interface data is 8/4 bits N=1 & RE=0: 3 Line setting N=1 & RE=1: 4 Line setting G=1: Graphic display on G=0: Graphic display off Others: 2 Line setting RE=1: Extended instruction setting. RE=0: Normal instruction setting.	60 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter	60 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter	60 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM/IRAM/GRAM)	60 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM/IRAM/GRAM)	60 us

● **Extension instruction**

**Instruction Table: (RE=1: Enable extension instruction.)**

Instruction	Instruction Code											Description	Execution Time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Standby Mode	0	0	0	0	0	0	0	0	0	0	1	Enter standby mode, only Icon areas display. Standby mode can be released by any other instructions.	60 us
Start Row Enable	0	0	0	0	0	0	0	0	0	1	SR	SR=1: Allow change start display Row. SR=0: Disable start display Row change.	60 us
Reverse Line Select	0	0	0	0	0	0	0	0	1	R1	R0	Choice one of 4 lines which data is reverse display.	60 us
Sleep mode and Set GRAM page	0	0	0	0	0	0	0	1	SL	GD	GW	SL=0: Enter sleep mode. SL=1: Wake-up from sleep mode. GD: Display graphic page 0 or 1 GW: Write data to graphic page 0 or 1. (Effective while GP=1)	60 us
Display Shift by dot	0	0	0	0	0	0	1	OA	LR	L1	L0	OA=1: One of 4 lines shift enable. OA=0: All line shift enable. LR=1: Dot by dot shift right. LR=0: Dot by dot shift left. L1, L0: Choice one of 4 lines shift.	60 us
Function Set (Modify)	0	0	0	0	0	1	CL	N	1	G	GP	CL=1: Select 16 character line CL=0: Select 8 character line N=1 & RE=1: 4 line display RE=1: Extended instruction setting. RE=0: Normal instruction setting. G=1: Graphic display on G=0: Graphic display off GP=1: Two page GRAM GP=0: One page GRAM	60 us
Set IRAM or Start Row address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 is start row SR=0: AC5~AC0 is ICON RAM address	60 us
Set Graphic RAM address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set Graphic RAM address in address counter. Execute once set the address of display row. Execute again set the address of display column. Each address of display column has data of 16 bits. Therefore write data should execute 2 times.	60 us

**Note:**

Be sure the LCM is not in the busy state (BF = 0) before sending an instruction from the MPU to the LCM. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

## ◆ Serial Interface & Transferring Serial Data

The LCM enters serial mode when the J8 is set low. A two-line clock synchronous transfer method is used. The LCM receives serial input data(SID) by synchronizing with a transfer clock(SCLK) sent from the master side.

When the MPU interfaces with several LCD MODULES, chip select pin(CS) must be used. The transfer clock(SCLK) input is activated by making chip select(CS) high. In addition, the transfer counter of the LCM can be reset and serial transfer synchronized by making chip select(CS) low. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single LCM interfaces to a single MPU, an interface can be constructed from the transfer clock(SCLK) and serial input data(SID). In this case, chip select(CS) should be fixed to high.

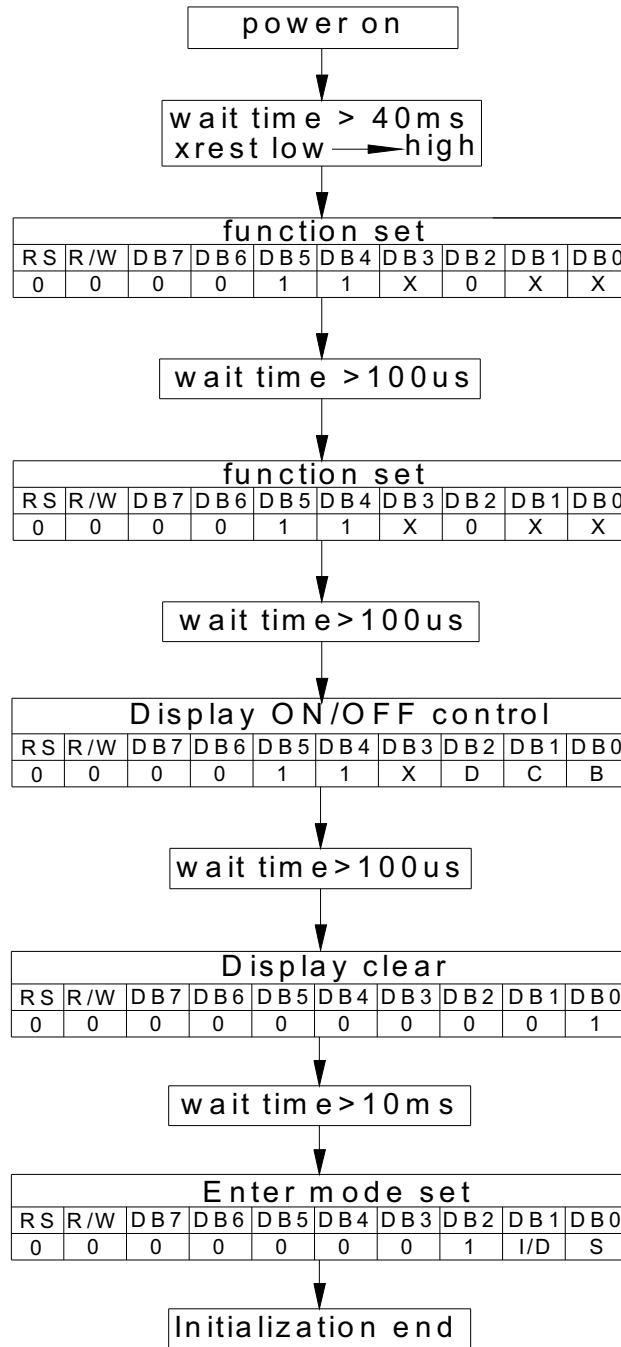
The transfer clock(SCLK) is independent of operational clock of the LCM. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock must be considered since the LCM does not have an internal transmit/receive buffer.

Following figure shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1(synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCM is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string(5 bits) specify transfer direction(RW bit) and register select(RS bit). Be sure to transfer 0 in the 8 th bit.

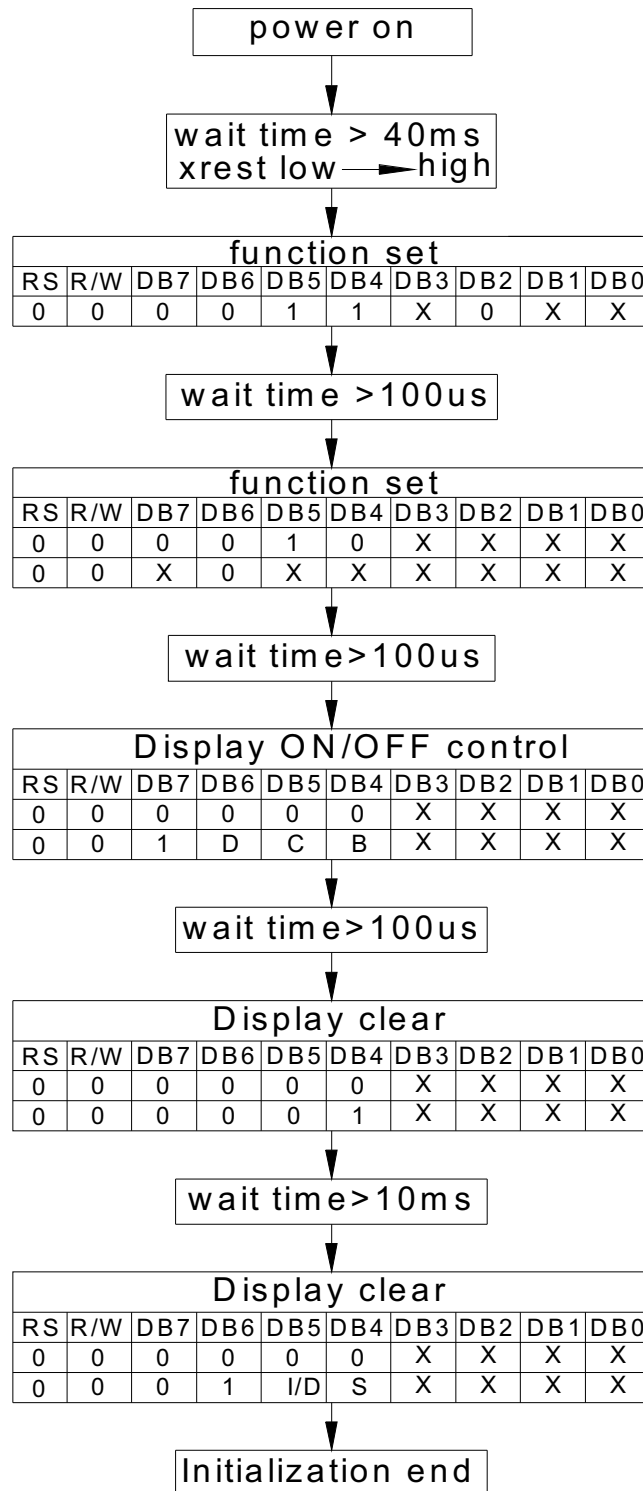
After receiving the start synchronizing bit string, the RW bit(=0), and RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the higher 4 bits of the instruction are placed in the LSB of the first byte, and the lower 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte.

◆ **Initialization procedure**

- 8-bit Interface:



● 4-bit Interface:







NHD-12864EZ

ACB0 爲炳炬炯炭炸炮矧爰牲牯抵狩狼狡玷
ACC0 珊玻玲珍珀玳甚畏界吠吹收疫疤疥
ACD0 疣癸皆皇飯盈益盍盅省眈相眉看瘡
ACE0 眇矜砂研砌欣祇社祇約紉胃背若茂虺
ACF0 突竿岑窳耶胖胥胥苦茄若虺虺述迥
AD40 耐要岫芋范茅莛苟苳赴起躡軍會酃
AD50 致舛岫芋范茅莛苟苳赴起躡軍會酃
AD60 苳赴起躡軍會酃
AD70 計訂訃貞迨郊郎郁郤重門限陋陌
ADA0 迭迫迨迨迨郊郎郁郤重門限陋陌
ADB0 降面革韋非音頁風飛食首香乘毫倍
ADC0 傲俯倦倥倥倥倥倥倥倥倥倥倥倥倥
ADD0 倨俱倡個候倘俳修倭倪俾倫倉兼冤冥
ADE0 冢凍凌准凋剖剗剔剛剗剔剛剗剔剛
ADF0 唐唔嗜嗜嗜嗜嗜嗜嗜嗜嗜嗜嗜嗜
AE40 哦啣唇唇唇唇唇唇唇唇唇唇唇唇
AE50 娑娘娜媚媚媚媚媚媚媚媚媚媚媚媚
AE60 害婁宴宮宵席席席席席席席席席席
AE70 峰島崑崑崑崑崑崑崑崑崑崑崑崑
AEA0 恣恥恐怨恭恩息悄悟悚悍悔悌悅悖
AEB0 扇拳擊擗擗擗擗擗擗擗擗擗擗擗擗
AEC0 挫挨捍擗擗擗擗擗擗擗擗擗擗擗擗
AED0 晁晁晁晁晁晁晁晁晁晁晁晁晁晁晁
AEE0 桌桑栽柴桐架格桃株桅杓移殊殉
AEF0 氣氣氣氣氣氣氣氣氣氣氣氣氣氣
AF40 涇涉浮浚浴浩涌忍泱泱泱泱泱泱泱
AF50 烈烏參特狼狹狹狹狹狹狹狹狹狹
AF60 畔畝畜畚畚畚畚畚畚畚畚畚畚
AF70 飽益盍盍盍盍盍盍盍盍盍盍盍盍
AFA0 秣秣秣秣秣秣秣秣秣秣秣秣秣秣
AFB0 秣秣秣秣秣秣秣秣秣秣秣秣秣秣
AFC0 素素素素素素素素素素素素素素
AFD0 耘耕耜耜耜耜耜耜耜耜耜耜耜耜耜
AFE0 能脊胛胛胛胛胛胛胛胛胛胛胛胛胛
AFF0 荆茸荐草茵茵茵茵茵茵茵茵茵茵
B040 虔蚊蚪蚪蚪蚪蚪蚪蚪蚪蚪蚪蚪蚪
B050 訃訃訃訃訃訃訃訃訃訃訃訃訃訃
B060 躬軒軻軻軻軻軻軻軻軻軻軻軻軻
B070 郡郝郢郢郢郢郢郢郢郢郢郢郢郢
B0A0 陞陞陞陞陞陞陞陞陞陞陞陞陞陞
B0B0 僞僞僞僞僞僞僞僞僞僞僞僞僞僞
B0C0 匾匾匾匾匾匾匾匾匾匾匾匾匾匾
B0D0 參參參參參參參參參參參參參參
B0E0 啤啤啤啤啤啤啤啤啤啤啤啤啤啤
B0F0 埠埠埠埠埠埠埠埠埠埠埠埠埠埠
B140 娼娼娼娼娼娼娼娼娼娼娼娼娼娼
B150 屨屨屨屨屨屨屨屨屨屨屨屨屨屨
B160 常帶帳帷康庸庶庵庾張強彗彬彩
B170 徙徙徙徙徙徙徙徙徙徙徙徙徙徙
B1A0 情悻悻悻悻悻悻悻悻悻悻悻悻悻
B1B0 掠掠掠掠掠掠掠掠掠掠掠掠掠掠
B1C0 推推推推推推推推推推推推推推
B1D0 教教教教教教教教教教教教教教
B1E0 晤晤晤晤晤晤晤晤晤晤晤晤晤晤
B1F0 械械械械械械械械械械械械械械
B240 毫毫毫毫毫毫毫毫毫毫毫毫毫毫
B250 涯涯涯涯涯涯涯涯涯涯涯涯涯涯
B260 深深深深深深深深深深深深深深

B270 梨猜猛猖猓猓猓猓猓猓猓猓猓猓
B2A0 甜盜盛盒窵窵窵窵窵窵窵窵窵窵
B2B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B2C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B2D0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B2E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B2F0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B340 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B350 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B360 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B370 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B3A0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B3B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B3C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B3D0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B3E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B440 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B450 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
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B470 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B4A0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B4B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B4C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
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B4E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B4F0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B540 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
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B5B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B5C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B5D0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B5E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B5F0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B640 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
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B6B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B6C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
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B6E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B6F0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B740 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B750 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B760 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B770 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7A0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7B0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7C0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7D0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7E0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B7F0 窵窵窵窵窵窵窵窵窵窵窵窵窵窵
B840 窵窵窵窵窵窵窵窵窵窵窵窵窵窵









