User's Guide

NHD-10032AZ-FSY-GBW

LCM

(Liquid Crystal Display Graphic Module)

RoHS Compliant

NHD-	Newhaven Display
10032-	100 x 32 pixels
AZ-	Version Line
F-	Transflective
SY-	Side Yellow/Green LED B/L
G-	STN- Gray
B-	6:00 View
W-	Wide Temperature (-20 ~ +70c)

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NEWHAVEN DISPLAY INTERNATIONAL

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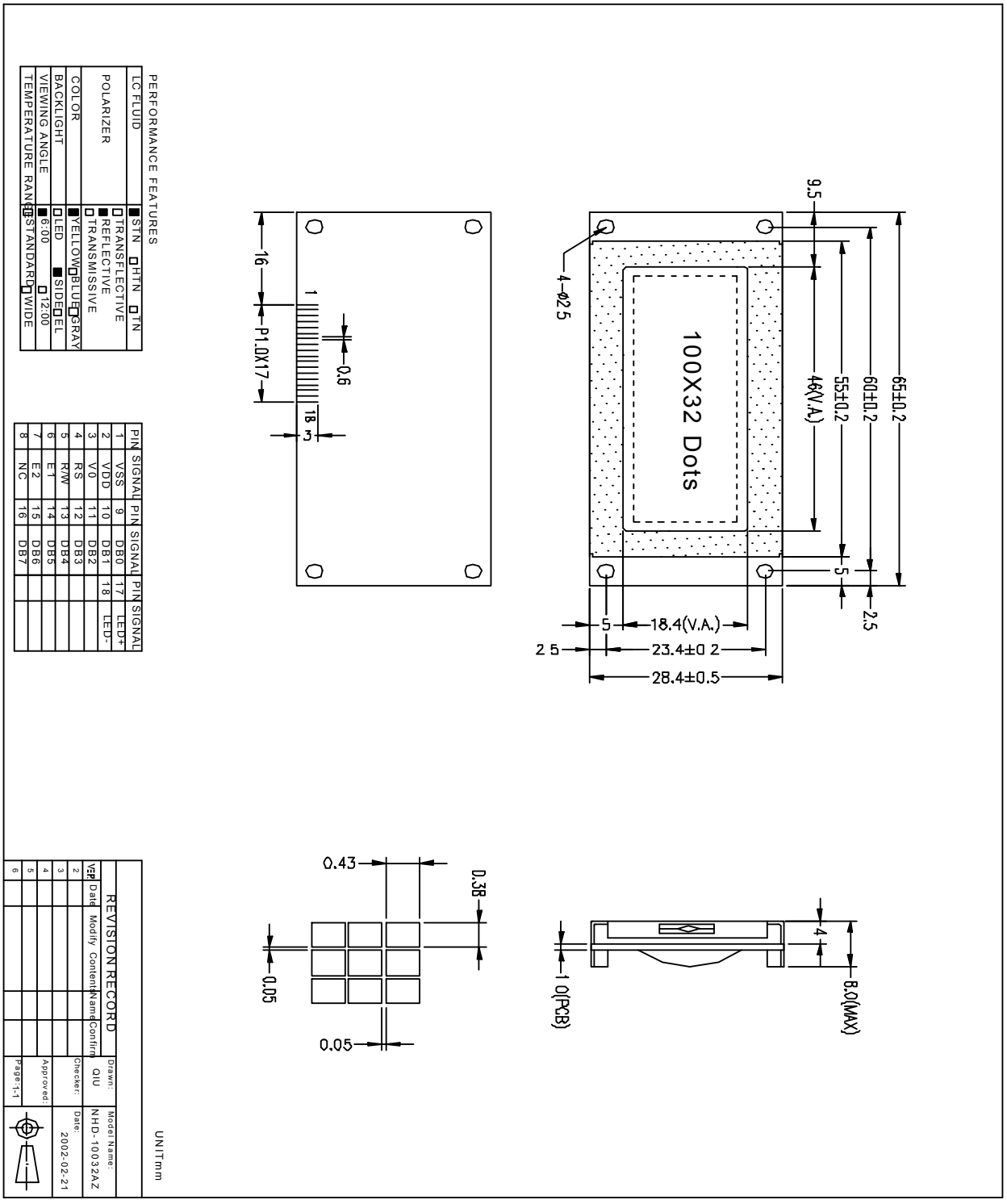
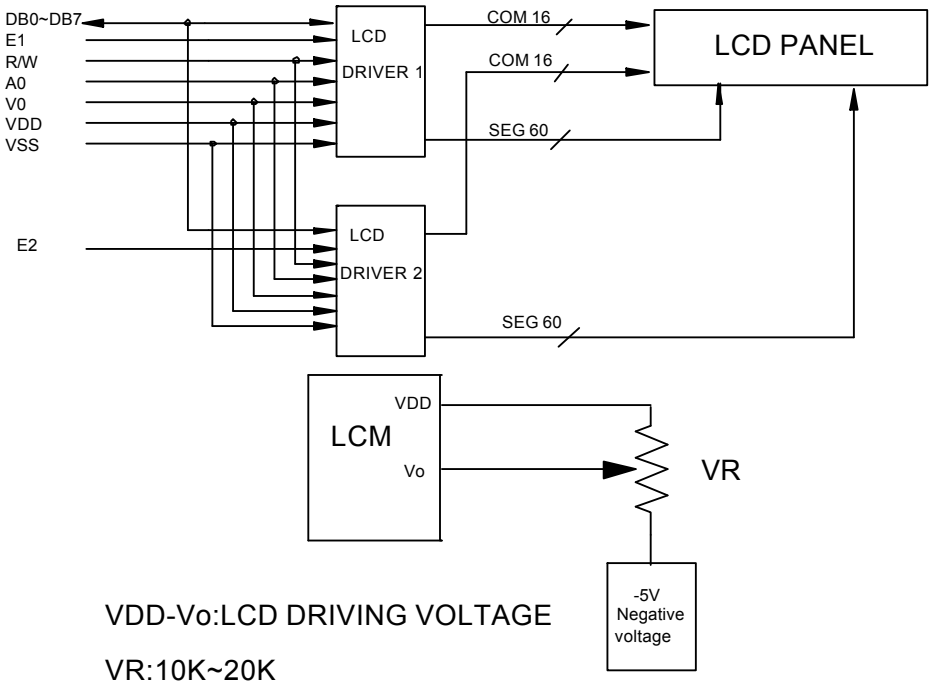


3、 Block diagram



VDD-Vo:LCD DRIVING VOLTAGE

VR:10K~20K

4、Features

Full dot-matrix structure with 100dots x 32 dots
1/32 duty ,1/5 bias
STN LCD, positive
Reflective LCD, yellow green
6 o'clock viewing angle
8 bits parallel data input

5、Mechanical specifications

Outline dimension : 65.0mm(L) x 28.4mm (W)
Viewing area : 46.0mm x 18.4mm
Active area : 42.95mm x 15.31 mm
Dot size : 0.38mm x 0.43 mm
Dot pitch : 0.43 mm x 0.48 mm

6、Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Power Voltage	V_{DD}-V_{SS}	0	7.0	V
Input Voltage	V_O	V_{SS}	V_{DD}	
Operating Temperature Range	V_{OP}	-20	+70	℃
Storage Temperature Range	T_{ST}	-30	+80	

7、Description Of Terminals

Pin No.	Pin Name	Input/ Output	External Connection	Function
1	VSS	—	Power Supply	Signal ground for LCM
2	VDD	—		VDD: +5V
3	VO	—		V_{LCD} adjustment
4	RS	Input	MPU	Register select input "0":Instruction register (when writing) Busy flag address counter (When reading) "1": Data register (when writing & reading)
5	R/W	Input	MPU	Read/write select signal "0" for writing, "1" for reading
6	E1	Input	MPU	Chip enable active "L", SEG (1~60)
7	E2	Input	MPU	Chip enable active "L", SEG (61~120)
8	NC	—	—	Not connected
9 / 12	DB0-DB3	Input/output	MPU	Low-order lines of data bus with 3-state, Bi-directional function for use in data Transaction with the MPU. These lines are Not used when interfacing with a 4-bit Microprocessor.
13 / 16	DB4-DB7	Input/output	MPU	High-order lines of data bus with 3-state, bi-directional function for use in data Transactions with the MPU. DB7 may also be used to check the busy flag.

8、DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_O$	T_A=25℃	—	4.5	—	V
Input voltage	V_{DD}		3	—	5.5	V
Supply current	I_{DD}	V_{DD}=5.0V;T_A=25℃	—	0.75	1.5	mA
Input leakage current	I_{LKG}		—	—	1.0	μA
"H" I evel input voltage	V_{IH}		2.2	—	V_{DD}	V
"L" level input voltage	V_{IL}	Twice initial value or less	0	—	0.6	V
"H" level output voltage	V_{OH}	LOH=0.25mA	2.4	—	—	V
"L" level output voltage	V_{OL}	LOL=1.6mA	—	—	0.4	V

9、Optical Characteristics

For TN Type Display Module (T_a=25℃, V_{DD}=5.0V±0.25V)

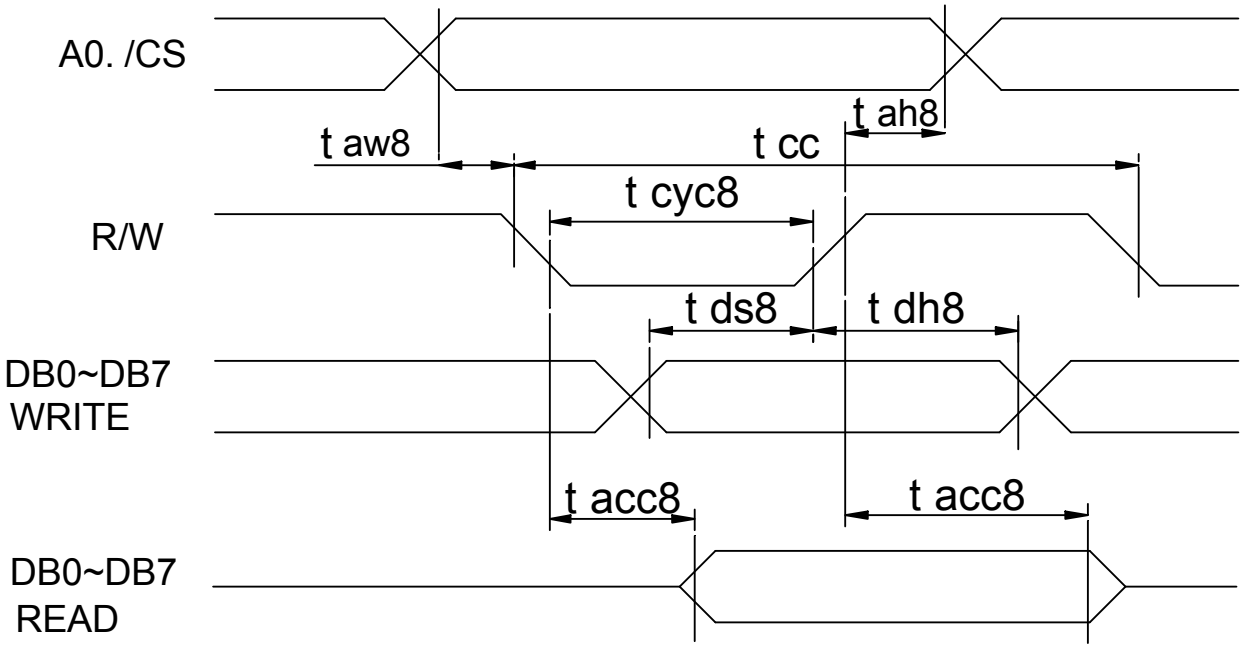
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 4$	-25	—	—	deg
	Φ		-30	—	30	
Contrast ratio	C_r		—	2	—	—
Response time(rise)	T_r	—	—	120	150	ms
Response time(fall)	T_r	—	—	120	150	ms

For STN Type Display Module (T_a=25℃, V_{DD}=5.0V±0.25V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 2$	-60	—	35	deg
	Φ		-40	—	40	
Contrast ratio	C_r		—	6	—	—
Response time(rise)	T_r	—	—	150	250	ms
Response time(fall)	T_r	—	—	150	250	ms

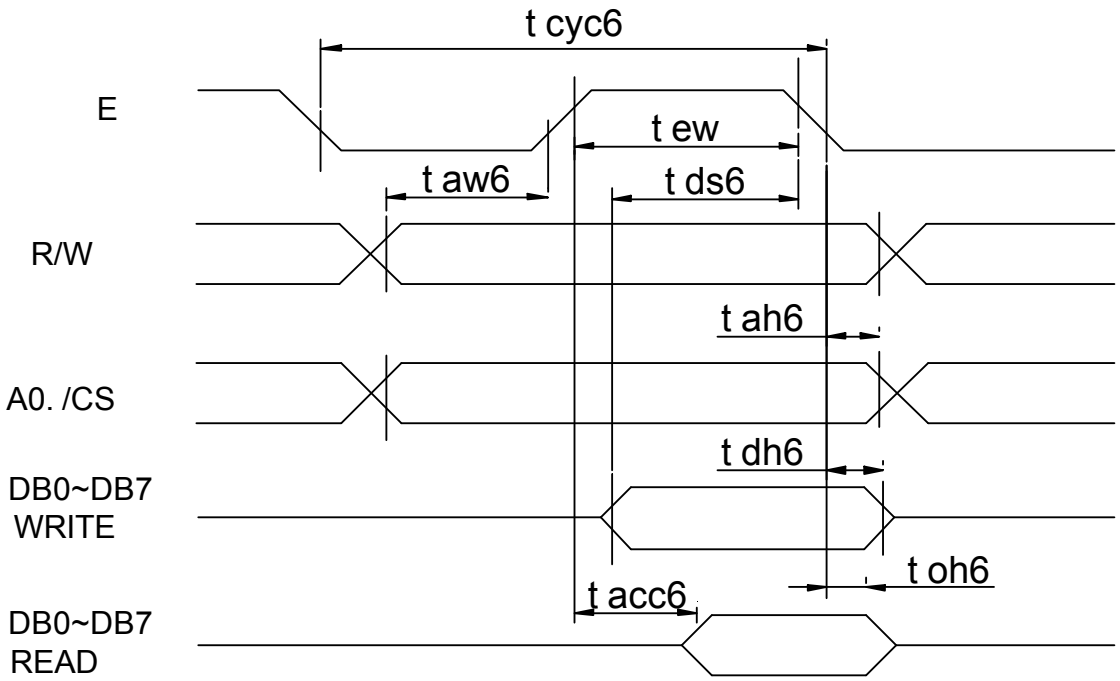
10、Timing Characteristics

MPU bus read/write 1(80-family MPU)



Item	symbol	Conditions	Min.	Max.	unit
System cycle time	t cyc8	—	1000	—	ns
Address setup time	t aw8	—	20	—	ns
Address hold time	t ah8	—	10	—	ns
Data setup time	t ds8	—	80	—	ns
Data hold time	t dh8	—	10	—	ns
Control pulse width	t cc	—	200	—	ns
RD access time	t cc8	CL=100pf	—	90	ns
Output disable time	t ch8		10	60	ns

MPU bus read/write 2(68-family MPU)



Item		symbol	Conditions	Min.	Max.	unit
System cycle time		t cyc6	—	1000	—	ns
Address setup time		t aw6	—	20	—	ns
Address hold time		t ah6	—	10	—	ns
Data setup time		t ds6	—	80	—	ns
Data hold time		t dh6	—	10	—	ns
Access time		t acc6	CL=100pf	—	90	ns
Output disable time		t oh6		10	60	ns
Enable pulse width	Read	t ew	—	100	—	ns
	Write		—	80	—	ns

11、Display command

Parameter	A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0	Note
Display ON /OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off 1: ON ; 0 : OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register
Read status	0	0	1	Busy	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Write data from data bus into display RAM
Read display data	1	0	1	Read data								Read data from display RAM onto data bus
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output 1: CCW output
Static driver ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: static driver, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Select LCD duty cycle 1: 1/32, 0: 1/16
Read-modify write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Table 3 is the command table. The SED1520 series identifies a data bus using a combination of A0 and R/W (RD or WR signals. As the MPU translates a command in the internal timing only (independent from the external clock). Its speed is very high. The busy check is usually not required.

Display ON/OFF (AEH, AFH)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The command turns the display on and off
D=1: display ON D=0: display OFF

Display start line (C0H~DFH)

This command specifies the line address shown if Figure 3 and indicates the display line that corresponds to COM0. the display area begins at the specified line address and continues the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command the vertical smooth scrolling and paging can be used.

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

This command loads the display start line register.

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
/	/	/	/	/	/
1	1	1	1	1	1F

Set page address (B8H~BBH)

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	0	A1	A0

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

Set column address (00H~4FH)

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
/	/	/	/	/	/	/	/
1	0	0	1	1	1	1	4F

Read status

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Busy	ADC	On/off	Reset	A3	A2	A1	A0

Reading the command I/O register (A0=0) yields system status information.

The busy bit indicates whether the driver will accept a command or not.

Busy=1: the driver is currently executing a command or is resetting. No new command will be accepted.

Busy=0: the driver will accept a new command.

The ADC bit indicates the way column addresses are assigned to segment drivers.

ADC=1 Normal. Column address n→ segment driver n.

ADC=0 Inverted. Column address 79 u→ segment driver u.

The ON/OFF bit indicates the current status of the display.

It is the inverse of the polarity of the display ON/OFF command.

ON/OFF=1: display off

ON/OFF=0: display on

The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

Reset=1: currently executing reset command.

Reset=0: normal operation

Write display data

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bit of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read display data

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bit of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC (A0H, A1H)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

This command selects the relationship between display data RAM column addresses and segment drivers.

D=1: SEG0← column address 4FH,…(inverted).

D=0: SEG0← column address 00H,…(normal).

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 go a table of segments and column addresses for the two values of D.

Static drive ON/OFF (A4H, A5H)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

Forces display on and all common outputs to be selected.
D=1:static drive on
D=0:static drive off

Select duty (A8H; A9H)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

This command sets the duty cycle of the LCD drive and is only valid for the SED1520F and SED1522F.it is invalid for the SED1521F, which performs passive operation. The duty cycle of the SED1521F is determined by the externally generated FR signal.

SED1520 SED1522

D=: 1/32 duty cycle 1/16 duty cycle

D=: 1/16 duty cycle 1/8 duty cycle

When using the SED1520F0A, SED1522F0A (having a built-in oscillator) and the SED1521F0A continuously, set the duty as follows:

		SED1521FOA
SED1520FOA	1/32	1/32
	1/16	1/16
SED1522FOA	1/116	1/32
	1/8	1/16

READ-MODIFY-WRITE (E0H)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

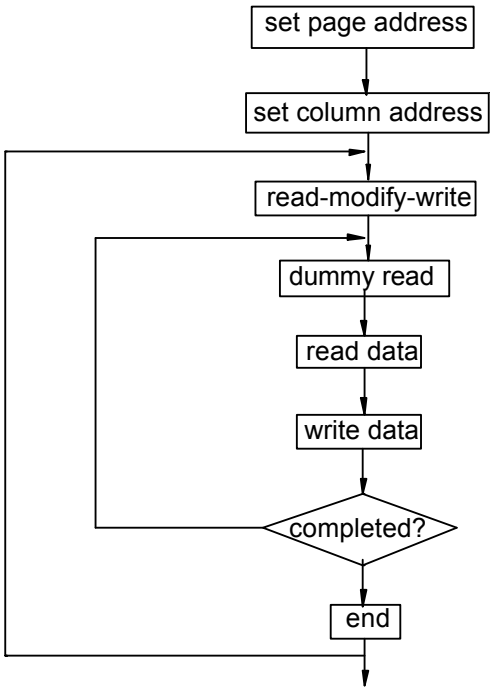
This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an end command is repeated.

Operation sequence during cursor display

When the end command is entered, the column address is returned to the one used during input of read-modify-write command. This function can reduce the load of MPU when data change is repeated at a specific

Display area (such as cursor blinking).

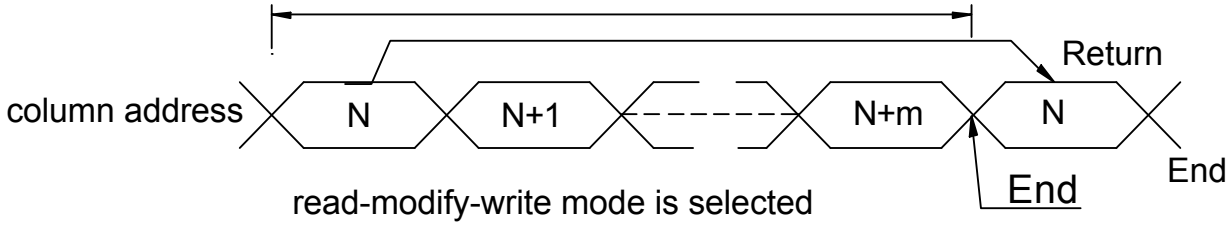
*Any command other than data read or write can be used in the read-modify-write mode. However, the column address set command cannot be used.



END (EEH)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the read-modify-write command.



RESET (E2H)

A0	E (RD)	R/W (/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

This command clears
The display start line register.
And set page address register to 3 page.
It does not affect the contents of the display data RAM.
When the power supply is turned on, a Reset signal is entered in the RES pin. The Reset command cannot be used instead of this Reset signal.