

FOD2200

Low Input Current Logic Gate Optocouplers

Features

- 1kV/ μ s minimum common mode rejection
- Compatible with LSTTL, TTL, and CMOS logic
- Wide V_{CC} range (4.5V to 20V)
- 2.5Mbd guaranteed over temperature
- Low input current (1.6mA)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to 85°C
- Hysteresis
- Safety approvals – UL, CSA, VDE (pending)
- $V_{ISO} = 5kV_{RMS}$

Applications

- Isolation of high speed logic systems
- Computer peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated bus driver
- High speed line receiver

Description

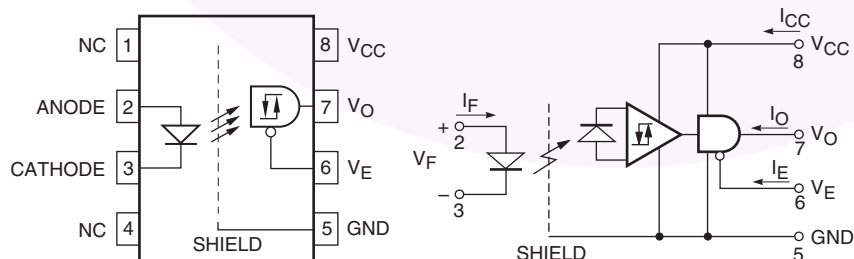
The FOD2200 is an optically coupled logic gate that combine an AlGaAs LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a V_{CC} range of 4.5V to 20V. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed opto-couplers. Logic signals are transmitted with a maximum propagation delay of 300ns. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

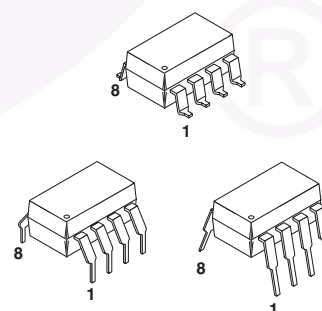
Truth Table (Positive Logic)

| LED | Enable | Output |
|-----|--------|--------|
| On | H | Z |
| Off | H | Z |
| On | L | H |
| Off | L | L |

Functional Block Diagram and Schematic



Package Outlines



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Value | Units |
|-----------------|---|----------------|------------------|
| T_{STG} | Storage Temperature | -40 to +125 | $^\circ\text{C}$ |
| T_{OPR} | Operating Temperature | -40 to +85 | $^\circ\text{C}$ |
| T_{SOL} | Lead Solder Temperature (1.6mm below seating plane) | 260 for 10 sec | $^\circ\text{C}$ |
| EMITTER | | | |
| $I_F (PK)$ | Peak Transient Input Current ($\leq 1\mu\text{s}$ PW, 300pps) | 1.0 | A |
| I_F | Average Forward Input Current | 10 | mA |
| V_R | Reverse Input Voltage | 5.0 | V |
| P_D | Output Power Dissipation (No derating required up to 85°C) | 45 | mW |
| DETECTOR | | | |
| V_{CC} | Supply Voltage | 0 to 20 | V |
| I_O | Average Output Current | 25 | mA |
| V_E | Three State Enable Voltage | -0.5 to 20 | V |
| V_O | Output Voltage | -0.5 to 20 | V |
| P_D | Output Power Dissipation (No derating required up to 85°C) | 150 | mW |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|--------------|----------------------------|------|------|------------------|
| $I_{F(ON)}$ | Forward Input Current | 1.6* | 5 | mA |
| $I_{F(OFF)}$ | Forward Input Current | | 0.1 | mA |
| V_{CC} | Supply Voltage, Output | 4.5 | 20 | V |
| V_{EL} | Enable Voltage, LOW Level | 0 | 0.8 | V |
| V_{EH} | Enable Voltage, HIGH Level | 2.0 | 20 | V |
| T_A | Operating Temperature | 0 | +85 | $^\circ\text{C}$ |
| N | Fan Out (TTL Load) | | 4 | |

*The initial switching threshold is 1.6mA or less. It is recommended that 2.2mA be used to permit at least a 20% CTR degradation guardband.

Electrical Characteristics ($T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ to 20V , $I_{F(ON)} = 1.6\text{mA}$ to 5mA , $V_{EH} = 2\text{V}$ to 20V , $V_{EL} = 0\text{V}$ to 0.8V , $I_{F(OFF)} = 0\text{mA}$ to 0.1mA unless otherwise specified.)⁽¹⁾

Individual Component Characteristics

| Symbol | Parameter | Test Conditions | Min. | Typ.* | Max. | Unit |
|-------------------------|-------------------------------------|---|---|------------|------------------|---------------|
| EMITTER | | | | | | |
| V_F | Input Forward Voltage | $I_F = 5\text{mA}$ $T_A = 25^\circ\text{C}$ | | 1.40 | 1.75 | V |
| B_{VR} | Input Reverse Breakdown Voltage | $I_R = 10\mu\text{A}$ | 5.0 | | | V |
| C_{IN} | Input Capacitance | Pins 2 & 3, $V_F = 0$, $f = 1\text{MHz}$ | | 60 | | pF |
| $\Delta V_F/\Delta T_A$ | Input Diode Temperature Coefficient | $I_F = 5\text{mA}$ | | -1.4 | | mV/°C |
| DETECTOR | | | | | | |
| I_{CCH} | High Level Supply Current | $I_F = 5\text{mA}$, $I_O = \text{Open}$, $V_E = \text{Don't Care}$ | $V_{CC} = 5.5\text{V}$ $V_{CC} = 20\text{V}$ | 3.5 4.0 | 4.5 6.0 | mA |
| I_{CCL} | Low Level Supply Current | $I_F = 0$, $I_O = \text{Open}$, $V_E = \text{Don't care}$ | $V_{CC} = 5.5\text{V}$ $V_{CC} = 20\text{V}$ | 4.4 5.2 | 6.0 7.5 | mA |
| I_{EL} | Low Level Enable Current | $V_E = 0.4\text{V}$ | | -0.1 | -0.32 | mA |
| I_{EH} | High Level Enable Current | $V_E = 2.7\text{V}$ $V_E = 5.5\text{V}$ $V_E = 20\text{V}$ | | | 20 100 250 | μA |
| V_{EH} | High Level Enable Voltage | | 2.0 | | | V |
| V_{EL} | Low Level Enable Voltage | | | | 0.8 | V |

Switching Characteristics ($T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $I_{F(ON)} = 1.6\text{mA}$ to 5mA , $I_{F(OFF)} = 0$ to 0.1mA , $V_{CC} = 4.5\text{V}$ to 20V unless otherwise specified.)

| Symbol | AC Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|------------|---|--|-------------------------|-------|------|------------------|
| T_{PLH} | Propagation Delay Time to Output High Level | With Peaking Capacitor ⁽²⁾⁽⁴⁾ (Fig. 1) | | 120 | 300 | ns |
| T_{PHL} | Propagation Delay Time to Output Low Level | With Peaking Capacitor ⁽³⁾⁽⁴⁾ (Fig. 1) | | 180 | 300 | ns |
| t_r | Output Rise Time (10% to 90%) | ⁽⁵⁾ (Fig. 1) | | 80 | | ns |
| t_f | Output Fall Time (90% to 10%) | ⁽⁶⁾ (Fig. 1) | | 25 | | ns |
| t_{PZH} | Enable Propagation Delay Time to Output High Level | (Fig. 2) | | 40 | | ns |
| t_{PZL} | Enable Propagation Delay Time to Output Low Level | (Fig. 2) | | 50 | | ns |
| T_{PHZ} | Disable Propagation Delay Time from Output High Level | (Fig. 2) | | 95 | | ns |
| T_{PLZ} | Disable Propagation Delay Time from Output Low Level | (Fig. 2) | | 80 | | ns |
| ICM_{HI} | Common Mode Transient Immunity (at Output High Level) | $T_A = 25^\circ\text{C}$, $I_F = 1.6\text{mA}$, $V_{OH} (\text{Min.}) = 2.0\text{V}$, $V_{CC} = 5\text{V}^{(7)}$ (Fig. 3) | $ V_{CM} = 50\text{V}$ | 1000 | | V/ μs |
| ICM_{LI} | Common Mode Transient Immunity (at Output Low Level) | $T_A = 25^\circ\text{C}$, $I_F = 0\text{mA}$, $V_{OL} (\text{Max.}) = 0.8\text{V}$, $V_{CC} = 5\text{V}^{(8)}$ (Fig. 3) | $ V_{CM} = 50\text{V}$ | 1000 | | V/ μs |

*Typical values at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_{F(ON)} = 3\text{mA}$ unless otherwise specified.

Electrical Characteristics (Continued)

Transfer Characteristics ($T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ to 20V , $I_{F(ON)} = 1.6\text{mA}$ to 5mA , $V_{EH} = 2\text{V}$ to 20V , $V_{EL} = 0\text{V}$ to 0.8V , $I_{F(OFF)} = 0\text{mA}$ to 0.1mA unless otherwise specified.)⁽¹⁾

| Symbol | DC Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|-----------|---|--|------|----------------|------|---------------|
| I_{OHH} | Output Leakage Current ($V_{OUT} > V_{CC}$) | $V_{CC} = 4.5\text{V}$, $I_F = 5\text{mA}$ | | 2.0 | 100 | μA |
| | | $V_O = 5.5\text{V}$ | | 2.5 | 500 | |
| V_{OL} | Low Level Output Voltage | $V_{CC} = 4.5\text{V}$, $I_F = 0\text{mA}$, $V_E = 0.4\text{V}$, $I_{OL} = 6.4\text{mA}$ ⁽²⁾ | | 0.33 | 0.5 | V |
| I_{FT} | Input Threshold Current | $V_{CC} = 4.5\text{V}$, $V_O = 0.5\text{V}$, $V_E = 0.4\text{V}$, $I_{OL} = 6.4\text{mA}$ | | | 1.6 | mA |
| V_{OH} | Logic High Output Voltage | $I_{OH} = -2.6\text{mA}$ | 2.4 | $V_{CC} - 1.8$ | | V |
| I_{OZL} | High Impedance State Output Current | $V_O = 0.4\text{V}$, $V_{EN} = 2\text{V}$, $I_F = 5\text{mA}$ | | | -20 | μA |
| I_{OZH} | High Impedance State Output Current | $V_O = 2.4\text{V}$, $V_{EN} = 2\text{V}$, $I_F = 5\text{mA}$ | | | 20 | μA |
| | | $V_O = 5.5\text{V}$, $V_{EN} = 2\text{V}$, $I_F = 5\text{mA}$ | | | 100 | |
| | | $V_O = 20\text{V}$, $V_{EN} = 2\text{V}$, $I_F = 5\text{mA}$ | | | 500 | |
| I_{OSL} | Logic Low Short Circuit Output Current ⁽¹⁰⁾ | $V_O = V_{CC} = 5.5\text{V}$, $I_F = 0\text{mA}$ | 25 | | | mA |
| | | $V_O = V_{CC} = 20\text{V}$, $I_F = 0\text{mA}$ | 40 | | | |
| I_{OSH} | Logic High Short Circuit Output Current ⁽¹⁰⁾ | $V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$, $V_O = \text{GND}$ | -10 | | | mA |
| | | $V_{CC} = 20\text{V}$, $I_F = 5\text{mA}$, $V_O = \text{GND}$ | -25 | | | |
| I_{HYS} | Input Current Hysteresis | $V_{CC} = 4.5\text{V}$ | | 0.03 | | mA |

Isolation Characteristics ($T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified)

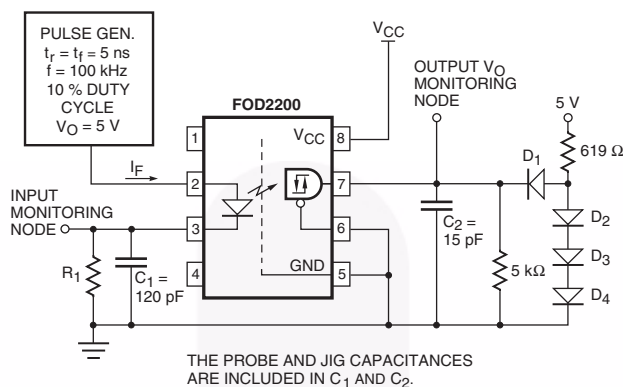
| Symbol | Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|-----------|-----------------------------------|--|------|-----------|------|-----------|
| V_{ISO} | Withstand Insulation Test Voltage | $R_H < 50\%$, $T_A = 25^\circ\text{C}$, $t = 1\text{ min.}$ ⁽⁹⁾ | 5000 | | | V_{RMS} |
| R_{I-O} | Resistance (Input to Output) | $V_{I-O} = 500\text{ VDC}$ ⁽⁹⁾ | | 10^{12} | | Ω |
| C_{I-O} | Capacitance (Input to Output) | $V_{I-O} = 0\text{V}$, $f = 1\text{MHz}$ ⁽⁹⁾ | | 0.6 | | pF |

*Typical values at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_{F(ON)} = 3\text{mA}$ unless otherwise stated.

Notes:

1. The V_{CC} supply to each optoisolator must be bypassed by a $0.1\mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. t_{PLH} – Propagation delay is measured from the 50% level on the LOW to HIGH transition of the input current pulse to the 1.3V level on the LOW to HIGH transition of the output voltage pulse.
3. t_{PHL} – Propagation delay is measured from the 50% level on the HIGH to LOW transition of the input current pulse to the 1.3V level on the HIGH to LOW transition of the output voltage pulse.
4. When the peaking capacitor is omitted, propagation delay times may increase by 100ns.
5. t_r – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
6. t_f – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
7. CM_H – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0\text{V}$).
8. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low state (i.e., $V_{OUT} < 0.8\text{V}$).
9. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.
10. Duration of output short circuit time should not exceed 10ms.

Test Circuits



| R_1 | 2.15 k Ω | 1.10 k Ω | 681 Ω |
|------------|-----------------|-----------------|--------------|
| I_F (ON) | 1.6 mA | 3 mA | 5 mA |

ALL DIODES ARE 1N916 OR 1N3064.

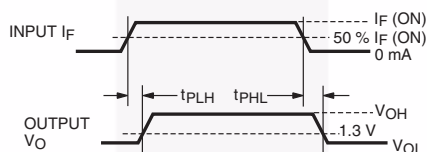


Fig. 1. Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f

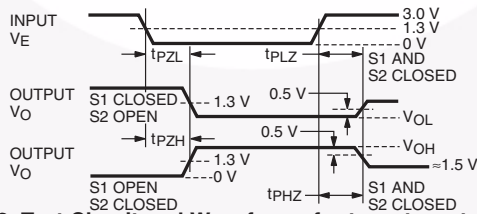
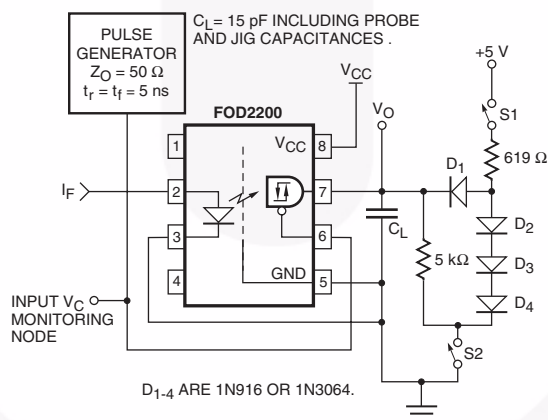


Fig. 2. Test Circuit and Waveforms for t_{PHZ} , t_{PZH} , t_{PLZ} , and t_{PZL}

Test Circuits (Continued)

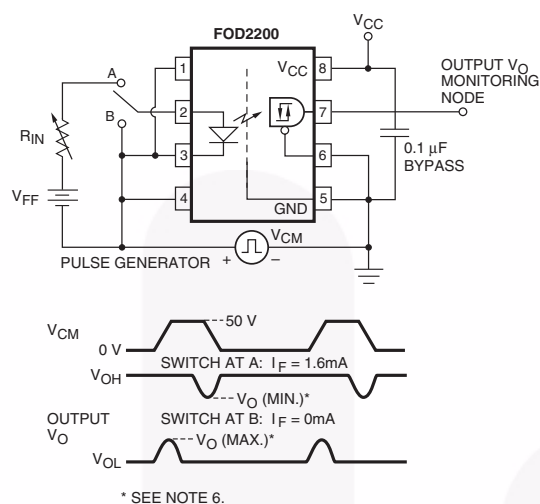


Fig. 3. Test Circuit and Typical Waveforms for Common Mode Transient Immunity

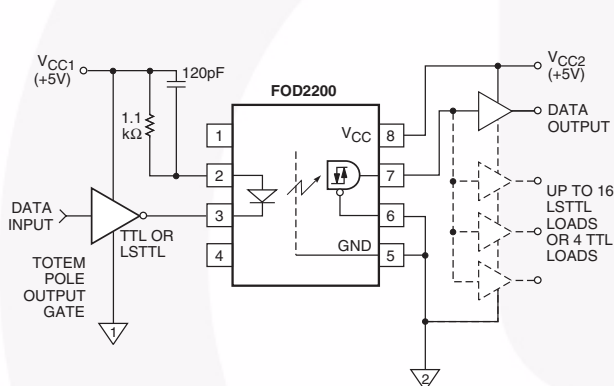


Figure 4. Recommended LSTTL to LSTTL Circuit

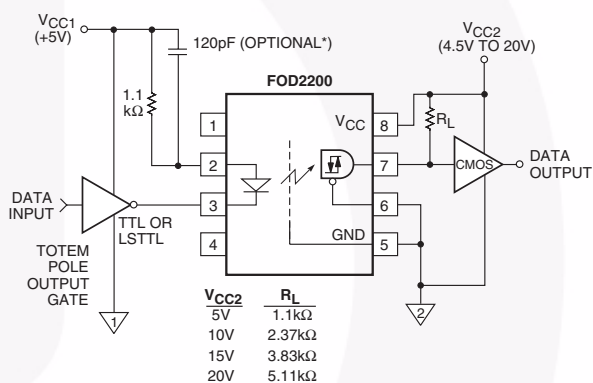


Figure 5. LSTTL to CMOS Interface Circuit

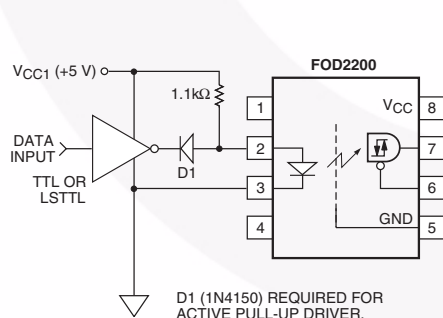


Figure 6. Recommended LED Drive Circuit

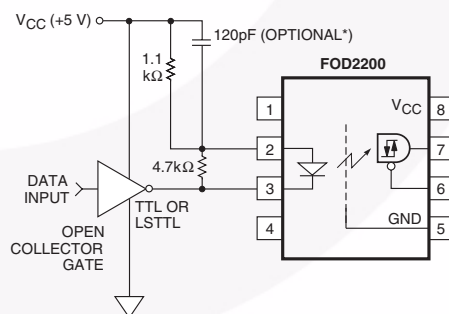


Figure 7. Series LED Drive with Open Collector Gate (4.7kΩ Resistor Shunts I_{OH} from the LED)

*The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Typical Performance Curves

Figure 8. Input Forward Current vs Forward Voltage

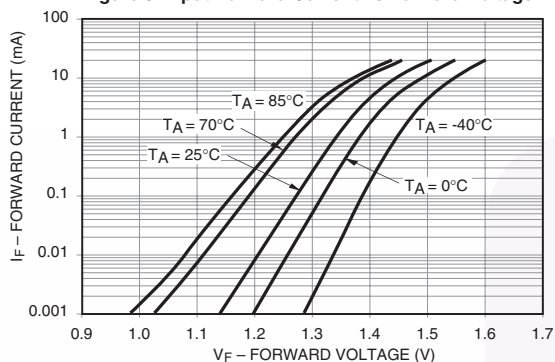


Figure 9. Output Voltage vs. Input Forward Current

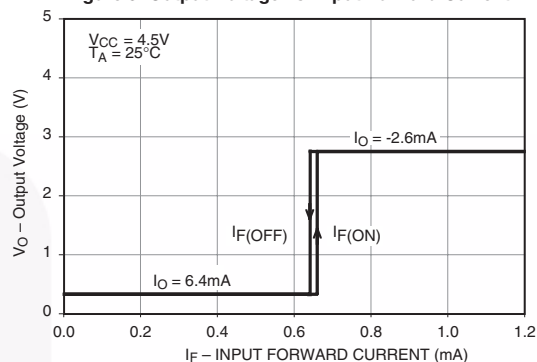


Figure 10. Input Threshold Current vs. Ambient Temperature

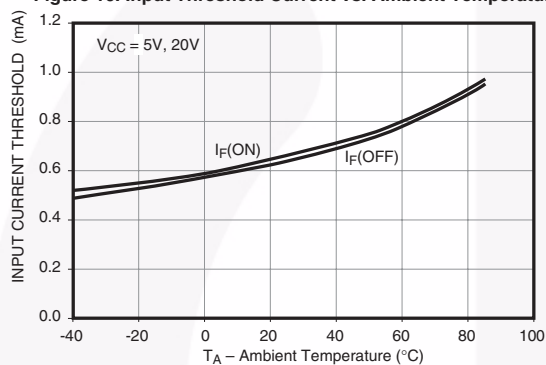


Figure 11. Logic Low Output Voltage vs. Ambient Temperature

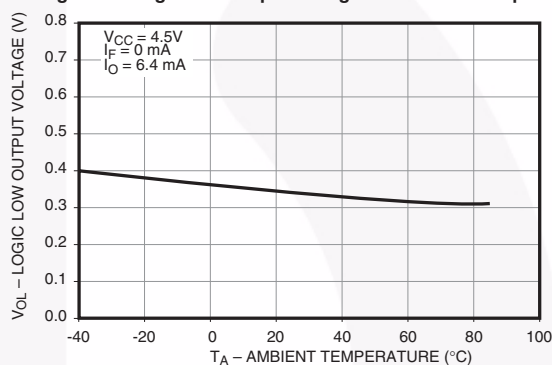


Figure 12. Logic High Output Voltage vs. Supply Voltage

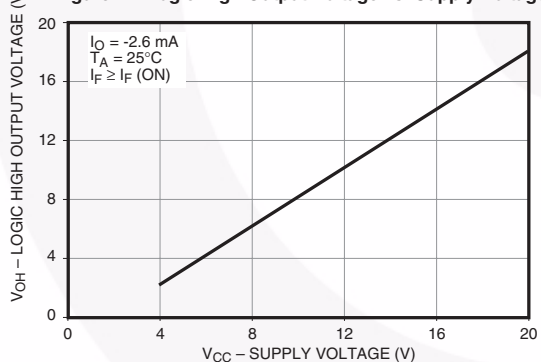


Figure 13. Logic High Output Current vs. Ambient Temperature

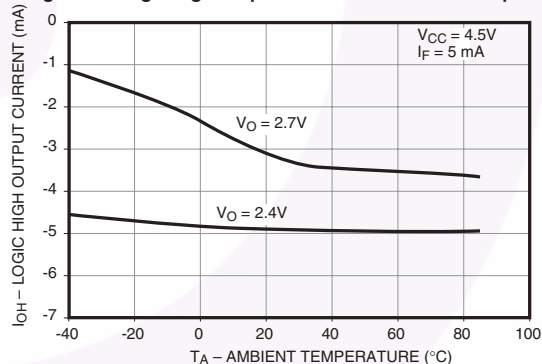


Figure 14. Propagation Delay vs Ambient Temperature

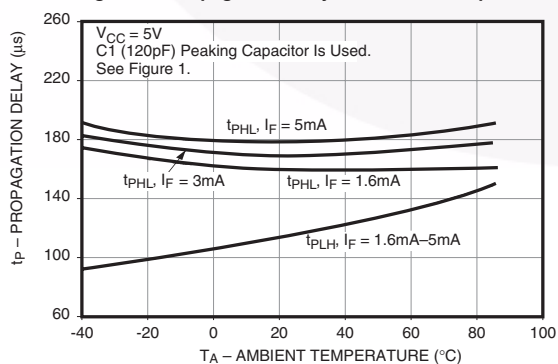
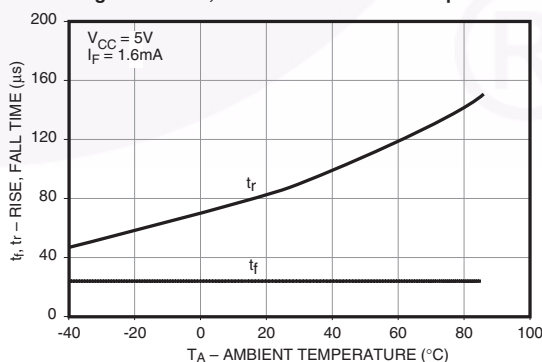
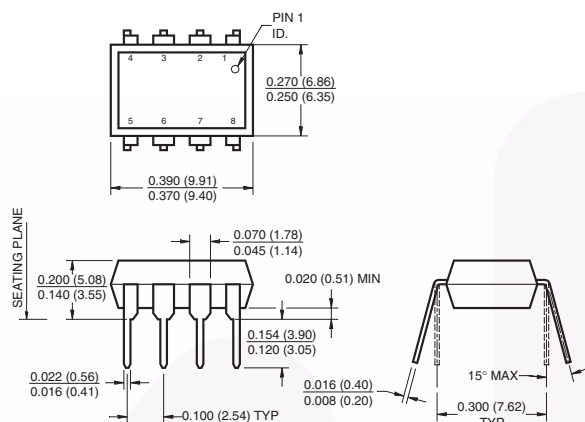


Figure 15. Rise, Fall Time vs Ambient Temperature

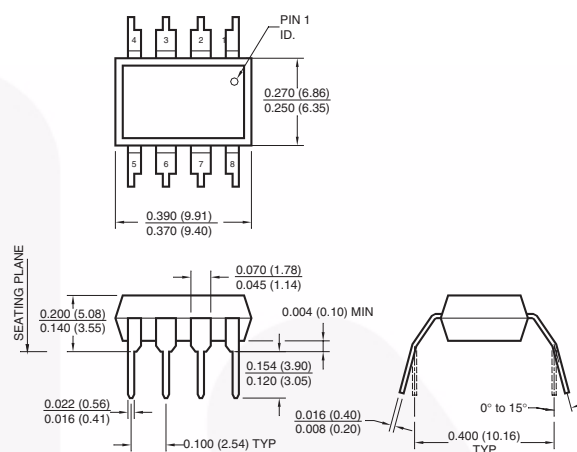


Package Dimensions

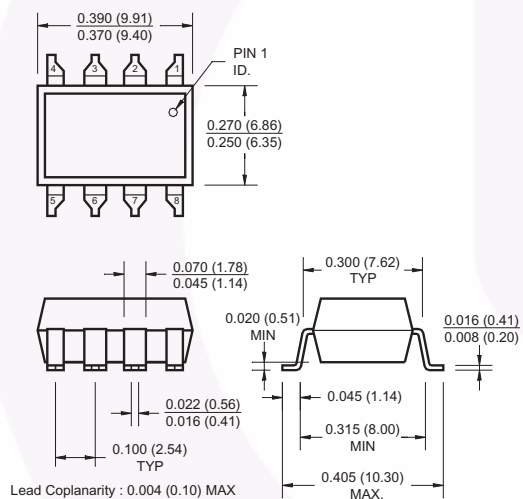
Through Hole



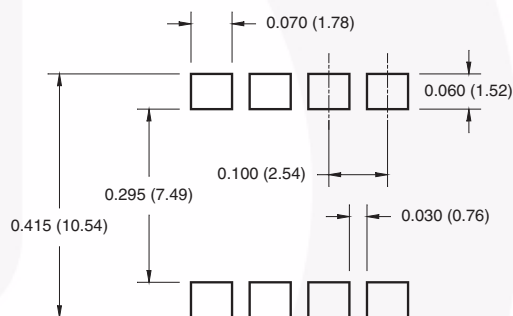
0.4" Lead Spacing



Surface Mount



8-Pin DIP – Land Pattern



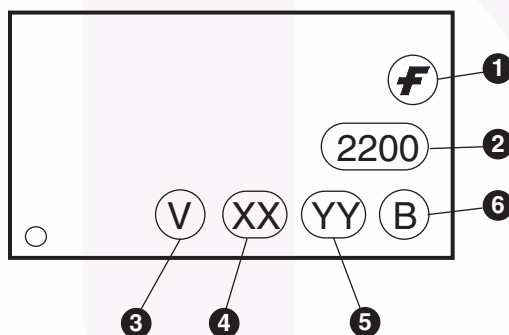
Note:

All dimensions are in inches (millimeters)

Ordering Information

| Option | Example Part Number | Description |
|-----------|---------------------|---------------------------------------|
| No Option | FOD2200 | Standard Through Hole |
| S | FOD2200S | Surface Mount Lead Bend |
| SD | FOD2200SD | Surface Mount; Tape and Reel |
| T | FOD2200T | 0.4" Lead Spacing |
| V | FOD2200V | VDE0884 |
| TV | FOD2200TV | VDE0884; 0.4" Lead Spacing |
| SV | FOD2200SV | VDE0884; Surface Mount |
| SDV | FOD2200SDV | VDE0884; Surface Mount; Tape and Reel |

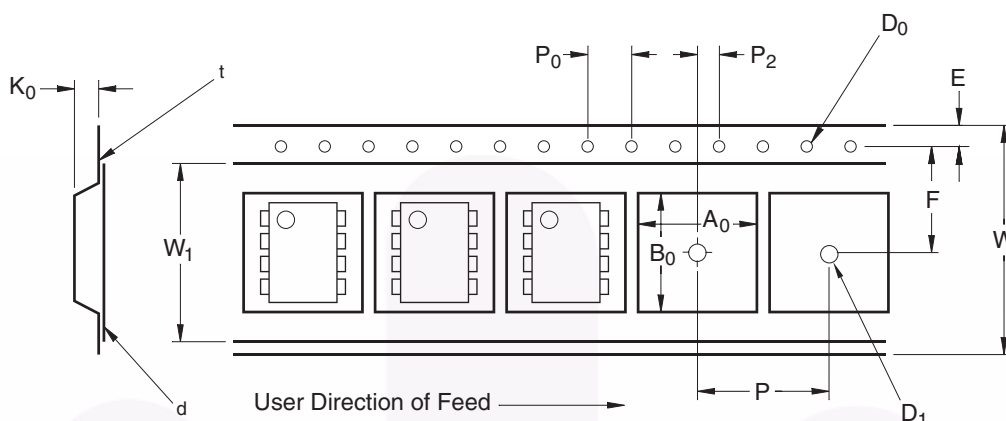
Marking Information



Definitions

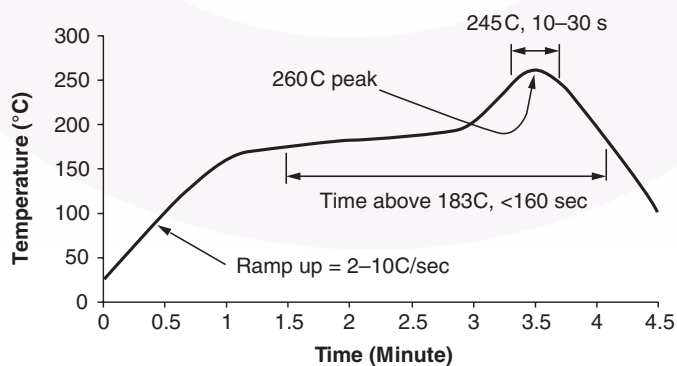
| | |
|---|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | Two digit year code, e.g., '03' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

Carrier Tape Specifications



| Symbol | Description | Dimension in mm |
|----------------|---------------------------------|-----------------|
| W | Tape Width | 16.0 ± 0.3 |
| t | Tape Thickness | 0.30 ± 0.05 |
| P ₀ | Sprocket Hole Pitch | 4.0 ± 0.1 |
| D ₀ | Sprocket Hole Diameter | 1.55 ± 0.05 |
| E | Sprocket Hole Location | 1.75 ± 0.10 |
| F | Pocket Location | 7.5 ± 0.1 |
| P ₂ | | 4.0 ± 0.1 |
| P | Pocket Pitch | 12.0 ± 0.1 |
| A ₀ | Pocket Dimensions | 10.30 ± 0.20 |
| B ₀ | | 10.30 ± 0.20 |
| K ₀ | | 4.90 ± 0.20 |
| W ₁ | Cover Tape Width | 1.6 ± 0.1 |
| d | Cover Tape Thickness | 0.1 max |
| | Max. Component Rotation or Tilt | 10° |
| R | Min. Bending Radius | 30 |

Reflow Profile



- Peak reflow temperature: 260°C (package surface temperature)
- Time of temperature higher than 183°C for 160 seconds or less
- One time soldering reflow is recommended





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FAST®
FastvCore™
FETBench™

FlashWriter®*
FPS™
F-PFS™
FRFET®
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Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
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TinyBuck™
TinyCalc™
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Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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