Full/Low Speed 5 kV USB Digital Isolator

ADuM4160

FEATURES

- USB 2.0 compatible
- Low and full speed data rate: 1.5 Mbps and 12 Mbps
- Bidirectional communication
- 4.5 V to 5.5 V V_{BUS} operation
  - 7 mA maximum upstream supply current @ 1.5 Mbps
  - 8 mA maximum upstream supply current @ 12 Mbps
  - 2.3 mA maximum upstream idle current
- Upstream short-circuit protection
- Class 3A contact ESD performance per ANSI/ESD STM5.1-2007
- High temperature operation: 105°C
- High common-mode transient immunity: >25 kV/µs
- 16-lead SOIC wide-body package
- RoHS compliant
- Safety and regulatory approvals
  - UL recognition: 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
    - IEC 60601-1: 125 V rms (reinforced)
    - IEC 60950-1: 380 V rms (reinforced)
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 846 V peak

APPLICATIONS

- USB peripheral isolation
- Isolated USB hub
- Medical applications

GENERAL DESCRIPTION

The ADuM4160[1] is a USB port isolator, based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics and are easily integrated with low and full speed USB-compatible peripheral devices.

FUNCTIONAL BLOCK DIAGRAM

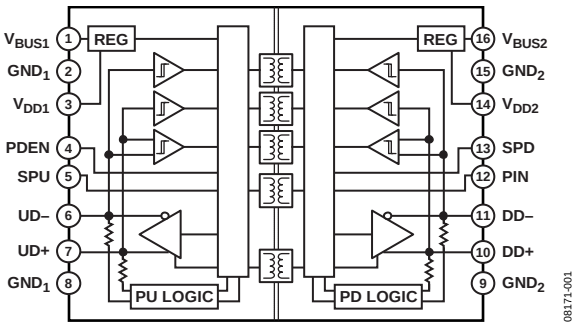

Figure 1.

Many microcontrollers implement USB so that it presents only the D+ and D− lines to external pins. This is desirable in many cases because it minimizes external components and simplifies the design; however, this presents particular challenges when isolation is required. USB lines must automatically switch between actively driving D+/D−, receiving data, and allowing external resistors to set the idle state of the bus. The ADuM4160 provides mechanisms for detecting the direction of data flow and control over the state of the output buffers. Data direction is determined on a packet-by-packet basis.

The ADuM4160 uses the edge detection based *i*Coupler technology in conjunction with internal logic to implement a transparent, easily configured, upstream facing port isolator. Isolating an upstream facing port provides several advantages in simplicity, power management, and robust operation.

The isolator has propagation delay comparable to that of a standard hub and cable. It operates with the bus voltage on either side ranging from 4.5 V to 5.5 V, allowing connection directly to V_{BUS} by internally regulating the voltage to the signaling level. The ADuM4160 provides isolated control of the pull-up resistor to allow the peripheral to control connection timing. The device has a low idle current; a suspend mode is required. A 2.5 kV version, the ADuM3160, is also available.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329. Other patents pending.

Rev. B

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REVISION HISTORY

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Changes to Features Section 1
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9/09—Rev. 0 to Rev. A

Added USB Logo, Reformatted Page 1 1

7/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

4.5 V ≤ V_{BUS1} ≤ 5.5 V, 4.5 V ≤ V_{BUS2} ≤ 5.5 V; 3.1 V ≤ V_{DD1} ≤ 3.6 V, 3.1 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Each voltage is relative to its respective ground.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Total Supply Current[1]						
1.5 Mbps						
V_{DD1} or V_{BUS1} Supply Current	$I_{DD1 (L)}$		5	7	mA	750 kHz logic signal rate C_L = 450 pF
V_{DD2} or V_{BUS2} Supply Current	$I_{DD2 (L)}$		5	7	mA	750 kHz logic signal rate C_L = 450 pF
12 Mbps						
V_{DD1} or V_{BUS1} Supply Current	$I_{DD1 (F)}$		6	8	mA	6 MHz logic signal rate C_L = 50 pF
V_{DD2} or V_{BUS2} Supply Current	$I_{DD2 (F)}$		6	8	mA	6 MHz logic signal rate C_L = 50 pF
Idle Current						
V_{DD1} or V_{BUS1} Idle Current	$I_{DD1 (I)}$		1.7	2.3	mA	
Input Currents	I_{DD-}, I_{DD+}, I_{UD+}, I_{UD-}, I_{SPD}, I_{PIN}, I_{SPU}, I_{PDEN}	−1	+0.1	+1	µA	0 V ≤ V_{DD-}, V_{DD+}, V_{UD+},V_{UD-}, V_{SPD}, V_{PIN}, V_{SPU}, V_{PDEN} ≤ 3.0
Single-Ended Logic High Input Threshold	V_{IH}	2.0			V	
Single-Ended Logic Low Input Threshold	V_{IL}			0.8	V	
Single-Ended Input Hysteresis	V_{HST}		0.4		V	
Differential Input Sensitivity	V_{DI}	0.2			V	$\lvert V_{XD+} - V_{XD-} \rvert$
Logic High Output Voltages	V_{OH}	2.8		3.6	V	R_L = 15 kΩ, V_L = 0 V
Logic Low Output Voltages	V_{OL}	0		0.3	V	R_L = 1.5 kΩ, V_L = 3.6 V
V_{DD1} and V_{DD2} Supply Undervoltage Lockout	V_{UVLO}	2.4		3.1	V	
V_{BUS1} Supply Undervoltage Lockout	V_{UVLOB1}	3.5		4.35	V	
V_{BUS2} Supply Undervoltage Lockout	V_{UVLOB2}	3.5		4.4	V	
Transceiver Capacitance	C_{IN}		10		pF	UD+, UD−, DD+, DD− to ground
Capacitance Matching			10		%	
Full Speed Driver Impedance	Z_{OUTH}	4		20	Ω	
Impedance Matching			10		%	
SWITCHING SPECIFICATIONS, I/O PINS LOW SPEED						
Low Speed Data Rate			1.5		Mbps	C_L = 50 pF
Propagation Delay[2]	t_{PHLL}, t_{PLHL}			325	ns	C_L = 50 pF, SPD = SPU = low V_{DD1}, V_{DD2} = 3.3 V
Side 1 Output Rise/Fall Time (10% to 90%) Low Speed	t_{RL}/t_{FL}	75		300	ns	C_L = 450 pF SPD = SPU = low V_{DD1}, V_{DD2} = 3.3 V
Low Speed Differential Jitter, Next Transition	$\lvert t_{LJN} \rvert$		45		ns	C_L = 50 pF
Low Speed Differential Jitter, Paired Transition	$\lvert t_{LJP} \rvert$		15		ns	C_L = 50 pF
SWITCHING SPECIFICATIONS, I/O PINS FULL SPEED						
Full Speed Data Rate			12		Mbps	C_L = 50 pF
Propagation Delay[2]	t_{PHLF}, t_{PLHF}	20	60	70	ns	C_L = 50 pF SPD = SPU = high, V_{DD1}, V_{DD2} = 3.3 V
Output Rise/Fall Time (10% to 90%) Full Speed	t_{RF}/t_{FF}	4		20	ns	C_L = 50 pF SPD = SPU = high, V_{DD1}, V_{DD2} = 3.3 V
Full Speed Differential Jitter, Next Transition	$\lvert t_{FJN} \rvert$		3		ns	C_L = 50 pF
Full Speed Differential Jitter, Paired Transition	$\lvert t_{FJP} \rvert$		1		ns	C_L = 50 pF

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
For All Operating Modes						
Common-Mode Transient Immunity						
At Logic High Output[3]	$\|CM_H\|$	25	35		kV/µs	V_{UD+}, V_{UD-}, V_{DD+}, V_{DD-} = V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
At Logic Low Output[3]	$\|CM_L\|$	25	35		kV/µs	V_{UD+}, V_{UD-}, V_{DD+}, V_{DD-} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] The supply current values for the device running at a fixed continuous data rate at 50% duty cycle alternating J and K states. Supply current values are specified with USB-compliant load present.
[2] Propagation delay of the low speed DD+ to UD+ or DD − to UD− in either signal directionis measured from the 50% level of the rising or falling edge, to the 50% level of the rising or falling edge of the corresponding output signal.
[3] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

[1] Device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4160 is approved by the organizations listed in Table 3. Refer to Table 8 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3.

UL	CSA	VDE
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage Reinforced insulation per IEC 60601-1 125 V rms (176 V peak) maximum working voltage	Reinforced insulation, 846 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM4160 is proof tested by applying an insulation test voltage ≥6000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM4160 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 5.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1590	V peak
Input-to-Output Test Voltage, Method a	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			1375	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1+ Side 2 Current		I_{S1}	550	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

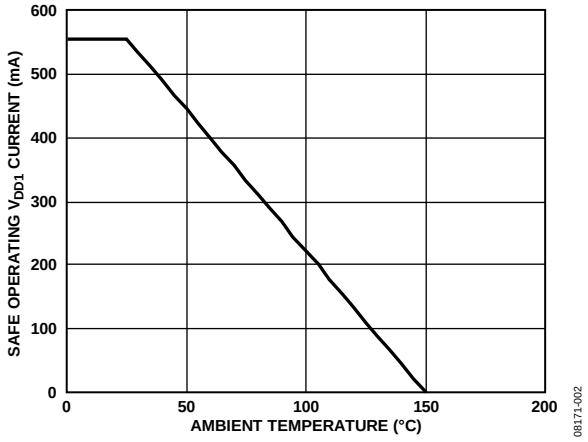

Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{BUS1}, V_{BUS2}	3.1	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{BUS1}, V_{BUS2}, V_{DD1}, V_{DD2})[1]	−0.5 V to +6.5 V
Input Voltage (V_{UD+},V_{UD-}, V_{SPU})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{DD-}, V_{DD+}, V_{SPD}, V_{PIN})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI}, V_{BUS1}, and V_{DD2}, V_{BUS2} refer to the supply voltages on the upstream and downstream sides of the coupler, respectively.
[3] See Figure 2 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	537	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	848	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	848	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	537	V peak	Maximum approved working voltage per IEC 60950-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

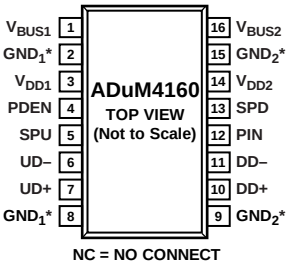

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Direction	Description
1	V_{BUS1}	Power	Input Power Supply for Side 1. Where the isolator is powered by the USB bus voltage, 4.5 V to 5.5 V, connect V_{BUS1} to the USB power bus. Where the isolator is powered from a 3.3 V power supply, connect V_{BUS1} to V_{DD1} and to the external 3.3 V power supply. Bypass to GND_1 is required.
2	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
3	V_{DD1}	Power	Power Supply for Side 1. Where the isolator is powered by the USB bus voltage, 4.5 V to 5.5 V, the V_{DDI} pin should be used for a bypass capacitor to GND_1. Signal lines that may require pull up, such as PDEN and SPU, should be tied to this pin. Where the isolator is powered from a 3.3 V power supply, connect V_{BUS1} to V_{DD1} and to the external 3.3 V power supply. Bypass to GND_1 is required.
4	PDEN	Input	Pull-Down Enable. This pin is read when exiting reset. For standard operation, connect this pin to V_{DD1}. When connected to GND_1 while exiting from reset, the downstream pull-down resistors are disconnected, allowing buffer impedance measurements.
5	SPU	Input	Speed Select Upstream Buffer. Active high logic input. Selects full speed slew rate, timing, and logic conventions when SPU is high, and low speed slew rate, timing, and logic conventions when SPU is tied low. This input must be set high via connection to V_{DD1} or set low via connection to GND_1 and must match Pin 13.
6	UD–	I/O	Upstream D–.
7	UD+	I/O	Upstream D+.
8	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Return	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream D+.
11	DD–	I/O	Downstream D–.
12	PIN	Input	Upstream Pull-Up Enable. PIN controls the power connection to the pull-up for the upstream port. It can be tied to V_{DD2} for operation on power-up, or tied to an external control signal for applications requiring delayed enumeration.
13	SPD	Input	Speed Select Downstream Buffer. Active high logic input. Selects full speed slew rate, timing, and logic conventions when SPD is high, and low speed slew rate, timing, and logic conventions when SPD is tied low. This input must be set high via connection to V_{DD2} or low via connection to GND_2, and must match Pin 5.
14	V_{DD2}	Power	Power Supply for Side 2. Where the isolator is powered by the USB bus voltage, 4.5 V to 5.5 V, the V_{DD2} pin should be used for a bypass capacitor to GND_2. Signal lines that may require pull-up, such as SPD, can be tied to this pin. Where the isolator is powered from a 3.3 V power supply, connect V_{BUS2} to V_{DD2} and to the external 3.3 V power supply. Bypass to GND_2 is required.
15	GND_2	Return	Ground 2. Ground reference for Isolator Side 2.
16	V_{BUS2}	Power	Input Power Supply for Side 2. Where the isolator is powered by the USB bus voltage, 4.5 V to 5.5 V, connect V_{BUS2} to the USB power bus. Where the isolator is powered from a 3.3 V power supply, connect V_{BUS2} to V_{DD2} and to the external 3.3 V power supply. Bypass to GND_2 is required.

Table 10. Truth Table, Control Signals, and Power (Positive Logic)[1]

V_{SPU} Input	V_{BUS1}, V_{DD1} State	V_{UD+}, V_{UD-} State	V_{SPD} Input	V_{BUS2}, V_{DD2} State	V_{DD+}, V_{DD-} State	V_{PIN} Input	Notes
H	Powered	Active	H	Powered	Active	H	Input and output logic set for full speed logic convention and timing.
L	Powered	Active	L	Powered	Active	H	Input and output logic set for low speed logic convention and timing.
L	Powered	Active	H	Powered	Active	H	Not allowed: V_{SPU} and V_{SPD} must be set to the same value. USB host detects communications error.
H	Powered	Active	L	Powered	Active	H	Not allowed: V_{SPU} and V_{SPD} must be set to the same value. USB host detects communications error.
X	Powered	Z	X	Powered	Z	L	Upstream Side 1 presents a disconnected state to the USB cable.
X	Unpowered	X	X	Powered	Z	X	When power is not present on V_{DD1}, the downstream data output drivers revert to high-Z within 32 bit times. The downstream side initializes in high-Z state.
X	Powered	Z	X	Unpowered	X	X	When power is not present on the V_{DD2}, the upstream side disconnects the pull-up and disables the upstream drivers within 32 bit times.

[1] H represents logic high input or output, L represents logic low input or output, X represents the don't care logic input or output, and Z represents the high impedance output state.

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

USB isolation in the D+/D− lines is challenging for several reasons. First, access to the output enable signals is normally required to control a transceiver. Some level of intelligence must be built into the isolator to interpret the data stream and determine when to enable and disable its upstream and downstream output buffers. Second, the signal must be faithfully reconstructed on the output side of the coupler while retaining precise timing and not passing transient states such as invalid SE0 and SE1 states. In addition, the part must meet the low power requirements of the suspend mode.

The *i*Coupler technology is based on edge detection, and, therefore, lends itself well to the USB application. The flow of data through the device is accomplished by monitoring the inputs for activity and setting the direction for data transfer based on a transition from the idle (J) state. When data direction is established, data is transferred until either an end-of-packet (EOP) or a sufficiently long idle state is encountered. At this point, the coupler disables its output buffers and monitors its inputs for the next activity

During the data transfers, the input side of the coupler holds its output buffers disabled. The output side enables its output buffers and disables edge detection from the input buffers. This allows the data to flow in one direction without wrapping back through the coupler making the *i*Coupler latch. Logic is included to eliminate any artifacts due to different input thresholds of the differential and single-ended buffers. The input state is transferred across the isolation barrier as one of three valid states, J, K, or SE0. The signal is reconstructed at the output side with a fixed time delay from the input side differential input.

The *i*Coupler does not have a special suspend mode, nor does it need one because its power supply current is below the suspend current limit of 2.5 mA when the USB bus is idle.

The ADuM4160 is designed to interface with an upstream facing low/full speed USB port by isolating the D+/D− lines. An upstream facing port supports only one speed of operation, thus, the speed related parameters, J/K logic levels, and D+/D− slew rate are set to match the speed of the upstream facing peripheral port (see Table 10).

A control line on the downstream side of the ADuM4160 activates a pull-up resistor integrated into the upstream side. This allows the downstream port to control when the upstream port attaches to the USB bus. The pin can be tied to the peripheral pull-up, a control line, or the V_{DD2} pin, depending on when the initial bus connect is to be performed.

PRODUCT USAGE

The ADuM4160 is designed to be integrated into a USB peripheral with an upstream facing USB port as shown in Figure 4. The key design points are:

1. The USB host provides power for the upstream side of the ADuM4160 through the cable.
2. The peripheral supply provides power to the downstream side of the ADuM4160
3. The DD+/DD− lines of the isolator interface with the peripheral controller, and the UD+/UD− lines of the isolator connect to the cable or host.
4. Peripheral devices have a fixed data rate that is set at design time. The ADuM4160 has configuration pins, SPU and SPD, that determine the buffer speed and logic convention for each side. These must be set identically and match the desired peripheral speed.
5. USB enumeration begins when either the UD+ or UD− line is pulled high at the peripheral end of the USB cable, which is the upstream side of the ADuM4160. Control of the timing of this event is provided by the PIN input on the downstream side of the coupler.
6. Pull-up and pull-down resistors are implemented inside the coupler. Only external series resistors and bypass capacitors are required for operation.

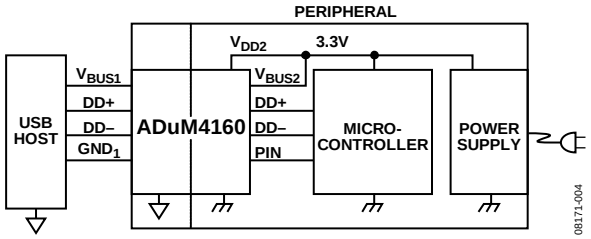

Figure 4. Typical Application

Other than the delayed application of pull-up resistors, the ADuM4160 is transparent to USB traffic, and no modifications to the peripheral design are required to provide isolation. The isolator adds propagation delay to the signals comparable to a hub and cable. Isolated peripherals must be treated as if there were a built-in hub when determining the maximum number of hubs in a data chain.

Hubs can be isolated like any other peripheral. Isolated hubs can be created by placing an ADuM4160 on the upstream port of a hub chip. This configuration can be made compliant if counted as two hub delays. The hub chip allows the ADuM4160 to operate at full speed yet maintains compatibility with low speed devices.

COMPATIBILITY OF UPSTREAM APPLICATIONS

The ADuM4160 is designed specifically for isolating a USB peripheral. However, the chip does have two USB interfaces that meet the electrical requirements for driving USB cables. This opens the possibility of implementing isolation in downstream USB ports such as isolated cables, which have generic connections to both upstream and downstream devices, as well as isolating host ports.

In a fully compliant application, a downstream facing port must be able to detect whether a peripheral is low speed or full speed based on the application of the upstream pull-up. The buffers and logic conventions must adjust to match the requested speed. Because the ADuM4160 sets its speed by hard wiring pins, the part cannot adjust to different peripherals on the fly.

The practical result of using the ADuM4160 in a host port is that the port works at a single speed. This behavior is acceptable in embedded host applications; however, this type of interface is not fully compliant as a general-purpose USB port.

Isolated cable applications have a similar issue. The cable operates at the preset speed only; therefore, treat cable assemblies as custom applications, not general-purpose isolated cables.

POWER SUPPLY OPTIONS

In most USB transceivers, 3.3 V is derived from the 5 V USB bus through an LDO regulator. The ADuM4160 includes internal LDO regulators on both the upstream and downstream sides. The output of the LDO is available on the V_{DD1} and V_{DD2} pins. In some cases, especially on the peripheral side of the isolation, there may not be a 5 V power supply available. The ADuM4160 has the ability to bypass the regulator and run on a 3.3 V supply directly.

Two power pins are present on each side, V_{BUSx} and V_{DDx}. If 5 V is supplied to V_{BUSx}, an internal regulator creates 3.3 V to power the xD+ and xD− drivers. V_{DDx} provides external access to the 3.3 V supply to allow external bypass as well as bias for external pull-ups. If only 3.3 V is available, it can be supplied to both V_{BUSx} and V_{DDx}. This disables the regulator and powers the coupler directly from the 3.3 V supply.

Figure 5 shows how to configure a typical application when the upstream side of the coupler receives power directly from the USB bus and the downstream side is receiving 3.3 V from the peripheral power supply. The downstream side can run from a 5V V_{BUS2} power supply as well. It can be connected in the same manner as V_{BUS1} as shown in Figure 5, if needed.

PRINTED CIRCUIT BOARD LAYOUT (PCB)

The ADuM4160 digital isolator requires no external interface circuitry for the logic interfaces. For full speed operation, the D+ and D− line on each side of the device requires a 24 Ω ± 1% series termination resistor. These resistors are not required for low speed applications. Power supply bypassing is required at the input and output supply pins (Figure 5). Install bypass capacitors between V_{BUSx} and V_{DDx} on each side of the chip. The capacitor value should have a value of 0.1 μF and be of a low ESR type. The total lead length between both ends of the capacitor and the power supply pin should not exceed 10 mm. Bypassing between Pin 2 and Pin 8 and between Pin 9 and Pin 15 should also be considered, unless the ground pair on each package side is connected close to the package.

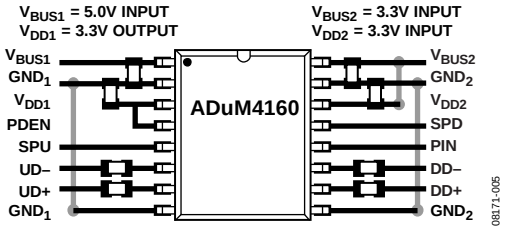

Figure 5. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than about 12 USB bit times, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 36 USB bit times, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM4160 is set by the condition in which induced voltage in the receiving

coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM4160 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\prod r_n^2; n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM4160 and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 6.

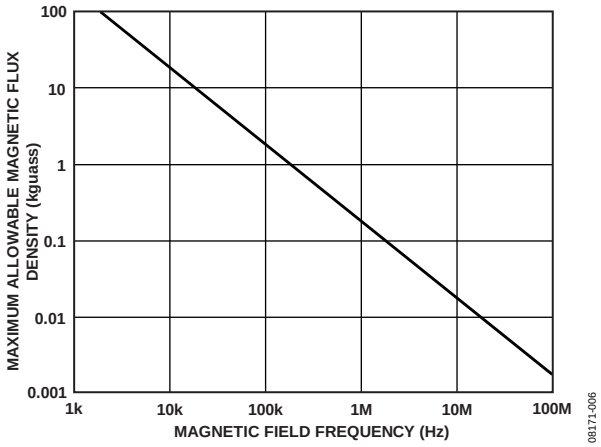

Figure 6. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM4160 transformers. Figure 7 expresses these allowable current magnitudes as a function of frequency for selected distances.

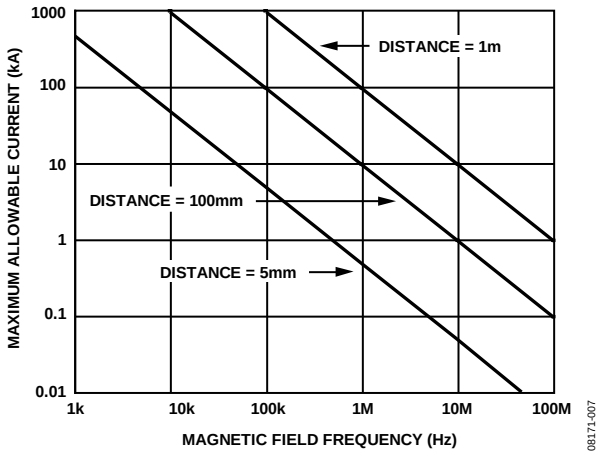

Figure 7. Maximum Allowable Current for Various Current-to-ADuM4160 Spacings

As shown, the ADuM4160 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current would need to be placed 5 mm away from the ADuM4160 to affect the operation of the component.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4160.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 8 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4160 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler

insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 8, Figure 9, and Figure 10 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages and still achieves a 50-year service life. The working voltages listed in Table 8 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Treat any cross insulation voltage waveform that does not conform to Figure 9 or Figure 10 as a bipolar ac waveform and limit its peak voltage to the 50-year lifetime voltage value listed in Table 8.

Note that the voltage presented in Figure 9 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

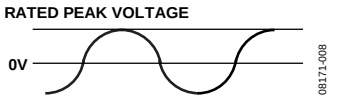

Figure 8. Bipolar AC Waveform

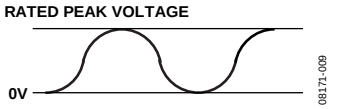

Figure 9. Unipolar AC Waveform

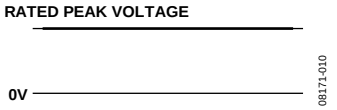

Figure 10. DC Waveform

OUTLINE DIMENSIONS

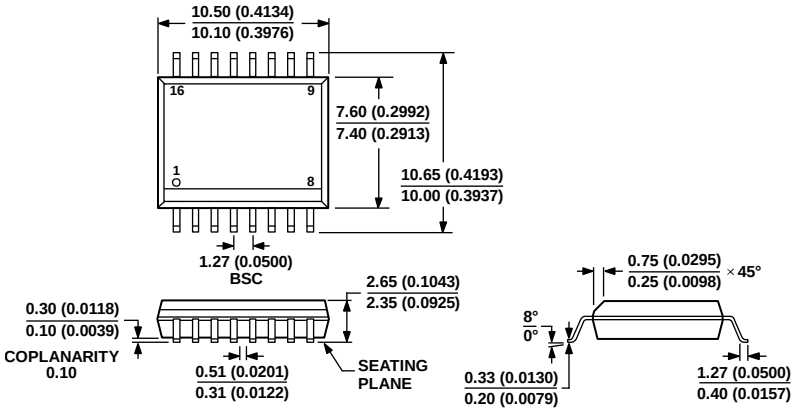

Figure 11. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimension shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Jitter (ns)	Temperature Range	Package Description	Package Option
ADuM4160BRWZ	2	2	12	70	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM4160BRWZ-RL	2	2	12	70	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
EVAL-ADUM4160EBZ							Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] For ADuM4160BRWZ and ADuM4160BRWZ-RL, specifications represent full speed buffer configuration.

NOTES

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