DIGITALVIEW®
visual communication specialists

LVDS Add On Board P/N 4162135-11

The LVDS add-on board P/N 4162135-11 design for dual pixel LVDS panels. It provides jumper setting to select the Data Enable (DE) signal on transmitter chips.

Jumper Settings :
JP1- Clock phase selection (Default 2-3 closed)
Change this setting to obtain best quality.

JP2 - Panel voltage selection
1-3, 2-4 closed : 12V panel
3-5, 4-6 closed : 3.3 / 5V panel (Default)

JP3 – Enable DE signal on signal or dual LVDS transmitter chip at even pixel side
1-2 closed : Enable DE signal on both LVDS transmitter chips (U1 & U2) (Default - Use for all panels)

2-3 closed : Enable DE signal on single LVDS transmitter chip (U1)
(Use for all panel except : NEC NL128102AC28-04 and NEC NL128102AC31-02A)

Compatible with LVDS board :

Old LVDS board	Jumper setting on LVDS board P/N 4162135-11
P/N 4162135-10	JP1 : 2-3 closed ; JP2 : 1-3, 2-4 closed ; JP3 : 1-2 closed
P/N 4162147-00	JP1 : 2-3 closed ; JP2 : 3-5, 4-6 closed ; JP3 : 1-2 closed

Use of connectors :

Connector	Connector type
CN2	Hirose DF11-28DS-2DSA
CN3	Hirose DF11-32DS-2DSA
CN4	Hirose DF11-20DF-2DSA
CN5	Hirose DF14-20P-1.25P
CN6	Hirose DF14-25P-1.25P

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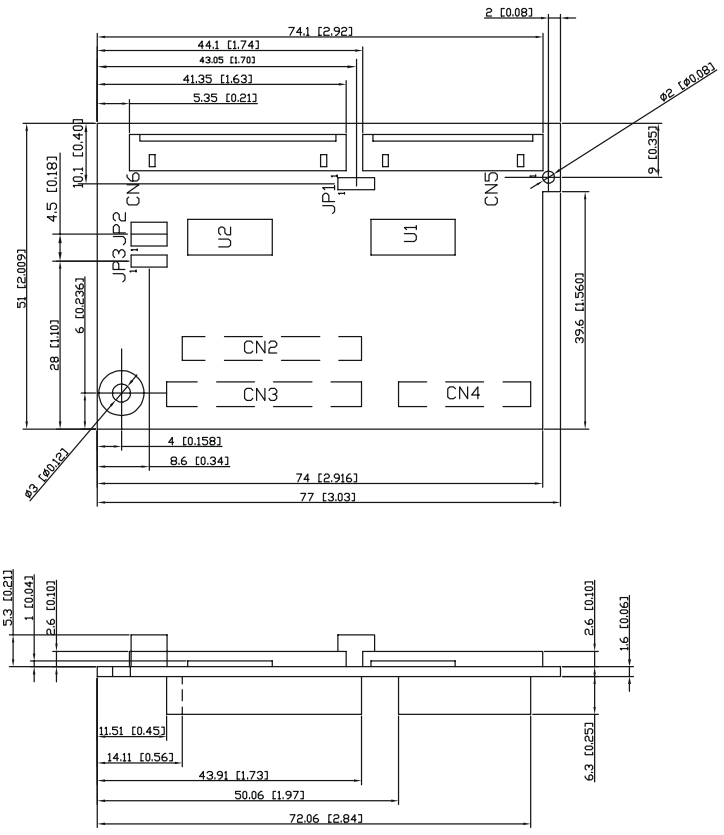
Mechanical Drawing :



All dimensions are in MM [Inch]

Pin Assignments :

CN5 - Hirose DF14-20P-1.25P

PIN	SYMBOL	DESCRIPTION
1	NC	No connection
2	GND	Ground
3	OUTO3	Positive differential LVDS data O3
4	/OUTO3	Negative differential LVDS data O3
5	GND	Ground
6	CLKOUTO	Positive LVDS clock O
7	/CLKOUTO	Negative LVDS clock O
8	GND	Ground
9	OUTO2	Positive differential LVDS data O2
10	/OUTO2	Negative differential LVDS data O2
11	GND	Ground
12	OUTO1	Positive differential LVDS data O1
13	/OUTO1	Negative differential LVDS data O1
14	GND	Ground
15	OUTO0	Positive differential LVDS data O0
16	/OUTO0	Negative differential LVDS data O0
17	GND	Ground
18	GND	Ground
19	VLCD	Panel power supply
20	VLCD	Panel power supply

CN6 DF14-25P-1.25P

PIN	SYMBOL	DESCRIPTION
1	VLCD	Panel power supply
2	VLCD	Panel power supply
3	VLCD	Panel power supply
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	OUTE3	Positive differential LVDS data E3
9	/OUTE3	Negative differential LVDS data E3
10	GND	Ground
11	CLKOUTE	Positive LVDS clock E
12	/CLKOUTE	Negative LVDS clock E
13	GND	Ground
14	OUTE2	Positive differential LVDS data E2
15	/OUTE2	Negative differential LVDS data E2
16	GND	Ground
17	/OUTE1	Negative differential LVDS data E1
18	OUTE1	Positive differential LVDS data E1
19	GND	Ground
20	OUTE0	Positive differential LVDS data E0
21	/OUTE0	Negative differential LVDS data E0
22	GND	Ground
23	GND	Ground
24	NC	No connection
25	NC	No connection

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