DDR SDRAM SODIMM

MT4VDDT1664H – 128MB
MT4VDDT3264H – 256MB

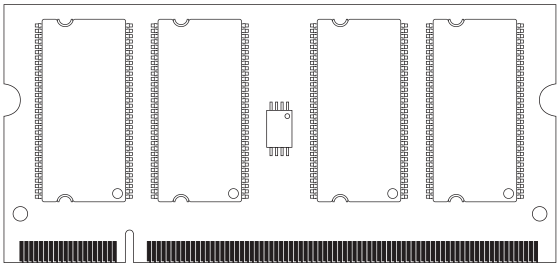
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 128MB (16 Meg x 64) or 256MB (32 Meg x 64)
- Vdd = Vddq = +2.5V (-40B: Vdd = Vddq = +2.6V)
- Vddspd = +2.3V to +3.6V
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) *2n*-prefetch architecture
- Bidirectional data strobe (DQS) transmitted/ received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Single rank
- Selectable burst lengths (BL): 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125µs maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts

Figure 1: 200-Pin SODIMM (MO-224)

PCB height: 31.75mm (1.25in)



Options — Marking

- Operating temperature[1]
  - Commercial (0°C ≤ T_A ≤ +70°C) — None
  - Industrial (–40°C ≤ T_A ≤ +85°C) — I
- Package
  - 200-pin DIMM (standard) — G
  - 200-pin DIMM (Pb-free) — Y
- Memory clock, speed, CAS latency
  - 5ns (200 MHz), 400 MT/s, CL = 3 — -40B
  - 6ns (167 MHz), 333 MT/s, CL = 2.5 — -335
  - 7.5ns (133 MHz), 266 MT/s, CL = 2[2] — -26A
  - 7.5ns (133 MHz), 266 MT/s, CL = 2.5[2] — -265

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^tRCD (ns)	^tRP (ns)	^tRC (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of ^tRCD and ^tRP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	128MB	256MB
Refresh count	8K	8K
Row address	8K (A0–A12)	8K (A0–A12)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	256Mb (16 Meg x 16)	512Mb (32 Meg x 16)
Column address	512 (A0–A8)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 128MB Modules

Base device: MT46V16M16,[1] 256Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Latency (CL-^{t}RCD-^{t}RP)
MT4VDDT1664HG-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT4VDDT1664HY-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT4VDDT1664HG-335__	128MB	16 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT1664HY-335__	128MB	16 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT1664HG-26A__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT4VDDT1664HG-265__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT4VDDT1664HY-265__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Table 4: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT46V32M16,[1] 512Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Latency (CL-^{t}RCD-^{t}RP)
MT4VDDT3264HG-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT4VDDT3264HY-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT4VDDT3264HG-335__	256MB	32 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT3264HY-335__	256MB	32 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT4VDDT3264HG-265__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes:
1. The data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT4VDDT3264HY-40BF2.

Pin Assignments and Descriptions

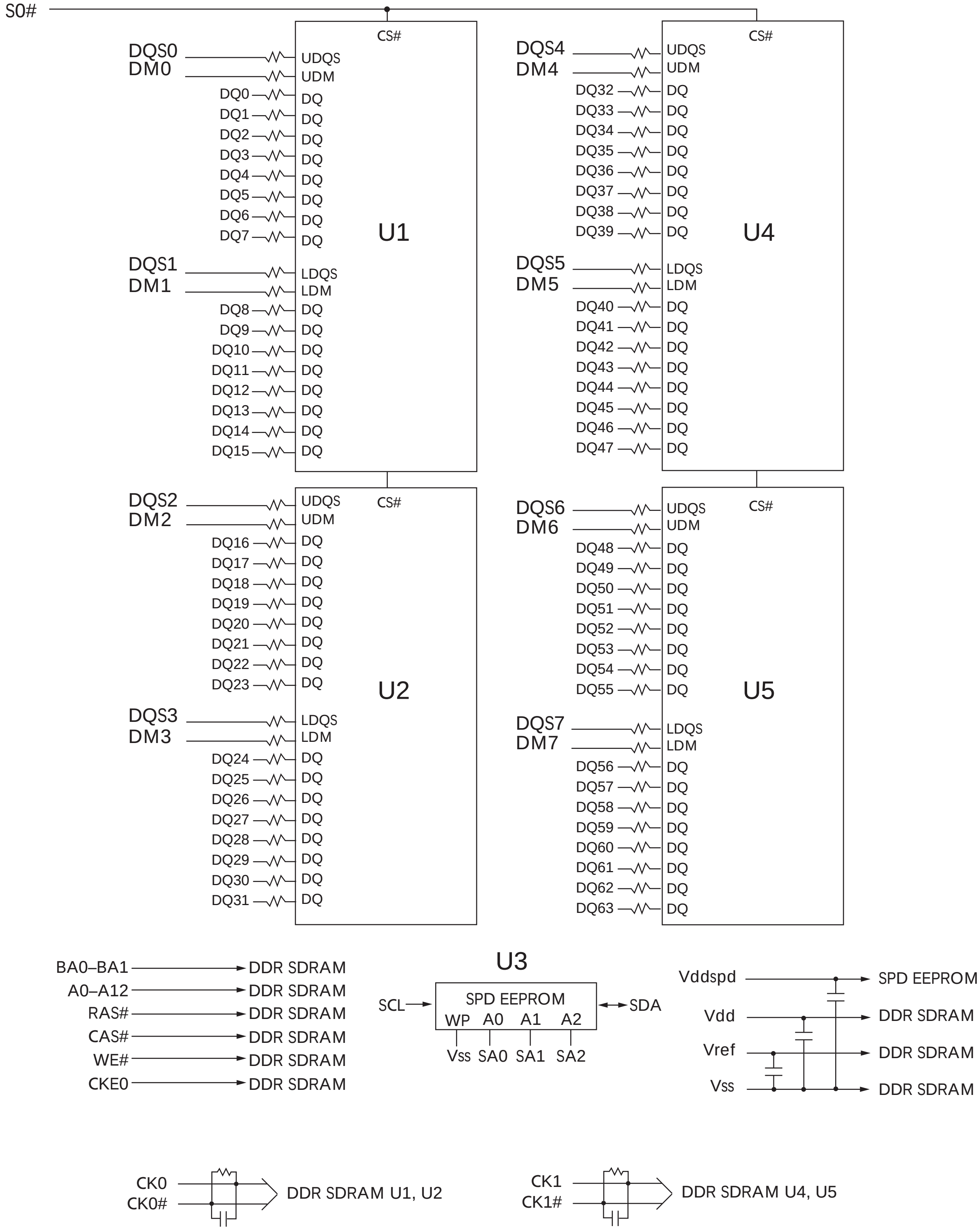
Table 5: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	Vref	51	Vss	101	A9	151	DQ42	2	Vref	52	Vss	102	A8	152	DQ46
3	Vss	53	DQ19	103	Vss	153	DQ43	4	Vss	54	DQ23	104	Vss	154	DQ47
5	DQ0	55	DQ24	105	A7	155	Vdd	6	DQ4	56	DQ28	106	A6	156	Vdd
7	DQ1	57	Vdd	107	A5	157	Vdd	8	DQ5	58	Vdd	108	A4	158	CK1#
9	Vdd	59	DQ25	109	A3	159	Vss	10	Vdd	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	Vss	12	DM0	62	DM3	112	A0	162	Vss
13	DQ2	63	Vss	113	Vdd	163	DQ48	14	DQ6	64	Vss	114	Vdd	164	DQ52
15	Vss	65	DQ26	115	A10	165	DQ49	16	Vss	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	Vdd	18	DQ7	68	DQ31	118	RAS#	168	Vdd
19	DQ8	69	Vdd	119	WE#	169	DQS6	20	DQ12	70	Vdd	120	CAS#	170	DM6
21	Vdd	71	DNU	121	S0#	171	DQ50	22	Vdd	72	DNU	122	NC	172	DQ54
23	DQ9	73	DNU	123	NC	173	Vss	24	DQ13	74	DNU	124	NC	174	Vss
25	DQS1	75	Vss	125	Vss	175	DQ51	26	DM1	76	Vss	126	Vss	176	DQ55
27	Vss	77	DNU	127	DQ32	177	DQ56	28	Vss	78	DNU	128	DQ36	178	DQ60
29	DQ10	79	DNU	129	DQ33	179	Vdd	30	DQ14	80	DNU	130	DQ37	180	Vdd
31	DQ11	81	Vdd	131	Vdd	181	DQ57	32	DQ15	82	Vdd	132	Vdd	182	DQ61
33	Vdd	83	DNU	133	DQS4	183	DQS7	34	Vdd	84	DNU	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	Vss	36	Vdd	86	NC	136	DQ38	186	Vss
37	CK0#	87	Vss	137	Vss	187	DQ58	38	Vss	88	Vss	138	Vss	188	DQ62
39	Vss	89	DNU	139	DQ35	189	DQ59	40	Vss	90	Vss	140	DQ39	190	DQ63
41	DQ16	91	DNU	141	DQ40	191	Vdd	42	DQ20	92	Vdd	142	DQ44	192	Vdd
43	DQ17	93	Vdd	143	Vdd	193	SDA	44	DQ21	94	Vdd	144	Vdd	194	SA0
45	Vdd	95	NC	145	DQ41	195	SCL	46	Vdd	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	Vddspd	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	Vss	199	NC	50	DQ22	100	A11	150	Vss	200	NC

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0 and BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
BA0, BA1	Input	**Bank address:** BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK0, CK0#, CK1, CK1#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and CKE disables (registered LOW) the internal clock, input buffers, and output drivers.
DM0–DM7	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#	Input	**Chip selects:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	I/O	**Data input/output:** Data bus.
DQS0–DQS7	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
Vdd	Supply	**Power supply:** +2.5V ±0.2V (-40B: +2.6V ±0.1V).
Vddspd	Supply	**SPD EEPROM power supply:** +2.3V to +3.6V.
Vref	Supply	SSTL_2 reference voltage (Vdd/2).
Vss	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Figure 2: Functional Block Diagram



General Description

The MT4VDDT1664H and MT4VDDT3264H are high-speed, CMOS dynamic random access 128MB and 256MB memory modules organized in a x64 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various DDR SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is connected to Vss, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum DC Ratings

Symbol	Parameter		Min	Max	Units
Vdd	Vdd supply voltage relative to Vss		–1	+3.6	V
Vin, Vout	Voltage on any pin relative to Vss		–0.5	+3.2	V
Ii	Input leakage current; Any input 0V ≤ Vin ≤ Vdd; Vref input 0V ≤ Vin ≤ 1.35V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE	–8	+8	µA
		CK, CK#	–4	+4	
		DM	–2	+2	
Ioz	Output leakage current; 0V ≤ Vout ≤ Vddq; DQ and ODT are disabled	DQ, DQS	–5	+5	µA
T_A	DRAM ambient operating temperature[1]	Commercial	0	+70	°C
		Industrial	–40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades
DDR components may exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5B
-335	-6
-26A	-75Z
-265	-75

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

Idd Specifications

Table 9: Idd Specifications and Conditions – 128MB (Die Revision K)
Values are for the MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		Idd0	400	360	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Iout= 0mA; Address and control inputs changing once per clock cycle		Idd1	480	460	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = (LOW)		Idd2P	16	16	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DM, and DQS		Idd2F	200	200	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		Idd3P	140	120	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		Idd3N	240	220	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); Iout = 0mA		Idd4R	720	640	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		Idd4W	720	640	mA
Auto refresh current	$^tRFC = {}^tRFC$ (MIN)	Idd5	640	640	mA
	$^tRFC = 7.8125\mu s$	Idd5A	24	24	mA
Self refresh current: CKE $\leq$ 0.2V		Idd6	16	16	mA
Operating bank interleave read current: Four device bank interleaving (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		Idd7	1160	1080	mA

Table 10: Idd Specifications and Conditions – 128MB (All Other Die Revisions)
Values are for the MT46V16M16 DDR SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	-26A/ -265	Units
Operating one bank active-precharge current: $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		Idd0	540	500	480	mA
Operating one bank active-read-precharge current: BL = 4; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Iout= 0mA; Address and control inputs changing once per clock cycle		Idd1	740	720	620	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = (LOW)		Idd2P	16	16	16	mA
Idle standby current: CS# = HIGH; All device banks idle; $^{t}CK = {}^{t}CK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DM, and DQS		Idd2F	240	200	180	mA
Active power-down standby current: One device bank active; Power-down mode; $^{t}CK = {}^{t}CK$ (MIN); CKE = LOW		Idd3P	160	120	100/ 120	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank; $^{t}RC = {}^{t}RAS$ (MAX); $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		Idd3N	280	240	200	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA		Idd4R	1040	880	740	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^{t}CK = {}^{t}CK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		Idd4W	860	780	640	mA
Auto refresh current	$^{t}RFC = {}^{t}RFC$ (MIN)	Idd5	1040	1020	940/ 980	mA
	$^{t}RFC = 7.8125\mu s$	Idd5A	24	24	24	mA
Self refresh current: CKE $\leq$ 0.2V		Idd6	16	16	16	mA
Operating bank interleave read current: Four device bank interleaving (BL = 4) with auto precharge; $^{t}RC = {}^{t}RC$ (MIN); $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs change only during active READ or WRITE commands		Idd7	2046	1760	1520/ 1600	mA

Table 11: Idd Specifications and Conditions – 256MB
Values are for the MT46V32M16 DDR SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

Parameter/Condition		Symbol	-40B	-335	-265	Units
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		Idd0	620	520	460	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Iout= 0mA; Address and control inputs changing once per clock cycle		Idd1	780	640	580	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = (LOW)		Idd2P	20	20	20	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DM, and DQS		Idd2F	220	180	160	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		Idd3P	180	140	120	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		Idd3N	240	200	180	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); Iout = 0mA		Idd4R	840	660	580	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		Idd4W	860	780	540	mA
Auto refresh current	$^tRFC = {}^tRFC$ (MIN)	Idd5	1380	1160	1120	mA
	$^tRFC = 7.8125\mu s$	Idd5A	44	40	40	mA
Self refresh current: CKE $\leq$ 0.2V		Idd6	24	20	20	mA
Operating bank interleave read current: Four device bank interleaving (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		Idd7	1920	1620	1400	mA

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	Vddspd	2.3	3.6	V
Input high voltage: Logic 1; All inputs	Vih	Vddspd × 0.7	Vddspd + 0.5	V
Input low voltage: Logic 0; All inputs	Vil	–1.0	Vddspd × 0.3	V
Output low voltage: Iout = 3mA	Vol	–	0.4	V
Input leakage current: Vin = GND to Vdd	Ili	–	10	µA
Output leakage current: Vout = GND to Vdd	Ilo	–	10	µA
Standby current: SCL = SDA = Vdd - 0.3V; All other inputs = Vss or Vdd	Isb	–	30	µA
Power supply current: SCL clock frequency = 100 kHz	Icc	–	2.0	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}HD:DAT	200	–	ns	
SDA fall time	^{t}F	–	300	ns	2
SDA rise time	^{t}R	–	300	ns	2
Data-in hold time	^{t}HD:DI	0	–	µs	
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	5	ms	4

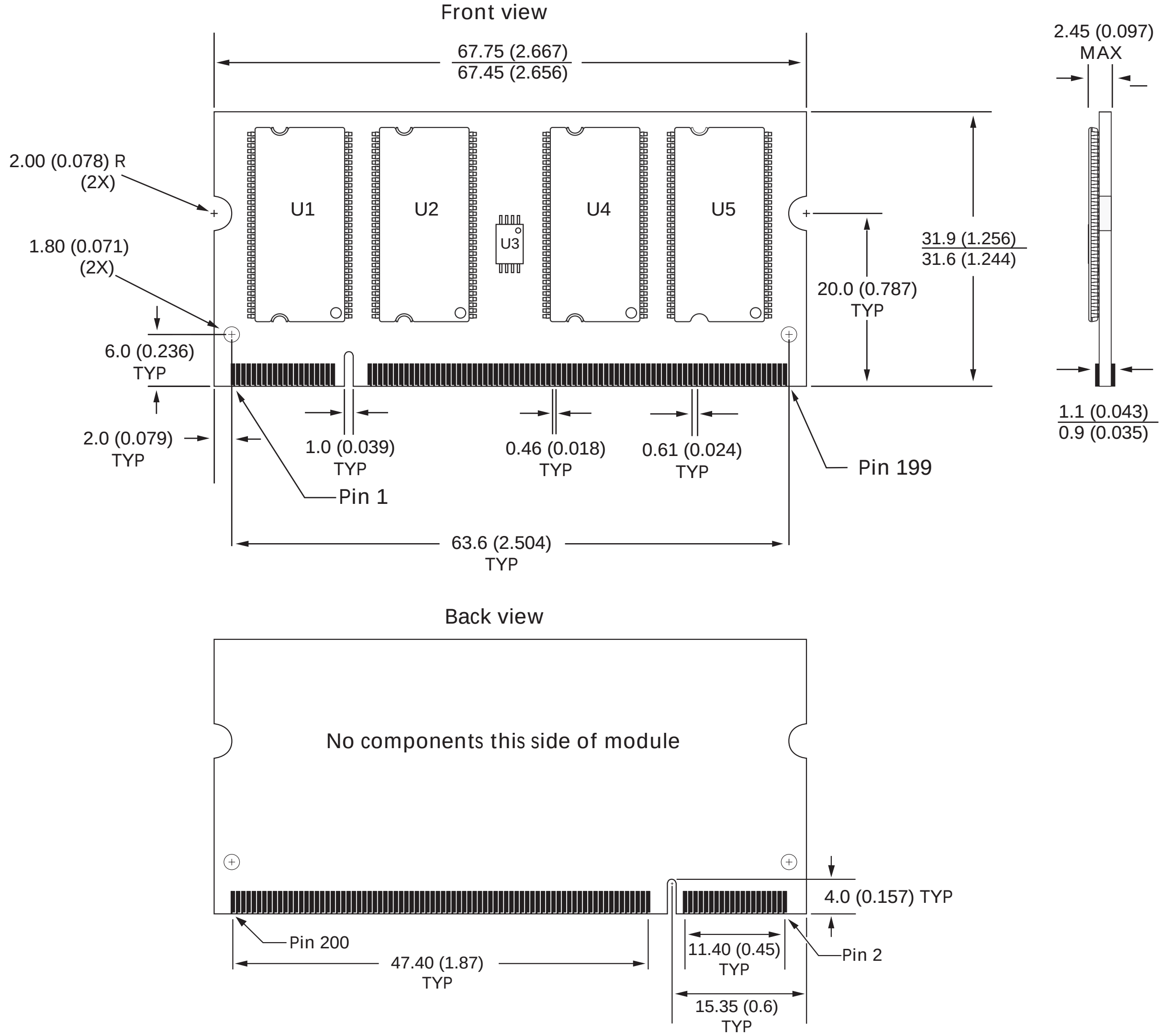
Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 3: 200-Pin SODIMM



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.