DDR2 SDRAM FBDIMM

MT36HTS51272F – 4GB

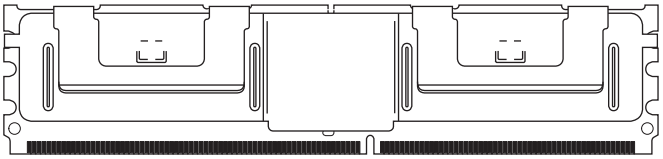
For the latest data sheet, refer to Micron's Web site: www.micron.com

Features

- 240-pin DDR2 fully buffered, dual in-line memory module (FBDIMM) with ECC to detect and report channel errors to the host memory controller
- Fast data transfer rates: PC2-4200 and PC2-5300 using 533 MT/s and 667 MT/s DDR2 SDRAM components
- 3.2 Gb/s and 4.0 Gb/s link transfer rates
- High-speed, differential, point-to-point link between host memory controller and the AMB using serial, dual-simplex bit lanes
  - 10-pair southbound (data path to FBDIMM)
  - 14-pair northbound (data path from FBDIMM)
- Fault tolerant; can work around a bad bit lane in each direction
- High-density scaling with up to 8 dual-rank modules (288 DDR2 SDRAM devices) per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
  - Enables memory controller to optimize DRAM accesses for maximum performance
  - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI
- MBIST and IBIST test functions
- Transparent mode for DDR2 SDRAM test support
- V_{DD} = $V_{DD}Q$ = +1.8V for DDR2 SDRAM
- V_{REF} = 0 .9V SDRAM C/A termination
- V_{CC} = 1.5V for advanced memory buffer (AMB)
- V_{DDSPD} = +1.7V to +3.6V for SPD EEPROM
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank
- Supports 95°C operation with 2X refresh (^{t}REFI = 7.8µs at or below 85°C; ^{t}REFI = 3.9µs above 85°C)

Figure 1: 240-Pin FBDIMM (MO-256 R/C J)

PCB height: 30.35mm (1.19in)



Options	Marking
• Package	
– 240-pin FBDIMM (lead-free)	Y
• Frequency/CL[1]	
– 3.75ns @ CL = 5 (DDR2-667)	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
• PCB height	
– 30.35mm (1.19in)	

Notes: 1. CL = CAS (READ) latency.

Table 1: FBDIMM/DDR2 SDRAM Addressing

Parameter	4GB
Refresh count	8K
Device bank addressing	8 (BA0, BA1, BA2)
Device page size per bank	1KB
Device configuration	TwinDie™ 1Gb (256 Meg x 4)
Row addressing	16K (A0–A13)
Column addressing	2K (A0–A9, A11)
Module rank addressing	2 (S0#, S1#)

Table 2: Performance Parameters

Speed Grade	Module Bandwidth	Peak Channel Throughput	Link Transfer Rate	Latency (CL-^{t}RCD-^{t}RP)
-667	PC2-5300	8.0 GB/s	4.0 GT/s	5-5-5
-53E	PC2-4200	6.4 GB/s	3.2 GT/s	4-4-4

Table 3: Part Numbers and Label Markings

Part Number[1]	Module Density	FBDIMM Configuration	Label Key Attributes
MT36HTS51272FY-53E__	4GB	256 Meg x 72	4GB 2Rx4 PC2-4200J-444-10-C_
MT36HTS51272FY-667__	4GB	256 Meg x 72	4GB 2Rx4 PC2-5300J-555-10-C_

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT36HTS51272FY-53EC2.

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Introduction

FBDIMM Specification Details

The JEDEC FBDIMM specification consists of the following sections and can be found at the JEDEC Web site member's area.

Each of these sections contains detailed information about the various aspects of FBDIMM construction, interfaces, and theory of operation. The JEDEC specification is simply too long and complex to condense into a single data sheet; minimal references are made throughout this document to give a brief overview. For design guidance and final specification information, designers must refer to the JEDEC FBDIMM specification.

1. **FBDIMM Design Specification**
   Defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300, 72-bit wide, fully buffered double data rate synchronous DRAM dual in-line memory modules (DDR2 SDRAM FBDIMMs). These DDR2 SDRAM FBDIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300 refers to the DIMM naming convention in which PC2-4200/PC2-5300 indicates a 240-pin DDR2 DIMM running at 266/333 MHz DDR2 SDRAM clock speed and offering 4.2/5.3 GB/s bandwidth.

   Reference design examples are included which provide an initial basis for FBDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/ support. All FBDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

2. **FBDIMM Architecture and Protocol Specification**
   Describes FBDIMM channel topology, physical signaling, clocking, and data flow.

3. **FBDIMM AMB Specification**
   Core specification for a FBDIMM memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to an AMB design appears in the other specifications, with specific cross-references provided.

4. **FBDIMM Link Signaling Specification**
   Defines the high-speed, differential, point-to-point signaling link for FBDIMM, operating at AMB V_{CC} = 1.5V, provided at the FBDIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter, a receiver, and the interconnect between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first-generation FBDIMM link is specified for 3.2–4.0 Gb/s and defined for three distinct bit rates: 3.2 Gb/s and 4.0 Gb/s.

   The link utilizes a derived-clock approach and transmitter de-emphasis to compensate for channel loss characteristics. The link definition has the flexibility to accommodate future silicon enhancement circuits, such as forwarded clocking or advanced equalization techniques, to meet future signaling targets.

5. **FBDIMM DFx Specification**
   Defines design for test, design for manufacturing, and design for validation (DFx) requirements and implementation guidelines for FBDIMM technology.

6. **FBDIMM SPD Specification**
   This section describes the serial presence-detect (SPD) values for FBDIMMs, referenced in the SPD "Specific Features" standard document. The SPD fields indicated in this specification will occur in the order presented in section 1.1 of the JEDEC document. *(Note that the descriptions of bytes 0 and 1 differ from those in previous SPD standards.)* Further description of byte 2 is found in Appendix A of the JEDEC FBDIMM SPD standard. All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0, except where noted.

General Description

The Micron FBDIMM adheres to the currently proposed industry specifications for FBDIMMs. This data sheet represents a minimal subset of the FBDIMM and AMB specification details and will be revised further as the specification matures and is approved and released. This document is to be used only as an introduction to the industry specification, which will serve as the final reference for any an all design parameters and criteria.

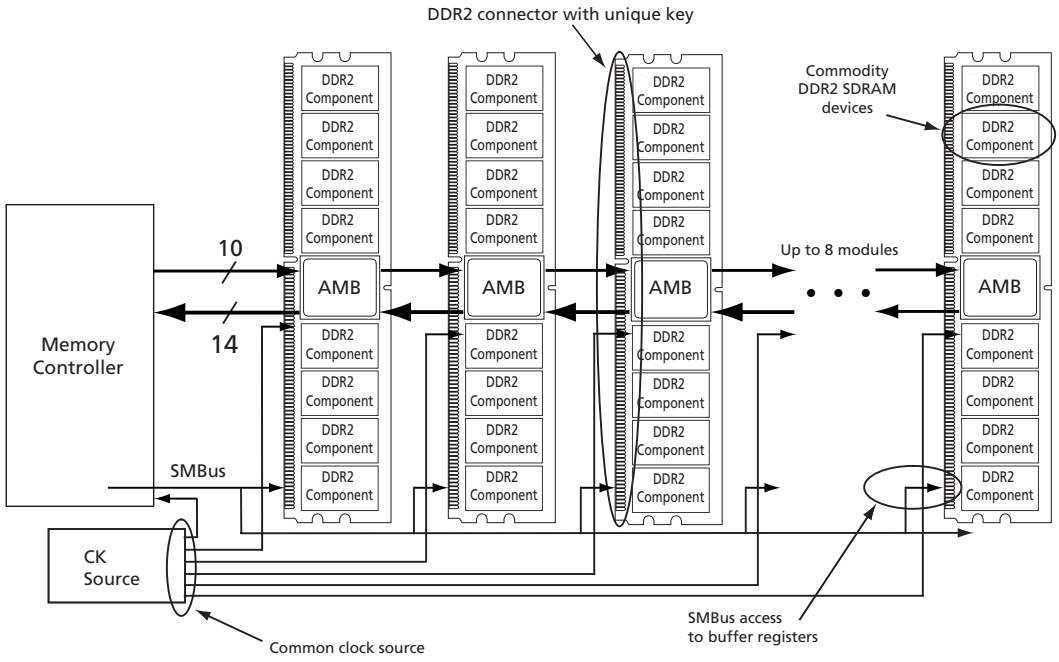
Micron's FBDIMM is a high-bandwidth, large-capacity-channel solution that has a narrow host interface. FBDIMMs use DDR2 SDRAM devices isolated from the channel behind a buffer on the FBDIMM. Memory-device capacity remains high and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 2 on page 8, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase reliability and availability of the memory subsystem.

Micron's FBDIMM features a novel architecture, including the AMB that isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, point-to-point interface at 1.5V.

The AMB also allows buffering of memory traffic to support large memory capacities. All memory control for the DDR2 SDRAM devices resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The AMB interface is responsible for handling channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the memory channel.

Figure 2: FBDIMM System Block Diagram



Functional Description

Advanced Memory Buffer (AMB)

The AMB reference design complies with the JEDEC standard, "FBDIMM Architecture and Protocol Specification." It is expected that there will be AMB multiple vendors, which will offer at least the minimum functionality set forth in the industry specification. To achieve optimal operation and compatibility with DDR2 SDRAM device and host/controller offerings, each vendor's AMB will have a unique set of personality bytes contained in the SPD for setting up and fine tuning that device.

The FBDIMM specification defines a number of options to support the requirements of different applications. The capabilities of the AMB are communicated to the host during the initialization process in the TS2 training pattern and in bits readable in the features register in the AMB.

The AMB is responsible for handling FBDIMM channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the channel. A complete and detailed description of the AMB is contained in the proposed FBDIMM AMB Specification. The AMB is a memory interface that connects an array of DDR2 SDRAM devices to the FBDIMM channel. The AMB is a slave device on the channel responding to channel commands and forwarding channel commands to other AMB devices.

All memory control for the DDR2 SDRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management.

The AMB is expected to perform the following functions:

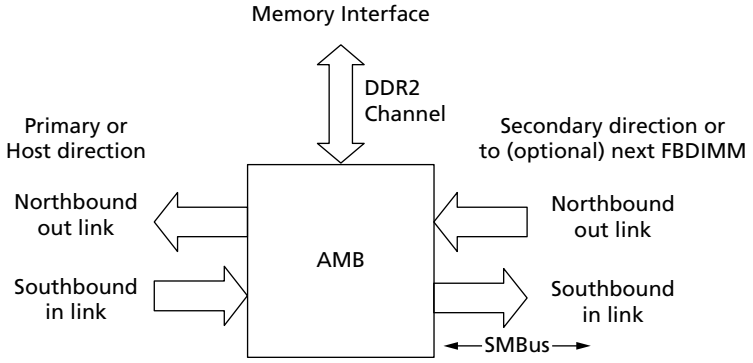
- Support channel initialization procedures as defined in the initialization chapter of the FBDIMM Architecture and Protocol Specification to align the clocks and the frame boundaries and verify channel connectivity
- Support the forwarding of southbound and northbound frames, servicing requests directed to a specific FBDIMM's AMB, as defined in the protocol chapter of the specification, and merging the return data into the northbound frames
- Initialize northbound frames if the FBDIMM's AMB is the last, southern-most frame on the channel
- Detect errors on the channel and report them to the host memory controller
- Support the FBDIMM configuration register set as defined in the FBDIMM AMB specification register chapter of the specification
- Act as a DRAM memory buffer for all read, write, and configuration accesses addressed to a specific FBDIMM's AMB
- Provide a read and write buffer FIFO
- Support an SMBus protocol interface for access to the AMB configuration registers
- Provide features to support MEMBIST and IBIST test functions
- Provide a register interface for the thermal sensor and status indicator
- Function as a repeater to extend the maximum length of FBDIMM Links
- Reconfigure FBDIMM inputs from differential high-speed link receivers to two single-ended, low-speed receivers (~200 MHz). These inputs directly control DDR2 command/address and input data that replicates to all DDR2 SDRAM devices.
- Bypass high speed parallel/serial circuitry and provide test results back to the tester, using low-speed FBDIMM outputs.

AMB Interface

Figure 3 illustrates the AMB and all of its interfaces. They consist of two FBDIMM links, one DDR2 channel, and an SMBus interface. Each FBDIMM link connects the AMB to a host memory controller or an adjacent FBDIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on an FBDIMM.

The FBDIMM channel uses a daisy-chain topology to provide expansion from a single FBDIMM per channel to up to eight FBDIMMs per channel. The host sends data on the southbound link to the first FBDIMM, where it is received and redriven to the second FBDIMM. On the southbound data path, each FBDIMM receives the data and redrives the data to the next FBDIMM, until the last FBDIMM receives the data. The last FBDIMM in the chain initiates the transmission of northbound data in the direction of the host. On the northbound data path, each FBDIMM receives the data and redrives the data to the next FBDIMM until the host is reached.

Figure 3: AMB Interface Block Diagram



High-Speed, Differential, Point-to-Point Link Interfaces (1.5V)

The AMB supports one FBDIMM channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide. It carries commands and write data from the host memory controller, or the adjacent FBDIMM in the host direction, to the next FBDIMM in the chain.

The northbound input link is 14 lanes wide. It carries read return data or status information from one FBDIMM to the next in the host direction and multiplexes in any internally generated READ return data or status information.

Data and commands sent to the DDR2 SDRAM devices travel southbound on 10 primary differential signal line pairs. Data and status information received from the DDR2 SDRAM devices travel northbound on 14 primary differential pairs. Data and commands sent to the upstream adjacent FBDIMM are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the upstream adjacent FBDIMM travel further northbound on 14 secondary differential pairs.

DDR2 Channel

The AMB DDR2 channel supports direct connection to DDR2 SDRAM devices. The DDR2 channel supports two ranks of eight banks with 16 row/column-request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support FBDIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays can differ between read data/check-bit strobe lanes on a given channel. Each strobe can be calibrated by hardware-state machines using WRITE/READ trial and error. Hardware aligns the read data and check-bits to a single core clock. The AMB provides four copies of the command clock phase references (CK[3:0]) and write data/check-bit strobes (DQS) for each DDR2 SDRAM device nibble.

SMBus Slave Interface

AMB support for an SMBus interface allows system access to configuration registers independent of the FBDIMM link. The AMB will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 KHz. SMBus access to the AMB may be a requirement to boot and to set link strength, frequency, and other parameters needed to ensure robust configurations. It is also required for diagnostic support when the high-speed link is down. The SMBus address straps located on the FBDIMM connector are used to set the unique ID.

Channel Latency

FBDIMM channel latency is measured from the time a read request is driven on the FBDIMM channel pins to the time when the first 16 bytes (second chunk) of read completion data is sampled by the memory controller.

When not using variable READ latency, the latency for a specific FBDIMM on a channel is always equal to the latency for any other FBDIMM on that channel. However, the latency for each FBDIMM in a specific configuration with some number of FBDIMMs installed may not be equal to the latency for each FBDIMM in a configuration with some different number of FBDIMMs installed. As more FBDIMMs are added to the channel, additional latency is required to read from each FBDIMM on the channel.

Because the channel is based on point-to-point interconnection of buffer components between FBDIMMs, memory requests are required to travel through N - 1 buffers before reaching the Nth buffer. The result is that a four-FBDIMM channel configuration will have greater idle READ latency than a one-FBDIMM channel configuration.

The variable READ latency capability can be used to reduce latency for FBDIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

Peak Theoretical Throughput

An FBDIMM channel transfers read completion data on the northbound data connection; 144 bits of data are transferred for every northbound data frame. This matches the 18-byte data transfer of an ECC DDR2 SDRAM device in a single DDR2 SDRAM command clock. A DDR2 SDRAM device burst of eight from a single channel, or burst of four from two lock-step channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). The AMB frame rate matches the DDR2 SDRAM command clock because of the fixed 6:1 ratio of the FBDIMM channel clock to the DDR2 SDRAM command clock.

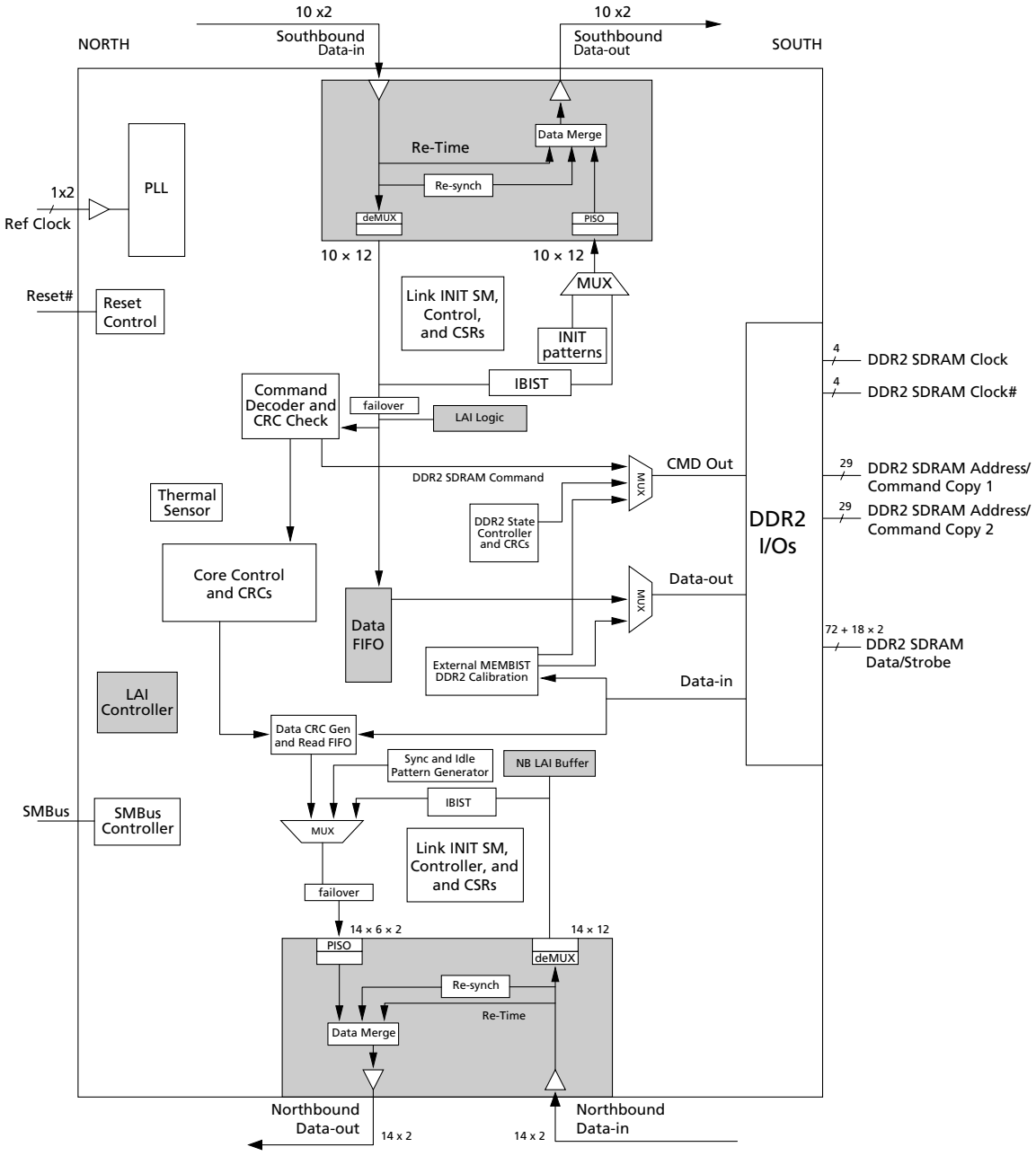
Therefore, the northbound data connection will exhibit the same peak theoretical throughput as a single DDR2 SDRAM channel. For example, when using DDR2-533 components, the peak theoretical bandwidth of the northbound data connection is 4.267 GB/s.

Write data is transferred on the southbound command and data connection, via Command + Wdata frames; 72 bits of data are transferred per frame. Two Command + Wdata frames match the 18-byte data transfer of an ECC DDR2 SDRAM in a single DDR2 SDRAM command clock.

A DDR2 SDRAM burst of eight transfers from a single channel, or a burst of four from two lock-step channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). When the FBDIMM frame rate matches the DDR2 SDRAM command clock, the southbound command and data connection will exhibit one-half the peak theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2-533 SDRAMs, the peak theoretical bandwidth of the southbound command and data connection is 2.133 GB/s.

The total peak theoretical throughput for a single FBDIMM channel is defined as the sum of the peak theoretical throughput of the northbound data connection and the southbound command and data connection. When the FBDIMM frame rate matches the DDR2 SDRAM command clock, it equals 1.5X the peak theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2-533 SDRAM devices, the peak theoretical throughput of a DDR2-533 channel would be 4.267 GB/s, while the peak theoretical throughput of an FBDIMM-533 channel would be 6.4 GB/s.

Figure 4: AMB Functional Block Diagram



Hot-Add

The FBDIMM channel does not provide a mechanism to automatically detect and report the addition of a new FBDIMM south of the currently active last FBDIMM. It is assumed the system will be notified through some means of the addition of one or more new FBDIMMs so that specific commands can be sent to the host controller to initialize the newly added FBDIMM(s) and perform a hot-add reset to bring them into the channel timing domain. It should be noted that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-Remove

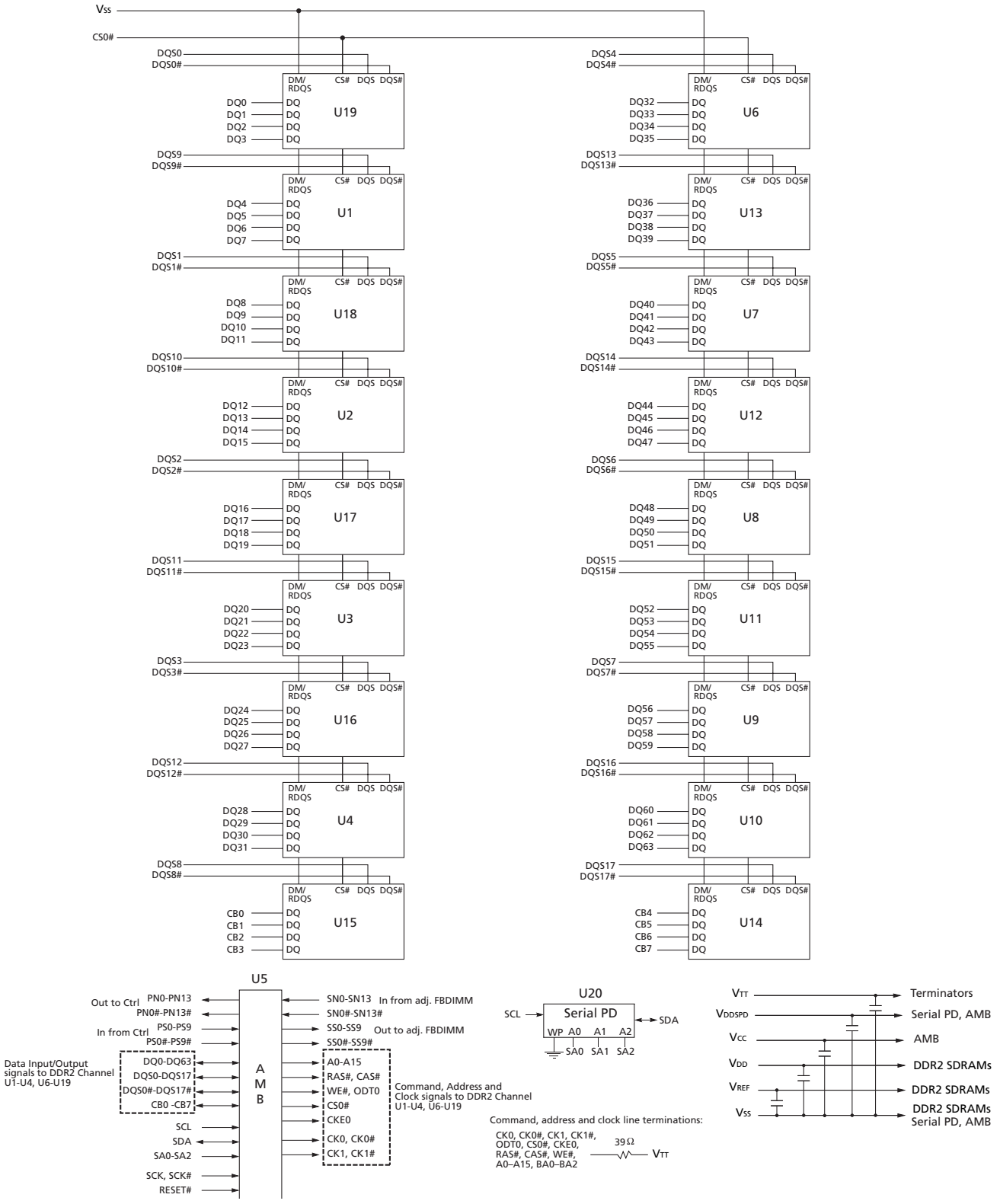
To remove one or more FBDIMMs, the host must perform a fast reset sequence targeted at the last FBDIMM that will be retained on the channel. The fast reset re-establishes the appropriate last FBDIMM so that the southbound transmission outputs of the last active FBDIMM and the southbound and northbound outputs of the FBDIMMs beyond the last active FBDIMM are disabled. Once the appropriate outputs are disabled, the system can coordinate the procedure to remove power in preparation for physical removal of the FBDIMM. Note that the power to the FBDIMM socket must be removed before a hot-remove FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-Replace

Hot-replace of FBDIMMs is accomplished by combining the hot-remove and hot-add processes.

FBDIMM Functional Block

Figure 5: FBDIMM Functional Block Diagram



Pin Assignments and Descriptions

Table 4: 240-pin FBDIMM Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VDD	121	VDD	31	PN3	151	SN3	61	PN9#	181	SN9#	91	PS9#	211	SS9#
2	VDD	122	VDD	32	PN3#	152	SN3#	62	VSS	182	VSS	92	VSS	212	VSS
3	VDD	123	VDD	33	VSS	153	VSS	63	PN10	183	SN10	93	PS5	213	SS5
4	VSS	124	VSS	34	PN4	154	SN4	64	PN10#	184	SN10#	94	PS5#	214	SS5#
5	VDD	125	VDD	35	PN4#	155	SN4#	65	VSS	185	VSS	95	VSS	215	VSS
6	VDD	126	VDD	36	VSS	156	VSS	66	PN11	186	SN11	96	PS6	216	SS6
7	VDD	127	VDD	37	PN5	157	SN5	67	PN11#	187	SN11#	97	PS6#	217	SS6#
8	VSS	128	VSS	38	PN5#	158	SN5#	68	VSS	188	VSS	98	VSS	218	VSS
9	VCC	129	VCC	39	VSS	159	VSS	69	VSS	189	VSS	99	PS7	219	SS7
10	VCC	130	VCC	40	PN13	160	SN13	70	PS0	190	SS0	100	PS7#	220	SS7#
11	VSS	131	VSS	41	PN13#	161	SN13#	71	PS0#	191	SS0#	101	VSS	221	VSS
12	VCC	132	VCC	42	VSS	162	VSS	72	VSS	192	VSS	102	PS8	222	SS8
13	VCC	133	VCC	43	VSS	163	VSS	73	PS1	193	SS1	103	PS8#	223	SS8#
14	VSS	134	VSS	44	RFU	164	RFU[1]	74	PS1#	194	SS1#	104	VSS	224	VSS
15	VTT	135	VTT	45	RFU	165	RFU[1]	75	VSS	195	VSS	105	RFU[2]	225	RFU[2]
16	VID1	136	VID0	46	VSS	166	VSS	76	PS2	196	SS2	106	RFU[2]	226	RFU[2]
17	RESET#	137	DNU/M_Test	47	VSS	167	VSS	77	PS2#	197	SS2#	107	VSS	227	VSS
18	VSS	138	VSS	48	PN12	168	SN12	78	VSS	198	VSS	108	VDD	228	SCK
19	RFU[2]	139	RFU[2]	49	PN12#	169	SN12#	79	PS3	199	SS3	109	VDD	229	SCK#
20	RFU[2]	140	RFU[2]	50	VSS	170	VSS	80	PS3#	200	SS3#	110	VSS	230	VSS
21	VSS	141	VSS	51	PN6	171	SN6	81	VSS	201	VSS	111	VDD	231	VDD
22	PN0	142	SN0	52	PN6#	172	SN6#	82	PS4	202	SS4	112	VDD	232	VDD
23	PN0#	143	SN0#	53	VSS	173	VSS	83	PS4#	203	SS4#	113	VDD	233	VDD
24	VSS	144	VSS	54	PN7	174	SN7	84	VSS	204	VSS	114	VSS	234	VSS
25	PN1	145	SN1	55	PN7#	175	SN7#	85	VSS	205	VSS	115	VDD	235	VDD
26	PN1#	146	SN1#	56	VSS	176	VSS	86	RFU[1]	206	RFU[1]	116	VDD	236	VDD
27	VSS	147	VSS	57	PN8	177	SN8	87	RFU[1]	207	RFU[1]	117	VTT	237	VTT
28	PN2	148	SN2	58	PN8#	178	SN8#	88	VSS	208	VSS	118	SA2	238	VDDSPD
29	PN2#	149	SN2#	59	VSS	179	VSS	89	VSS	209	VSS	119	SDA	239	SA0
30	VSS	150	VSS	60	PN9	180	SN9	90	PS9	210	SS9	120	SCL	240	SA1

Notes:
1. Reserved for forwarded clocks to be used in future module implementations.
2. Reserved for future architecture flexibility.
3. The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#.
4. RFU = reserved for future use.

Figure 6: FBDIMM Pin Locations

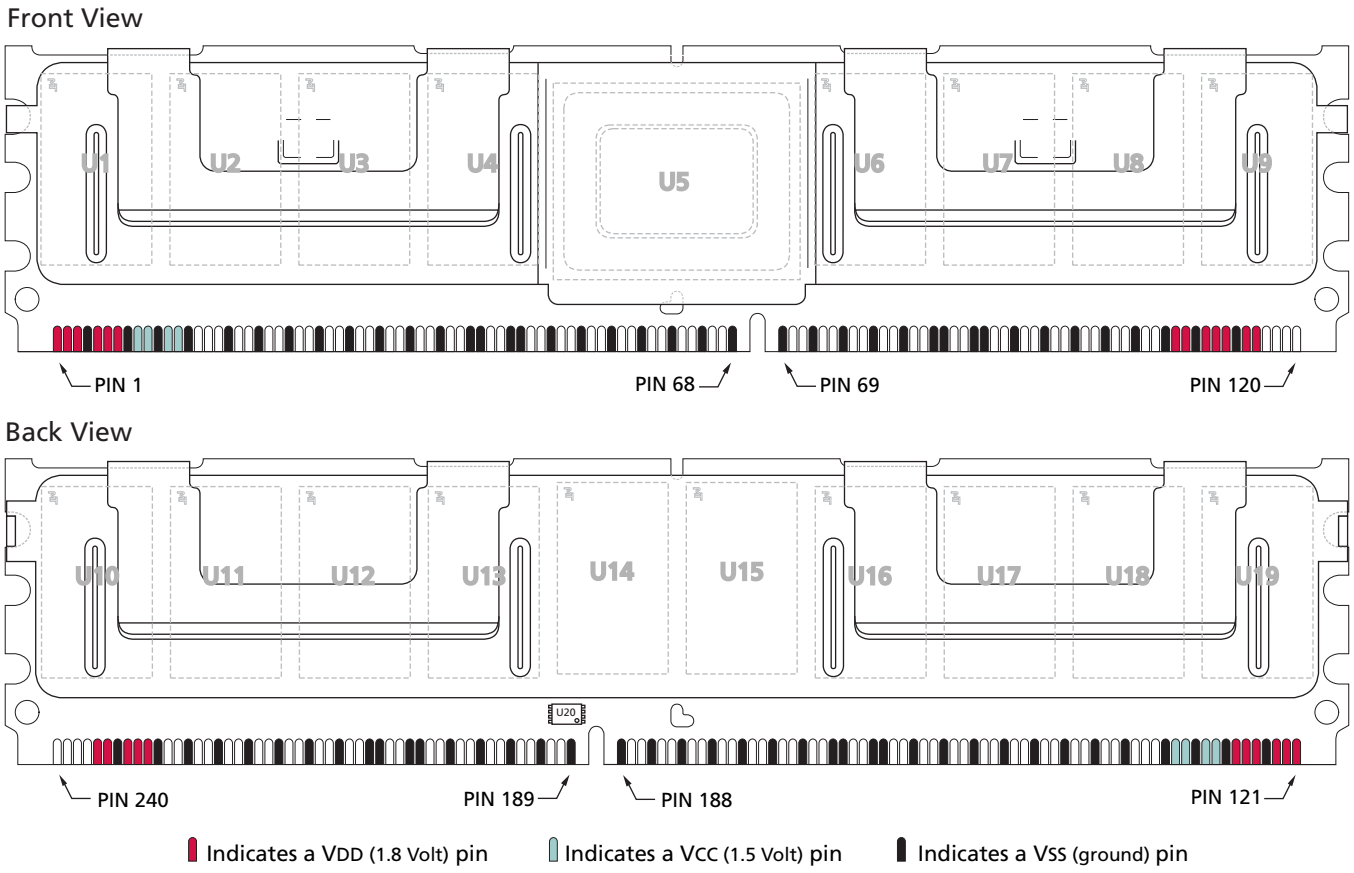


Table 5: Pin Descriptions

Pin Numbers	Symbol	Type	Description
228	SCK	Input	System clock input, positive line
229	SCK#	Input	System clock Input, negative line
22, 25, 28, 31, 34, 37, 40, 48, 51, 54, 57, 60, 63, 66	PN[13:0]	Output	Primary northbound data, positive lines
23, 26, 29, 32, 35, 38, 41, 49, 52, 55, 58, 61, 64, 67	PN#[13:0]	Output	Primary northbound data, negative lines
70, 73, 76, 79, 82, 90, 93, 96, 99, 102	PS[9:0]	Input	Primary southbound data, positive lines
71, 74, 77, 80, 83, 91, 94, 97, 100, 103	PS#[9:0]	Input	Primary southbound data, negative lines
142, 145, 148, 151, 154, 157, 160, 168, 171, 174, 177, 180, 183, 186	SN[13:0]	Output	Secondary northbound data, positive lines
143, 146, 149, 152, 155, 158, 161, 169, 172, 175, 178, 181, 184, 187	SN#[13:0]	Output	Secondary northbound data, negative lines
190, 193, 196, 199, 202, 210, 213, 216, 219, 222	SS[9:0]	Input	Secondary southbound data, positive lines
191, 194, 197, 200, 203, 211, 214, 217, 220, 223	SS#[9:0]	Input	Secondary southbound data, negative lines
120	SCL	Input	Serial presence detect (SPD) clock input
119	SDA	I/O	SPD data input / output
118, 239, 240	SA[2:0]	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB
16, 136	VID[1:0]	NC	Voltage ID: These pins must be unconnected for DDR2-based FBDIMMs; VID[0] is V_{DD} value: OPEN = 1.8V, GND = 1.5V; VID[1] is V_{CC} value: OPEN = 1.5V, GND = 1.2V
17	RESET#	Supply	AMB reset signal
9, 10, 12, 13, 129, 130, 132, 133	V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V)
1, 2, 3, 5, 6, 7, 108, 109, 111, 112, 113, 115, 116, 121, 122, 123, 125, 126, 127, 231, 232, 233, 235, 236	V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.8V)
15, 117, 135, 237	V_{TT}	Supply	DRAM address/command/clock termination power (V_{DD}/2)
238	V_{DDSPD}	Supply	SPD power
4, 8, 11, 14, 18, 21, 24, 27, 30, 33, 36, 39, 42, 43, 46, 47, 50, 53, 56, 59, 62, 65, 68, 69, 72, 75, 78, 81, 84, 85, 88, 89, 92, 95, 98, 101, 104, 107, 110, 114, 124, 128, 131, 134, 138, 141, 144, 147, 150, 153, 156, 159, 162, 163, 166, 167, 170, 173, 176, 179, 182, 185, 188, 189, 192, 195, 198, 201, 204, 205, 208, 209, 212, 215, 218, 221, 224, 227, 230, 234	V_{SS}	Supply	Ground
19, 20, 44, 45, 86, 87, 105, 106, 139, 140, 164, 165, 206, 207, 225, 226	RFU	RFU	Reserved for future use
137	DNU/ M_Test	DNU	The DNU/M_Test pin provides an external connection on R/Cs A–D for testing the margin of V_{REF}, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.3	1.75	V	
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	–0.3	1.75	V	
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.5	2.3	V	
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	–0.5	2.3	V	
Storage temperature	T_{STG}	–55	100	°C	
DDR2 SDRAM device operating temperature (ambient)	T_{CASE}	0	95	°C	1, 2
AMB device operating temperature (ambient)		0	110	°C	

Notes:
1. T_{CASE} is specified at 95°C only when using 2X refresh timing (^{t}REFI = 7.8µs at or below 85°C; ^{t}REFI = 3.9µs above 85°C);DDR2 SDRAM component datasheet, though the FBDIMM does not have an IT option.
2. See applicable DDR2 SDRAM component datasheet for ^{t}REFI and extended mode register settings. The $^{t}REFI_{IT}$ parameter is used to specify the doubled refresh interval necessary to sustain 95°C operation; however, the FBDIMM does not have an IT option.

Table 7: Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	V_{CC}	1.46	1.50	1.54	V	–
DDR2 SDRAM supply voltage	V_{DD}	1.7	1.8	1.9	V	–
Termination voltage	V_{TT}	0.48 × V_{DD}	0.50 × V_{DD}	0.52 × V_{DD}	V	–
EEPROM supply voltage	V_{DDSPD}	1.7	–	3.6	V	–
SPD Input HIGH (logic 1) voltage	$V_{IH(DC)}$	2.1	–	V_{DDSPD}	V	1
SPD Input LOW (logic 0) voltage	$V_{IL(DC)}$		–	0.8	V	1
RESET Input HIGH (logic 1) voltage	$V_{IH(DC)}$	1.0	–		V	2
RESET Input LOW (logic 0) voltage	$V_{IL(DC)}$		–	0.5	V	1
Leakage Current (RESET)	I_L	-90	–	90	µA	2
Leakage Current (link)	I_L	-5	–	5	µA	3

Notes:
1. Applies to SMB and SPD bus signals.
2. Applies to AMB CMOS signal RESET#.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.

Table 8: Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Notes
Electrical idle (EI) assertion pass-through timing	^{t}EI Propagate	–	–	4	CK	
EI de-assertion pass-through timing	^{t}EID	–	–	Bitlock	CK	2
EI assertion duration	^{t}EI	100	–	–	CK	1, 2
FBDIMM command to DDR@ clock out that latches command	–	–	8.1	–	ns	3
FBDIMM command to DDR2 WRITE	–	–	TBD	–	ns	
DDR2 READ to FBDIMM (last FBDIMM)	–	–	5.0	–	ns	4
Resample pass-through time	–	–	1.075	–	ns	
Resynch pass-through time	–	–	2.075	–	ns	
Bitlock interval	^{t}Bitlock	–	–	119	frames	1
Framelock interval	^{t}Framelock	–	–	154	frames	1

Notes:
1. Defined in FBDIMM architecture and protocol specification.
2. Clocks defined as core clocks - 2 × SCK input.
3. For DDR2-667 (PC2-5300), this is measured from the beginning of the frame at the south-bound input to the DDR2 clock output that latches the first command of a frame to the DDR2 SDRAM devices.
4. For DDR2-667 (PC2-5300), this is measured from the latest DQS input to the AMB to the start of the matching data frame at the northbound FBDIMM outputs.

IDD Specifications and Conditions

Assumptions for All Parameters

- primary channel drive strength at 100 percent with de-emphasis at –6.5dB, secondary channel drive strength at 60 percent with de-emphasis at –3dB when enabled.
- Address and data fields are pseudo-random, which provides a 50 percent toggle rate on DDR2 SDRAM data lines and link lanes when data is being transferred.
- Assuming 1 ACTIVATE command and 1 READ/WRITE command per BL = 4 transfer, BL = 4.
- Ten southbound lanes and 14 northbound lanes are enabled and active.

SPD-specific assumptions:

- Number of devices on the specific FBDIMM assumed
- Termination of command, address, and control is actual value used on the FBDIMM
- ECC as per the specific FBDIMM
- SPD specifies ΔT

AMB power-specification assumptions:

- Specific ECC FBDIMM assumed (72-bit data, 14 lanes northbound with DDR2 SDRAMs as defined in configuration options of this data sheet)
- Modeled with 27Ω termination for command, address, and clocks, and 47Ω termination for control
- AMB specification specifies current for each rail

Table 9: DDR2 IDD Specifications and Conditions – 4GB

Parameter/Condition	Symbol	-667	-53E	Units
Idle current, single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE HIGH; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_0	TBD	TBD	mA
Idle current, first FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE HIGH; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_1	TBD	TBD	mA
Idle current, DDR2 SDRAM power-down: L0 state, idle (0 BW); primary and secondary channels enabled, CKE HIGH; command and address lines floated, DDR2 SDRAM clock active; ODT and CKE driven LOW.	IDD_IDLE_2	TBD	TBD	mA
Active Power: L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE HIGH; DDR2 SDRAM clock active.	IDD_ACTIVE_1	TBD	TBD	mA
Active Power, data pass-through: L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE HIGH; DDR2 SDRAM clock active.	IDD_ACTIVE_2	TBD	TBD	mA
Channel standby: Average power over 42 frames where the channel enters and exits L0s; DDR2 SDRAM devices Idle (0 BW); CKE LOW; command and address lines floated; DDR2 SDRAM lock active, ODE and CKE driven LOW.	IDD_L0S	TBD	TBD	mA
Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	IDD_TRAINING	TBD	TBD	mA

Table 10: Reference Clock Input Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Reference clock frequency	*f*SCK	133.33	200	MHz	1, 2
Rise time, fall time	TSCK-RISE, TSCK-FALL	175	700	ps	3
Voltage high	VSCK-HIGH	660	850	mV	
Voltage low	VSCK-LOW	–150		mV	
Absolute crossing point	VCROSS-ABS	250	550	mV	4
Relative crossing point	VCROSS-REL	calculated	calculated	–	4, 5
Percent mismatch between rise and fall times	TSCK-RISE-FALL-MATCH	–	10	%	
Duty cycle of reference clock	TSCK-DUTYCYCLE	40	60	%	
Clock leakage current	II-CK	–10	10	µA	6, 7
Clock input capacitance	CI-CK	0.5	2	pF	7
Clock input capacitance delta	CI_CK(D)	–0.25	0.25	pF	8
Transport delay	T1		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}	–	Periods	11
Reference clock jitter, filtered	TREF-JITTER	–	40	ps	12, 13
Reference clock deterministic jitter	TREF-DJ	–	TBD	ps	

Notes:
1. 133 MHz for PC2-4200 and 166 MHz for PC2-5300.
2. Measured with SSC disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. VCROSS_REL_(MIN) and VCROSS_REL_(MAX) are derived using the following calculation: MIN = 0.5 (V_{HAVG} - 0.710) + 0.250; and MAX = 0.5 (V_{HAVG} - 0.710) + 0.550, where V_{HAVG} is the average of VSCK-HIGHM.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and SCK#.
8. Difference between SCK and SCK# input.
9. T1 = |Tdatapath - Tclockpath| (excluding PLL loop delays). This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter TREF-JITTER.
10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. See Figure 3-3 of the JEDEC specification. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do *not* include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 1,016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10^{16} samples extrapolated from an estimate of the sigma of the random jitter components.
12. Measured with SSC-enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal-MIN parameters.

Table 11: VTT Currents

Description	Symbol	Typ	Max	Unit
Idle current, DDR2 SDRAM device power-down	ITT1	500	700	mA
Active power, 50% DDR2 SDRAM BW	ITT2	500	700	mA

Differential Transmitter and Receiver Specifications

Table 12: Differential Transmitter Output Specifications

Parameter	Symbol	Min	Max	Unit	Comments, Notes
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFFp-p\_L}$	900	1,300	mV	EQ 1, Note 1
Differential peak-to-peak output voltage for regular voltage swing	$V_{TX-DIFFp-p\_R}$	800	–	mV	EQ 1, Note 1
Differential peak-to-peak output voltage for small voltage swing	$V_{TX-DIFFp-p\_S}$	520	–	mV	EQ 1, Note 1
DC common code output voltage for large voltage swing	V_{TX-CM_L}	–	375	mV	EQ 2, Note 1
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	EQ 2, Note 1, 2
De-emphasized differential output voltage ratio for –3.5dB de-emphasis	$V_{TX-DE-3.5-Ratio}$	–3.0	–4.0	dB	Note 1, 3, 4
De-emphasized differential output voltage ratio for –6.0dB de-emphasis	$V_{TX-DE-6.0-Ratio}$	–5.0	–7.0	dB	Note 1, 3, 4
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-ACp-p-L}$	–	90	mV	EQ 7, Note 1, 5
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-ACp-p-R}$	–	80	mV	EQ 7, Note 1, 5
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-ACp-p-S}$	–	70	mV	EQ 7, Note 1, 5
MAX single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE}$	–	50	mV	Note 6
MAX single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-DC}$	–	20	mV	Note 6
MAX peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p}$	–	40	mV	
Single-ended voltage (referenced to Vss) on D+/D–	V_{TX-SE}	–75	750	mV	Note 1, 7
MIN TX eye width, 3.2 and 4.0 Gb/s	$T_{TX-Eye-MIN}$	0.7	–	UI	Note 1, 8
MIN TX eye width 4.8 Gb/s	$T_{TX-EYE-MIN4.8}$	TBD	–	UI	Note 1, 8
MAX TX deterministic jitter, 3.2 and 4.8 Gb/s	$T_{TX-DJ-DD}$	–	0.2	UI	Note 1, 8, 9
MAX TX deterministic jitter, 4.8 Gb/s	$T_{TX-DJ-DD-4.8}$	–	TBD	UI	Note 1, 8, 9
Instantaneous pulse width	$T_{TX\ -PULSE}$	0.85		UI	Note 10
Differential TX output rise/fall time	$T_{TX-RISE}$ $T_{TX-FALL}$	30	90	ps	20–80% voltage, Note 1
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$	–	20	ps	
Differential return loss	$RL_{TX-DIFF}$	8	–	dB	Meas. 0.1–2.4 GHz, Note 11
Common mode return loss	RL_{TX-CM}	6	–	dB	Meas. 0.1–2.4 GHz, Note 11
Transmitter termination impender	R_{TX}	41	55	Ω	12
D+/D– TX Impedance difference	$R_{TX-MATCH-DC}$	–	4	%	EQ 4; Boundaries are applied separately to high and low output voltage states
Lane-to-lane skew at TX	$L_{TX-SKEW\ 1}$	–	100 + 3UI	ps	Note 13, 15
Lane-to-lane skew at TX	$L_{TX-SKEW\ 2}$	–	100 = 2UI	ps	Note 14, 15

Table 12: Differential Transmitter Output Specifications (Continued)

Parameter	Symbol	Min	Max	Unit	Comments, Notes
MAX TX drift (resync mode)	$T_{TX-DRIFT-RESYNC}$	–	240	ps	Note 16
MAX TX drift (resample mode only)	$T_{TX-DRIFT-RESAMPLE}$	–	120	ps	Note 16
Bit error ratio	BER	10^{-12}	–	–	Note 17

Notes:
1. Specified at the package pins into a timing and voltage compliance test load as shown in Figure 4-2 and in steps outlined in 4.1.2.1 of the JEDEC specification. Common-mode measurements to be performed using a 101010 pattern.
2. The transmitter designer should not artificially elevate the common mode in order to meet this specification.
3. This is the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
4. De-emphasis shall be disabled in the calibration state.
5. Includes all sources of AC common mode noise.
6. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the EI condition.
7. The maximum value is specified to be at least (VTX-DIFFp-pL/4) + VTX-CML + (VTX-CM-ACp-p/2).
8. This number does not include the effects of SSC or reference clock jitter.
9. Defined as the expected maximum jitter for the given probability as measured in the system (TJ), less the unbounded jitter.
10. Pulse width measure at 0V differential.
11. One of the components that contribute to the deterioration of the return loss is the ESD structure which must be carefully designed.
12. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed ±5W with regard to the average of the values measured at 100mV and 400mV for that pin.
13. Lane-to-lane skew at the transmitter pins for an end component.
14. Lane-to-lane skew at the transmitter pins for an intermediate component (assuming zero Lane-to-lane skew at the receiver pins of the incoming port).
15. This is a static skew. An FBDIMM component is not allowed to change its lane-to-lane phase relationship after initialization.
16. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate change is significantly below the tracking capability of the receiver.
17. BER per differential lane.

$$V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}| \quad \text{(EQ 1)}$$

$$V_{TX-CM} = DC_{(AVG)} \text{ of } (|V_{TX-D+} + V_{TX-D-}|/2) \quad \text{(EQ 2)}$$

$$V_{TX-CM-AC} = ((\text{Max}\,|V_{TX-D+} + V_{TX-D-}|)/2) - ((\text{Min}\,|V_{TX-D+} + V_{TX-D-}|)/2) \quad \text{(EQ 3)}$$

$$R_{TX-MATCH-DC} = 2 \times ((|R_{TX-D+} - R_{TX-D-}|)/(R_{TX-D+} + R_{TX-D-})) \quad \text{(EQ 4)}$$

Table 13: Differential Receiver Input Specifications

Parameter	Symbol	Min	Max	Unit	Comments, Notes
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFFp-p}$	170	TBD	mV	EQ 5, Note 1
MAX single-ended voltage in EI condition	$V_{RX-IDLE-SE}$	–	75	mV	Note 2, 3
MAX single-ended voltage in EI condition (DC only)	$V_{RX-IDLE-SE-DC}$	–	50	mV	Note 2, 3
MAX peak-to-peak differential voltage in EI condition	$V_{RX-IDLE-DIFFp-p}$	–	65	mV	Note 3
Single-ended voltage (referencing Vss) on D+/D–	V_{RX-SE}	–300	900	mV	Note 4
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85	–	mV	Note 4, 5
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$	–	TBD	–	Note 4, 6
MAX RX inherent timing error, 3.2 and 4.0 Gb/s	$T_{RX-TJ-MAX}$	–	0.4	UI	Note 4, 7, 8
MAX RX inherent deterministic timing error, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX4.8}$	–	TBD	UI	Note 4, 7, 8
Single-pulse width as zero-voltage crossing	$V_{RX-DJ-DD}$	–	0.3	UI	Note 4, 7, 8, 9
Single pulse width at MIN-level crossing	$V_{RX-DJ-DD-4.8}$	–	TBD	UI	Note 4, 7, 8, 9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55	–	UI	Note 4, 5
Common mode input voltage	$T_{RX-PW-ML}$	0.2	–	UI	Note 4, 5
Differential RX output rise/fall time	$T_{RX-RISE}$ $T_{RX-FALL}$	50	–	ps	20–80% voltage
Common mode of input voltage	V_{RX-CM}	120	400	mV	EQ 6, Note 1, 10
AC peak-to-peak common mode of input voltage	$V_{RX-CM-ACp-p}$	–	270	mV	EQ 7, Note 1
Ratio of $V_{RX-CM-ACp-p}$ to MIN $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-RATOP}$	–	45	%	11
Differential return loss	$RL_{RX-DIFF}$	9	–	dB	Meas. 0.1–2.4 GHz, Note 12
Common mode return loss	RL_{RX-CM}	6	–	dB	Meas. 0.1–2.4 GHz, Note 12
RX termination impedance	R_{RX}	41	55	Ω	Note 13
D+/D– RX Impedance difference	$R_{RX-MATCH-DC}$	–	4	%	EQ 8
Lane-to-lane PCB skew at RX	$L_{RX-PCB-SKEW}$	–	6	UI	Lane-to-lane skew at the receiver that must be tolerated, Note 14
MIN RX drift tolerance	$T_{RX-DRIFT}$	400	–	ps	Note 15
MIN data tracking 3dB bandwidth	F_{TRK}	0.2	–	MHz	Note 16
EI entry detect time	$T_{EI-ENTRY-DETECT}$	–	60	ns	Note 17
EI exit detect time	$T_{EI-EXIT-DETECT}$	–	30	ns	
Bit error ratio	BER	–	10^{-12}	–	Note 18

Notes:
1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the EI condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliance test setup.

5. See Figure 3-8 and Figure 3-9 of the JEDEC specification. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. See Figure 3-10 of the JEDEC specification. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of SSC or reference clock jitter.
8. This number includes setup and hold of the RX sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15mV DC offset between transmit and receive devices.
11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if VRX-DIFFp-p is 200mV, the maximum AC peak-to peak common mode is the lesser of (200mV × 0.45 = 90mV) and VRX-CM-AC-p-p.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which must be carefully designed.
13. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed ±5W with regard to the average of the values measured at 100mV and at 400mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI, see Section 4 of the JEDEC specification for full jitter tolerance mask.
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane. Refer to Section 4 of the JEDEC specification for a complete definition of bit error ratio.

$$V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D-}| \quad \text{(EQ 5)}$$

$$(V_{RX\text{-}CM} = DC_{(AVG)} \text{ of } |V_{RX\text{-}D+} + V_{RX\text{-}D-}|/2) \quad \text{(EQ 6)}$$

$$V_{RX\text{-}CM\text{-}AC} = ((MAX\,|V_{RX\text{-}D+} + V_{RX\text{-}D-}|)/2)((MIN\,|V_{RX\text{-}D+} + V_{RX\text{-}D-}|)/2) \quad \text{(EQ 7)}$$

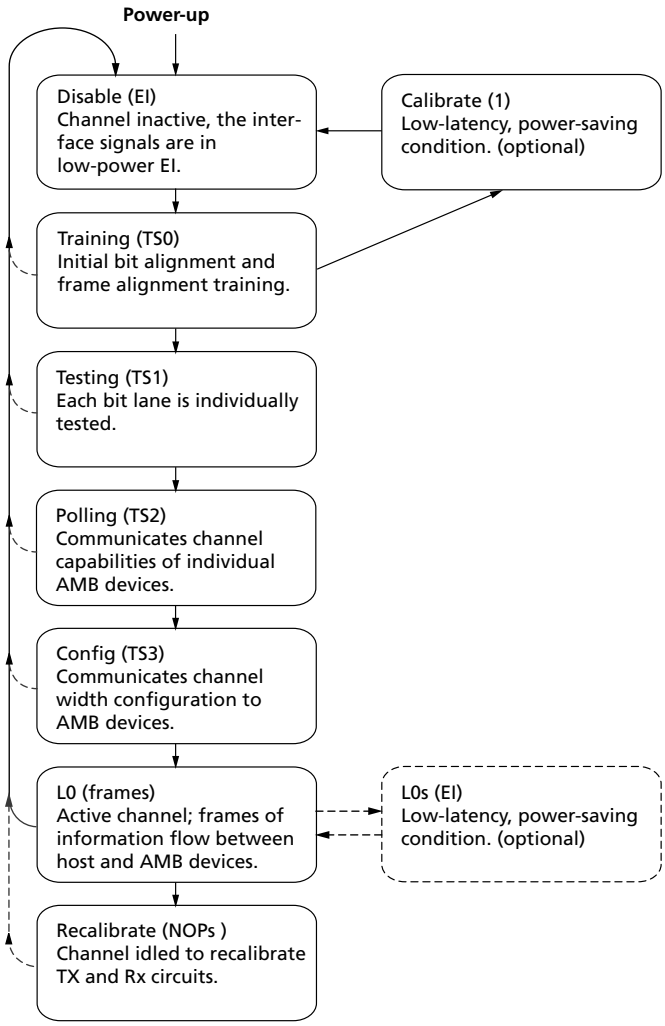
$$R_{RX\text{-}MATCH\text{-}DC} = 2 \times ((|R_{RX\text{-}D+} - R_{RX\text{-}D-}|)/(R_{RX\text{-}D+} + R_{RX\text{-}D-}|)) \quad \text{(EQ 8)}$$

AMB Initialization

The FBDIMM initialization process generally follows the top-to-bottom sequence of state transitions shown in Figure 7. The host must sequence the AMB devices through the disable, calibrate, (back to disable), training, testing, and polling states to move the AMBs into the active channel L0 state. The value in parentheses in each state bubble indicates the condition/activity of the links during these states.

Each bit lane is initialized (mostly) independently to support fault tolerance. The transitions in Figure 7 represent the transitions of the AMB core logic state machine and are taken when the transition event is detected on the minimum required number of southbound bit lanes. The chain of FBDIMM links connecting the host to the AMBs must each be initialized to establish the timing for broadcasting data frames in the southbound direction and for merging data frames in the northbound direction. The AMBs on the channel are generally initialized as a group, but because each AMB is individually addressable, many alternate initialization sequences may be employed.

Figure 7: AMB Initialization Flow Diagram



Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions, as shown in Figures 8 and 9 on page 29.

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data, as shown in Figure 10 on page 29.

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode, the SPD device will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 8: Data Validity

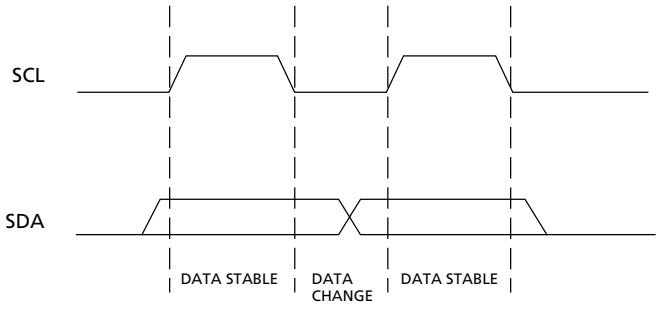


Figure 9: Definition of Start and Stop

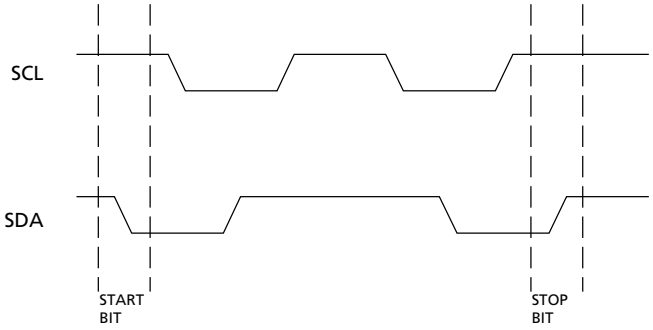


Figure 10: Acknowledge Response from Receiver

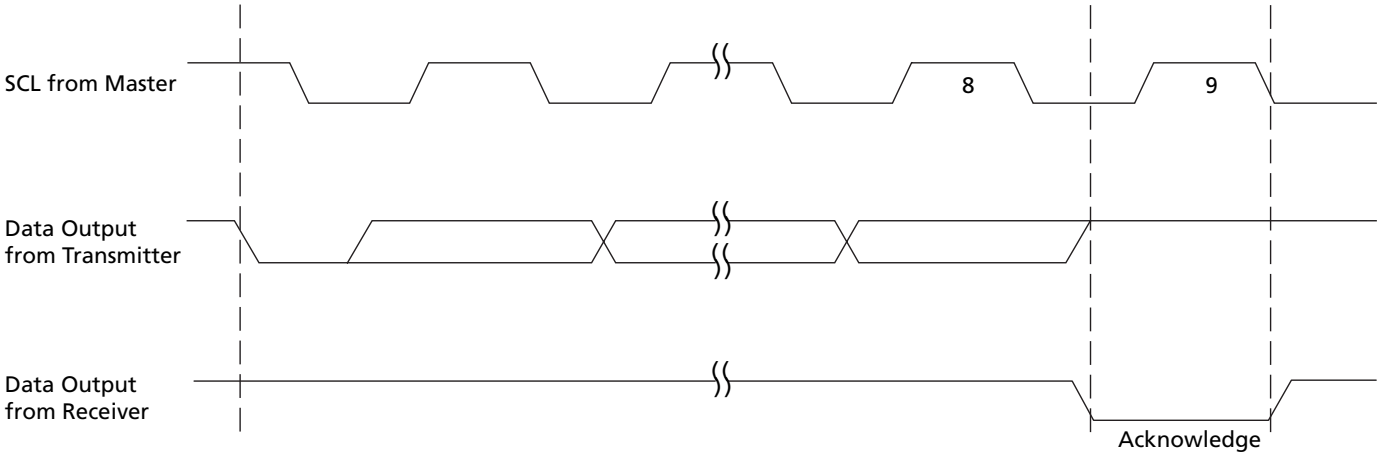


Table 14: EEPROM Device Select Code

The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

Table 15: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	Start, device select, RW = '1'
Random address read	0	VIH or VIL	1	Start, device select, RW = '0', Address
	1	VIH or VIL	1	Restart, device select, RW = '1'
Sequential read	1	VIH or VIL	≥1	Similar to current or random address read
Byte write	0	VIL	1	Start, device select, RW = '0'
Page write	0	VIL	≤16	Start, device select, RW = '0'

Figure 11: SPD EEPROM Timing Diagram

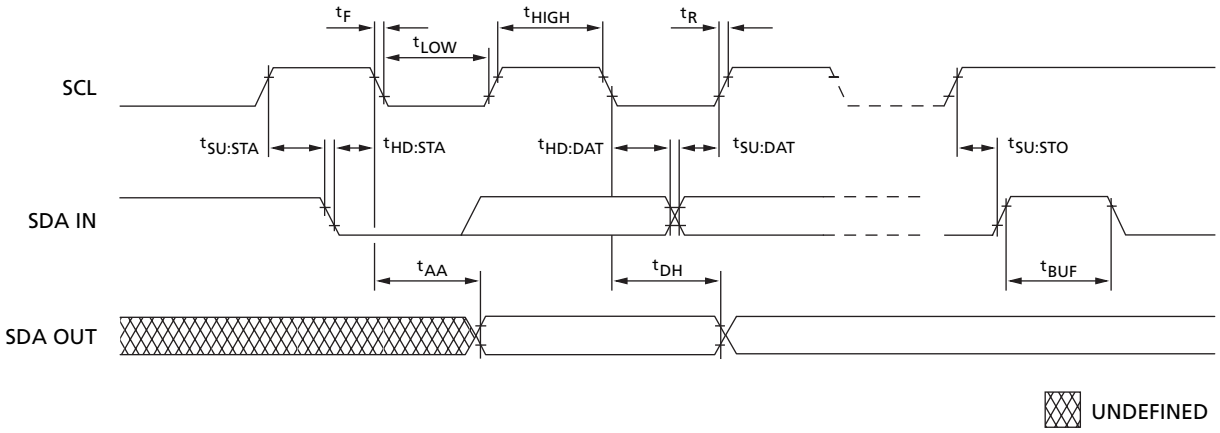


Table 16: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current:	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 18: MT36HTS51272F Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry	MT36HTS51272F		
			D	E	N
0	CRC Range/SPD bytes total/bytes used	Dytes 0–116/ 256 bytes/ 176 bytes	92	92	92
1	SPD revision	1.1	11	11	11
2	Key byte/DRAM device type	DDR2 FBDIMM	09	09	09
3	Voltage levels of this assembly	DRAM/AMB	12	12	12
4	SDRAM addressing: Device rows/columns/banks	1Gb	49	49	49
5	Module physical attributes: Height/thickness	1.18in/0.315–0.354in	25	25	25
6	Module type	FBDIMM	07	07	07
7	Module organization: Module ranks/SDRAM device width (I/O)	Dual rank/x4	10	10	10
8	Fine time-base dividend and divisor	5ps	51	51	51
9	Medium time-base dividend	1/4 = 0.25ns	01	01	01
10	Medium time-base divisor	1/4 = 0.25ns	04	04	04
11	SDRAM MIN cycle time (^{t}CKMIN)	-53E -667	0F 0C	0F 0C	0F 0C
12	SDRAM MAX cycle time (^{t}CKMAX)	-53E, -667	20	20	20
13	SDRAM CLs supported: -53E CL = 4, 3; -667 CL = 5, 4, 3	-53E -667	23 33	23 33	23 33
14	SDRAM MIN CL time (^{t}CAS)	15ns	3C	3C	3C
15	SDRAM WRITE recovery times supported	Range, MIN	22	22	22
16	SDRAM WRITE recovery time (^{t}WR)	-53E, -667	3C	3C	3C
17	SDRAM WRITE latencies supported	Range, MIN	42	42	42
18	SDRAM additive latencies supported	Range, MIN	40	40	40
19	SDRAM MIN RAS-to-CAS delay (^{t}RCD)	-53E, -667	3C	3C	3C
20	SDRAM MIN row active-to-row active delay (^{t}RRD)	-53E, -667	1E	1E	1E
21	SDRAM MIN row precharge time (^{t}RP)	-53E, -667	3C	3C	3C
22	SDRAM upper nibbles for ^{t}RAS and ^{t}RC		00	00	00
23	SDRAM MIN active to precharge time (^{t}RAS)	-53E, -667	B4	B4	B4
24	SDRAM MIN auto-refresh-to-active/auto-refresh time (^{t}RC)	-53E, -667	DC	DC	DC
25	SDRAM MIN auto-refresh-to-active/auto-refresh command period (^{t}RFC - MSB)	–	FE	FE	FE
26	SDRAM MIN auto-refresh-to-active/auto-refresh command period (^{t}RFC - LSB)	–	01	01	01
27	SDRAM internal WRITE-to-READ command delay (^{t}WTR)	-53E, -667	1E	1E	1E
28	SDRAM internal READ-to-PRECHARGE command delay (^{t}RTP)	-53E, -667	1E	1E	1E
29	SDRAM burst lengths supported	4, 8	03	03	03
30	SDRAM drivers/terminations supported: 03 = 75 and 100Ω; 07 = 50, 75, and 100Ω	-53E -667	03 07	03 07	03 07
31	Drivers supported	Weak drivers	01	01	01
32	SDRAM refresh rate (^{t}REFI)	7.8µs	02	02	02

Table 18: MT36HTS51272F Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry	MT36HTS51272F		
			D	E	N
33	Bits 7:4: ΔTCASEMAX (DRAM case temperature difference between MAX case temperature and baseline MAX case temperature), the baseline MAX case temperature is 85°C. Bits 3:0: DT4R4W Δ (case temperature rise difference between IDD4R/page open burst READ and IDD4W/page open burst WRITE operations).	–	01	01	01
34	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM) at still air condition based on JESD51-2 standard.	–	31	31	31
35	DT0/TCASE mode bits: Bits 7:2: Case temperature rise from ambient due to IDD0/activate precharge operation minus 2.8°C offset temperature. Bit 1: Double refresh mode bit. Bit 0: High temperature self-refresh rate support indication.	–	04	04	04
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/ precharge standby operation for UDIMM and due to IDD2Q/ precharge quiet standby operation for RDIMM.	–	0F	0F	0F
37	DT2P: Case temperature rise from ambient due to IDD2P/ precharge power-down operation.	–	0A	0A	0A
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	–	0B	0B	0B
39	DT4R/mode bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	–	18	18	18
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	–	12	12	12
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	–	15	15	15
42–78	FBDIMM reserved bytes	–	00	00	00
79	FBDIMM ODT definition	–	12	12	12
80	FBDIMM reserved byte	–	00	00	00
81	Chanel protocol supported (lower byte)	–	02	02	02
82	Chanel protocol supported (upper byte)	–	00	00	00
83	Back-to-back turnaround clock cycles	–	00	10	15
84	Buffer read access at ^{t}CK for MAX CL	–	36	56	44
85	Buffer read access at ^{t}CK for MAX CL - 1	–	34	40	36
86	Buffer read access at ^{t}CK for MAX CL - 2	–	32	36	30
87	PSI T-A AMB	–	2A	30	2B
88	DT AMB idle_0	-53E -667	54 5E	54 67	4C 55
89	DT AMB idle_1	-53E -667	67 73	6E 7F	69 73
90	DT AMB idle_2	-53E -667	50 5C	60 6E	69 73
91	DT AMB active_1	-53E -667	8D 9B	9A AA	87 92
92	DT AMB active_2	-53E -667	74 80	78 86	69 73

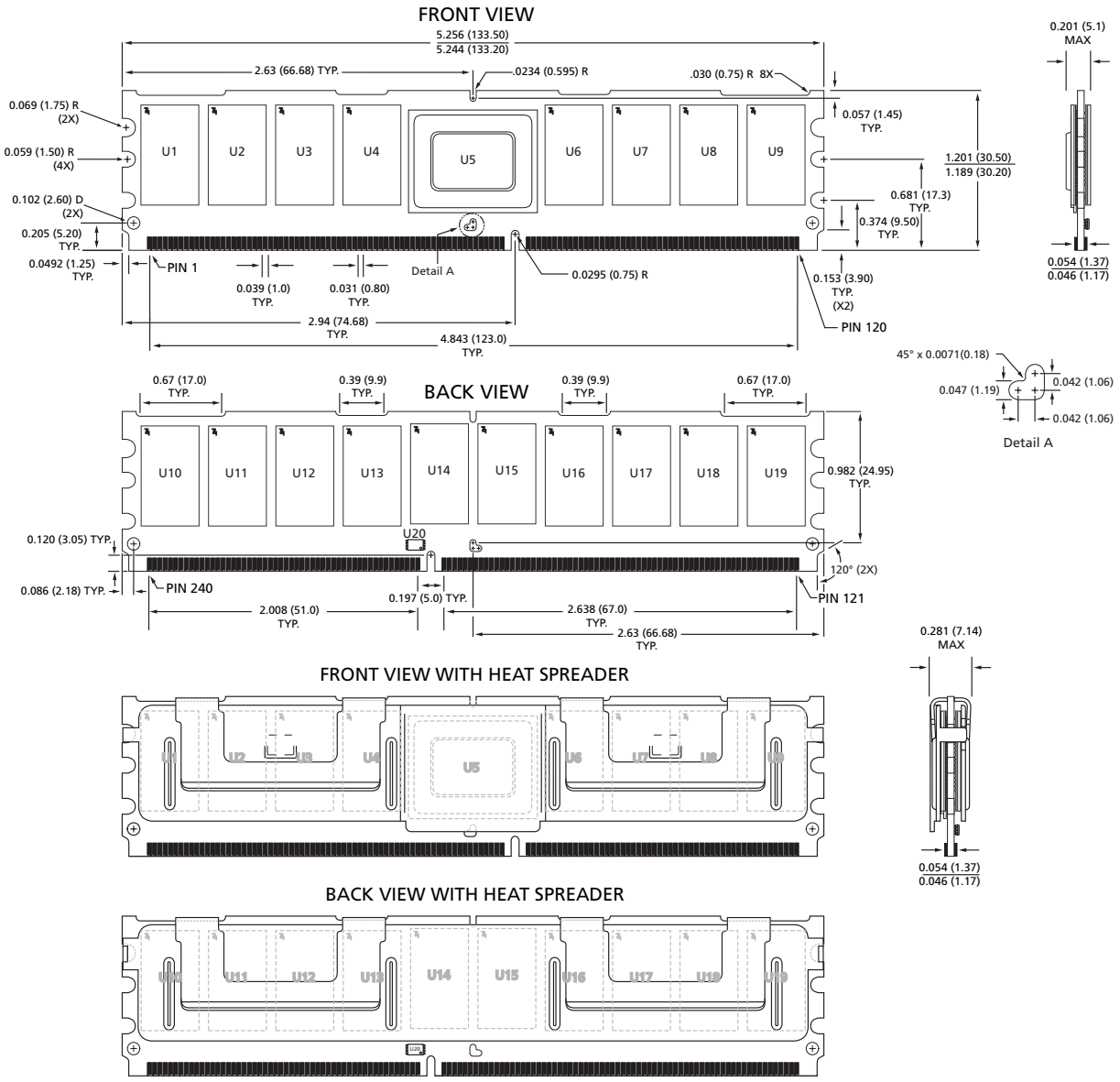
Table 18: MT36HTS51272F Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry	MT36HTS51272F		
			D	E	N
93	DT AMB LOS	-53E -667	00 00	00 00	69 73
94	PSI T-A DRAM-AF	–	00	00	00
95	PSIT-A AMB-AF	–	00	00	00
96	PSI D-A	–	00	00	00
97	PSI A-D	–	00	00	00
98	AMB TJMAX	–	1F	00	1F
99	Airflow imp/DRAM/heat spreader types	–	12	0A	12
100	Reserved	–	00	00	00
101	AMB Pre-initialization bytes	–	40	80	02
102	AMB Pre-initialization bytes	–	C0	20	3C
103	AMB Pre-initialization bytes	–	02	00	10
104	AMB Pre-initialization bytes	–	44	44	01
105	AMB Pre-initialization bytes	–	9C	00	00
106	AMB Pre-initialization bytes	–	30	80	00
107	AMB Post-initialization bytes	–	60	40	00
108	AMB Post-initialization bytes	–	33	53	00
109	AMB Post-initialization bytes	–	60	00	02
110	AMB Post-initialization bytes	–	1B	00	00
111	AMB Post-initialization bytes	–	60	65	00
112	AMB Post-initialization bytes	–	1B	4C	00
113	AMB Post-initialization bytes	–	60	00	00
114	AMB Post-initialization bytes	–	1B	05	00
115	AMB manufacturer's ID code (lower byte)	–	80	80	80
116	AMB manufacturer's ID code (upper byte)	–	B3	89	10
117	Module ID: Module manufacturer's JEDEC ID code	Micron	80	80	80
118	Module ID: Module manufacturer's JEDEC ID code	Micron	2C	2C	2C
119	Module ID: Module manufacturing location	01–12	01–0C	01–0C	01–0C
120–121	Module ID: Module manufacturing date	–	Variable data	Variable data	Variable data
122–125	Module ID: Module serial number	–	Variable data	Variable data	Variable data
126–127	Checksum for bytes 0–116	-53E -667	00DA DBDF	17D5 F105	22BD 5EEC
128–145	Module part number	–	Variable data	Variable data	Variable data
146–147	Module revision code	–	Variable data	Variable data	Variable data
148–149	DRAM manufacturer's JEDEC ID code	Micron	802C	802C	802C
150–175	Manufacturer-specific data (RSVD)	–	FF	FF	FF
176–255	Open for customer use	–	FF	FF	FF

Module Dimensions

All dimensions are in inches (millimeters). The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 12: 240-pin DDR2 FBDIMM Module Dimensions



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