DDR2 SDRAM SODIMM

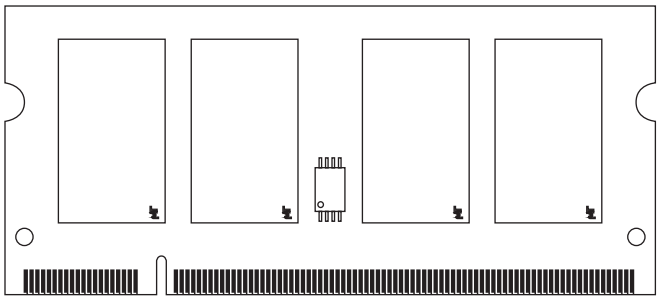
MT16HTS25664H – 2GB

For component specifications, refer to Micron's Web site: www.micron.com/products/ddr2sdram

Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- 2GB (256 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +1.8V
- V_{DDSPD} = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 200-pin SODIMM (MO-224 R/C "B")



Options	Marking
• Package	
– 200-pin SODIMM (lead-free)	Y
• Frequency/CAS latency[1]	
– 3ns @ CL = 5 (DDR2-667)[2]	-667
– 3.75ns @ CL = 4 (DDR2-533)	-53E
– 5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB height	
– 1.18in (29.97mm)	

Notes: 1. CL = CAS (READ) Latency.
2. Contact Micron for product availability.

Table 1: Address Table

	2GB
Refresh count	8K
Row addressing	16K (A0–A13)
Device bank addressing	8 (BA0, BA1, BA2)
Device page size per bank	1KB
Device configuration	1Gb (128 Meg x 8)
Column addressing	1K (A0–A9)
Module rank addressing	2 (S0#, S1#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5			
-667	400	533	667	15	15	55
-53E	400	533	–	15	15	55
-40E	400	400	–	15	15	55

Table 3: Part Numbers and Timing Parameters

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT16HTS25664HY-667__	2GB	256 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTS25664HY-53E__	2GB	256 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTS25664HY-40E__	2GB	256 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16HTF12864HY-40EA1.

Module Pin Assignments and Descriptions

Table 4: Pin Assignment

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42	2	VSS	52	DM2	102	A0	152	DQ46
3	VSS	53	VSS	103	VDD	153	DQ43	4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS	6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	VSS	58	DQ23	108	RAS#	158	DQ52
9	VSS	59	VSS	109	WE#	159	DQ49	10	DM0	60	VSS	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	VSS	12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	VSS	65	VSS	115	S1#	165	VSS	16	DQ7	66	VSS	116	A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	VSS	68	DQS3#	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS	22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS	28	VSS	78	VSS	128	VSS	178	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS	34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	VSS	38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58	40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59	42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS	44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	VSS
47	VSS	97	A5	147	DM5	197	SCL	48	VSS	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	VSS	199	VDDSPD	50	NC	100	A2	150	VSS	200	SA1

Figure 2: Pin Locations

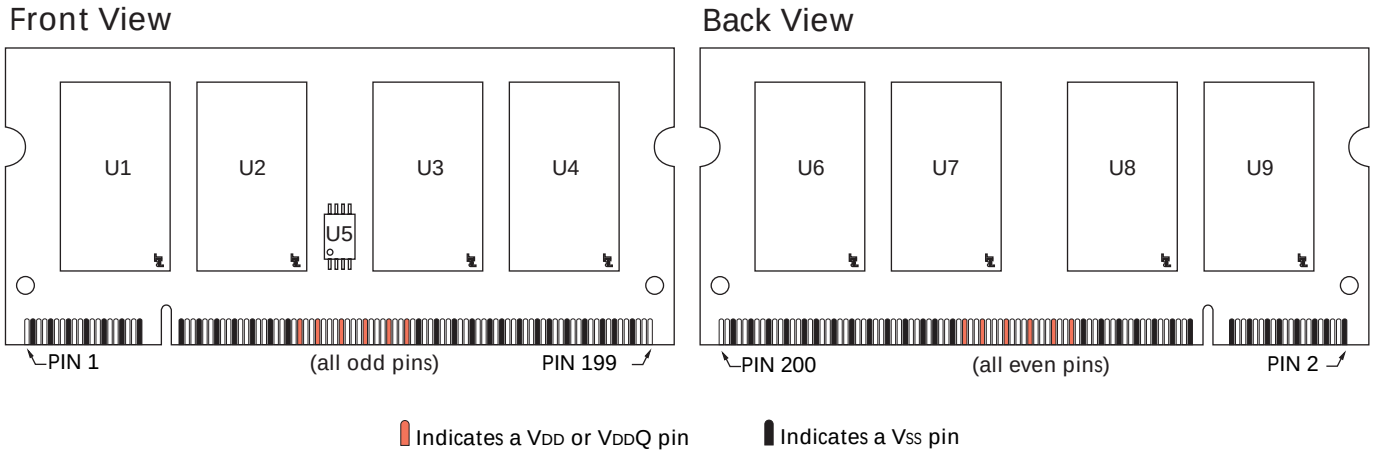


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 3 for more information

Pin Numbers	Symbol	Type	Description
114, 119	ODT0, ODT1	Input	On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
30, 32, 164, 166	CK0, CK0# CK1, CK1#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
79, 80	CKE0, CKE1	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all device banks idle), or active power-down (row active in any device bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation V_{REF} must be maintained to this input.
110, 115	S0#, S1#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
108, 109, 113	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
85, 106, 107	BA0, BA1, BA2	Input	Bank address inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
89, 90, 91, 92, 93, 94, 97, 98, 99, 100, 101, 102, 105	A0–A13	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
10, 26, 52, 67, 130, 147, 170, 185	DM0–DM7	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.

Table 5: Pin Descriptions

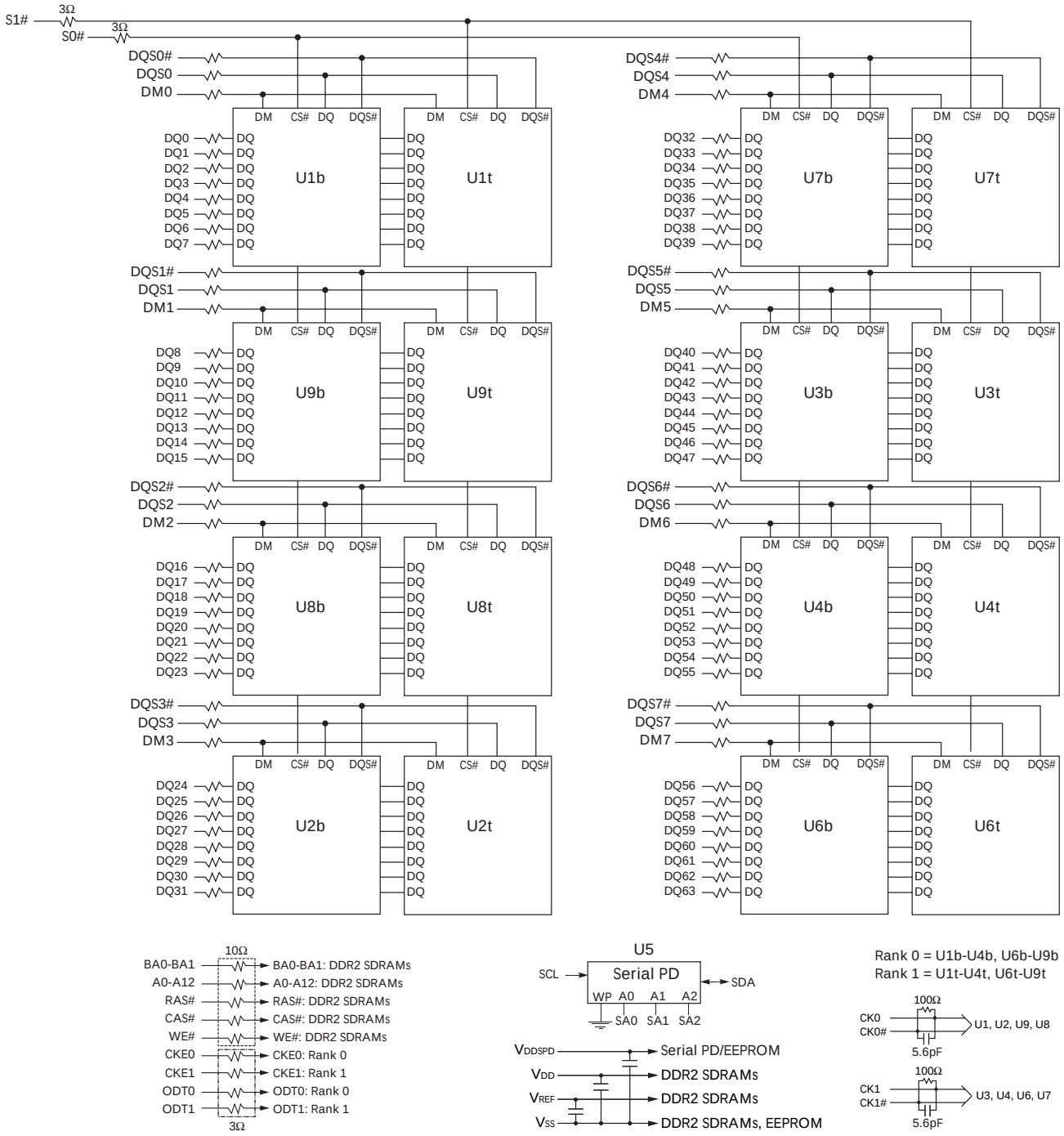
Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 3 for more information

Pin Numbers	Symbol	Type	Description
197	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
198, 200	SA0–SA1	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
4, 5, 6, 7, 14, 16, 17, 19, 20, 22, 23, 25, 35, 36, 37, 38, 43, 44, 45, 46, 55, 56, 57, 58, 61, 62, 63, 64, 73, 74, 75, 76, 123, 124, 125, 126, 134, 135, 136, 137, 140, 141, 142, 143, 151, 152, 153, 154, 157, 158, 159, 160, 173, 174, 175, 176, 179, 180, 181, 182, 189, 191, 192, 194	DQ0–DQ63	I/O	Data input/output: Bidirectional data bus.
11, 13, 29, 31, 49, 51, 68, 70, 129, 131, 146, 148, 167, 169, 186, 188	DQS0–DQS7, DQS0#–DQS7#	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
195	SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
81, 82, 87, 88, 95, 96, 103, 104, 111, 112, 117, 118	V_{DD}	Supply	Power supply: +1.8 ±0.1V.
1	V_{REF}	Supply	SSTL_18 reference voltage.
2, 3, 8, 9, 12, 15, 18, 21, 24, 27, 28, 33, 34, 39, 40, 41, 42, 47, 48, 53, 54, 59, 60, 65, 66, 71, 72, 77, 78, 121, 122, 127, 128, 132, 133, 138, 139, 144, 145, 149, 150, 155, 156, 161, 162, 165, 168, 171, 172, 177, 178, 183, 184, 187, 190, 193, 196	V_{SS}	Supply	Ground.
199	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
50, 69, 80, 83, 84, 85	NC	–	No connect: These pins should be left unconnected.

Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω. Micron module part numbers are explained in the Module Part Numbering Guide a www.micron.com/support/numbering.html. Modules use the following DDR2 SDRAM devices: MT47H128M8BT (1GB). Component specifications are available at: www.micron.com/products/ddr2sdram.

Figure 3: Functional Block Diagram



General Description

The MT16HTS25664H DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 2GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured eight-bank DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect (SPD) Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum DC Ratings

Parameter		Symbol	Min	Max	Units
VDD supply voltage relative to VSS		VDD	–1.0	2.3	V
VDDQ supply voltage relative to VSS		VDDQ	–0.5	2.3	V
VDDL supply voltage relative to VSS		VDDL	–0.5	2.3	V
Voltage on any pin relative to VSS		VIN, VOUT	–0.5	2.3	V
Storage temperature		T_{STG}	–55	100	°C
DDR2 SDRAM device operating temperature (ambient)		T_{CASE}	0	85	°C
Operating temperature (ambient)		T_{OPR}	0	65	°C
Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE	I_I	–80	80	µA
	CK, CK#		–40	40	
	DM		–10	10	
Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	I_{OZ}	–10	10	µA
VREF leakage current; VREF = Valid VREF level		I_{VREF}	–32	32	µA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

Table 7: DDR2 IDD Specifications and Conditions – 2GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0[a]	840	680	680	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1[a]	1,200	800	800	mA
Precharge power-down current; All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P[b]	112	80	80	mA
Precharge quiet standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q[b]	960	656	560	mA
Precharge standby current; All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N[b]	1,040	720	560	mA
Active power-down current; All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	IDD3P[b]	640	480	400	mA
	Slow PDN Exit MR[12] = 1		80	80	80	mA
Active standby current; All device banks open; tCK = tCK(IDD), tRAS = tRAS MAX (IDD), tRP = tRP(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N[b]	1,120	800	640	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W[a]	1,480	1,080	1,000	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R[a]	1,680	1,200	1,120	mA
Burst refresh current; tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5[b]	4,320	4,000	3,840	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6[b]	112	80	80	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD)-1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.		IDD7[a]	2,760	2,400	2,400	mA

Note:
a. Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b. Value calculated reflects all module ranks in this operating condition.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets, available at www.micron.com/products/ddr2sdram. Module speed grades correlate with component speed grades as shown in the following table:

Table 8: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-667	-3
-53E	-37E
-40E	-53E

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 4 on page 11, and Figure 5 on page 11).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 6 on page 11).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 4: Data Validity

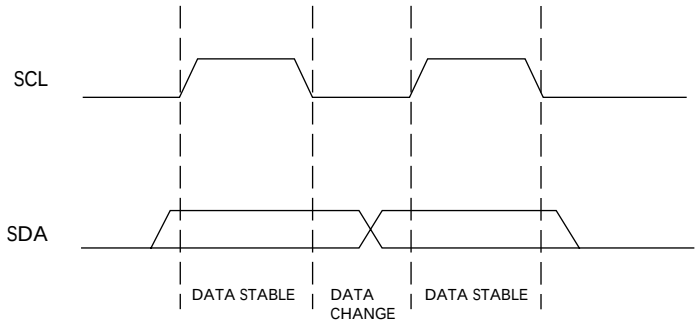


Figure 5: Definition of Start and Stop

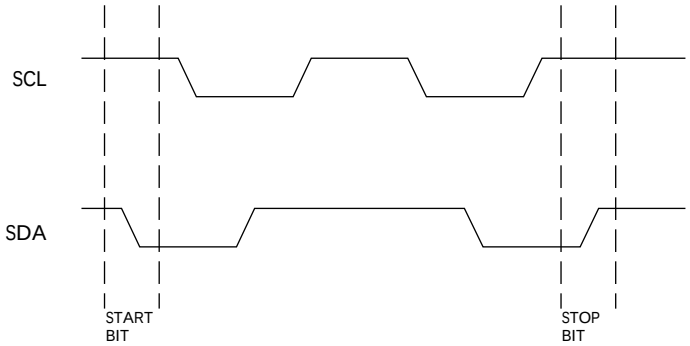


Figure 6: Acknowledge Response From Receiver

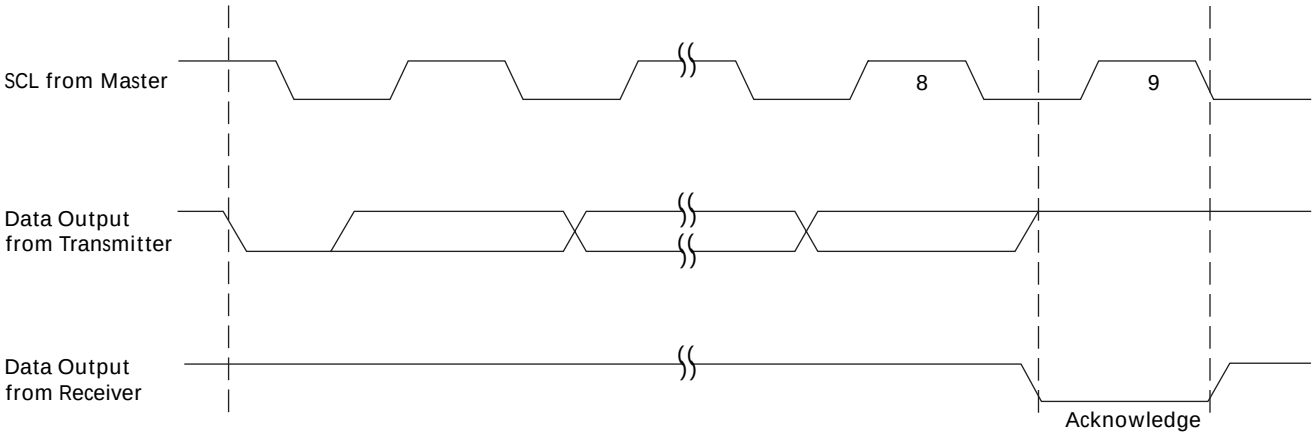


Table 9: EEPROM Device Select Code

The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

Table 10: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	START, Device select, RW = '1'
Random address read	0	VIH or VIL	1	START, Device select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device select, RW = '1'
Sequential read	1	VIH or VIL	≥ 1	Similar to current or random address read
Byte write	0	VIL	1	START, Device select, RW = '0'
Page write	0	VIL	≤ 16	START, Device select, RW = '0'

Figure 7: SPD EEPROM Timing Diagram

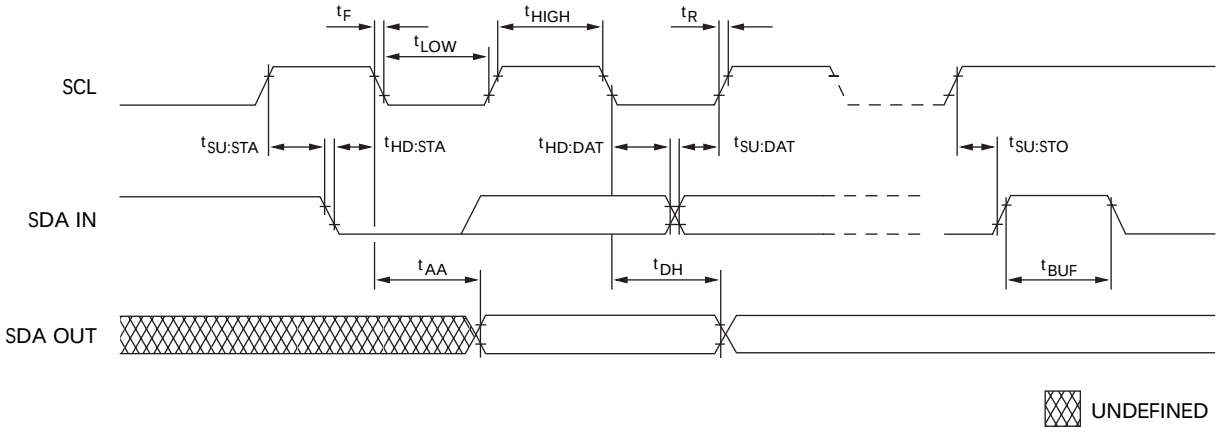


Table 11: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Inputl low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current:	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 12: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^fSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 13: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 15

Byte	Description	Entry (Version)	MT16HTS25664H
0	Number of SPD bytes used by Micron	128	80
1	Total number of bytes in SPD device	256	08
2	Fundamental memory type	DDR2 SDRAM	08
3	Number of row addresses on assembly	14	0E
4	Number of column addresses on assembly	10	0A
5	DIMM height and module ranks	1.18in, dual rank	61
6	Module data width	64	40
7	Reserved		00
8	Module voltage interface levels	SSTL 1.8V	05
9	SDRAM cycle time, ^{t}CK (CL = maximum value, see byte 18)	-667 -53E -40E	30 3D 50
10	SDRAM access from clock, ^{t}AC (CL = maximum value, see byte 18)	-667 -53E -40E	45 50 60
11	Module configuration type		00
12	Refresh rate/type	7.81µs/SELF	82
13	SDRAM device width (primary SDRAM)	8	08
14	Error-checking SDRAM data width	N/A	00
15	Reserved		00
16	Burst lengths supported	4, 8	0C
17	Number of banks on SDRAM device	8	08
18	CAS latencies supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18
19	Module thickness		01
20	DDR2 DIMM type	SODIMM	04
21	SDRAM module attributes		00
22	SDRAM device attributes: Weak driver (01) and 50Ω ODT (03)	-667 -53E/-40E	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-667 -53E/-40E	3D 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-667/-53E -40E	45 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-667 -53E/-40E(N/A)	50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-667 -53E/-40E(N/A)	45 00
27	Minimum row precharge time, ^{t}RP		3C
28	Minimum row active to row active, ^{t}RRD		1E
29	Minimum RAS# to CAS# delay, ^{t}RCD		3C
30	Minimum RAS# pulse width, ^{t}RAS (see note 1)	-667/-53E -40E	2D 28
31	Module rank density	1GB	01
32	Address and command setup time, $^{t}IS_{b}$	-667/-53E -40E	20 35

Table 13: Serial Presence-Detect Matrix

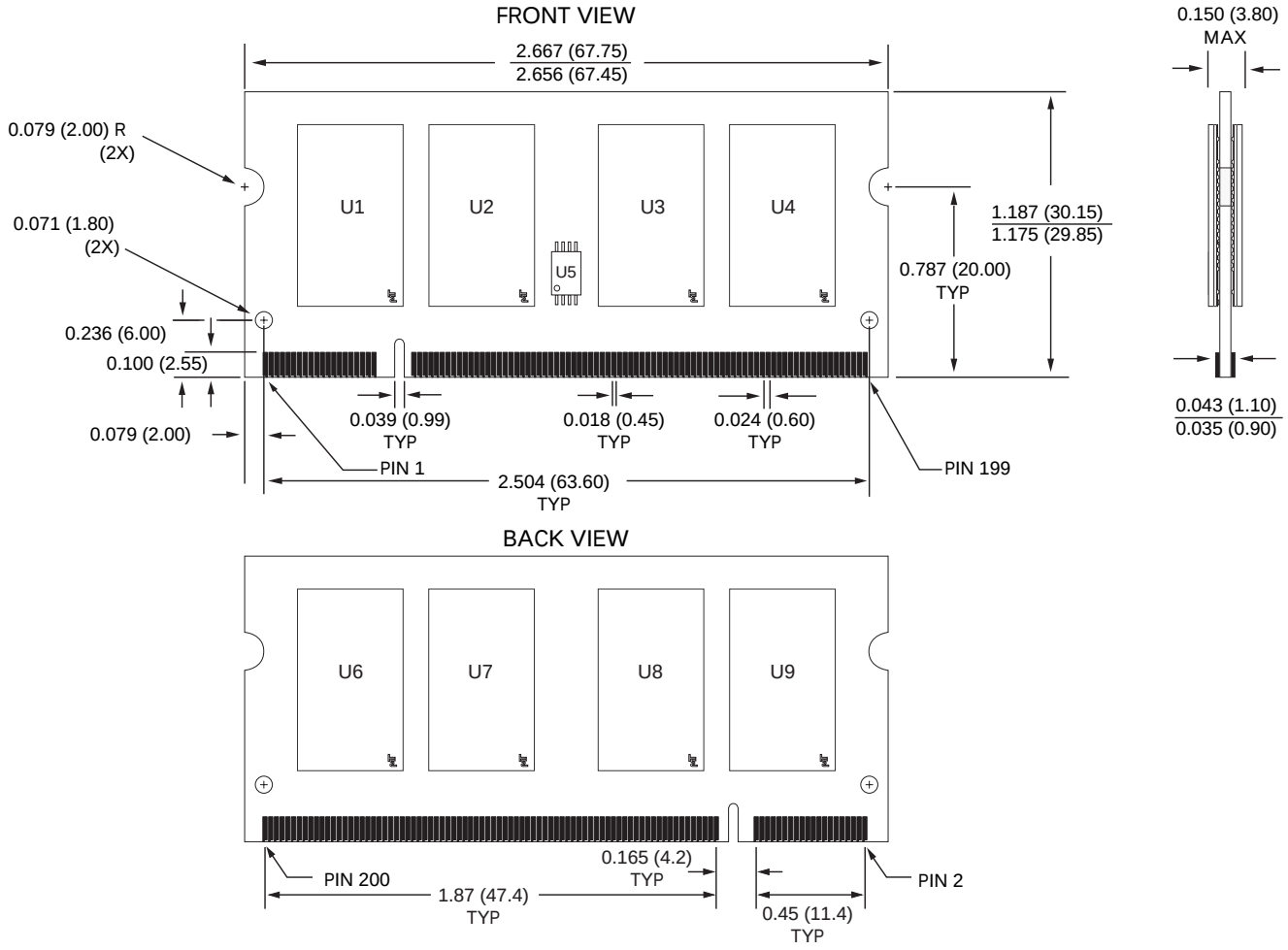
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 15

Byte	Description	Entry (Version)	MT16HTS25664H
33	Address and command hold time, $^{t}IH_{b}$	-667 -53E -40E	27 37 47
34	Data/ Data mask input setup time, $^{t}DS_{b}$	-667/-53E -40E	10 15
35	Data/ Data mask input hold time, $^{t}DH_{b}$	-667 -53E -40E	17 22 27
36	Write recovery time, ^{t}WR		3C
37	Write to Read CMD delay, ^{t}WTR	-667/-53E -40E	1E 28
38	Read to precharge CMD delay, ^{t}RTP		1E
39	Memory analysis probe		00
40	Extension for bytes 41 and 42		06
41	Minimum active auto refresh time, ^{t}RC	-667/-53E -40E	3C 37
42	Minimum auto refresh to active/ auto refresh command period, ^{t}RFC		7F
43	SDRAM device MAX cycle time, $^{t}CK_{MAX}$		80
44	SDRAM device MAX DQS-DQ skew time, $^{t}DQSQ$	-667 -53E -40E	18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-667 -53E -40E	22 28 2D
46	PLL relock time		00
47–61	Optional features, not supported		00
62	SPD revision	Release 1.2	12
63	Checksum For bytes 0–62	-667 -53E -40E	EF 9A 01
64	Manufacturer's JEDEC ID code	MICRON	2C
65–71	Manufacturer's JEDEC ID code	(Continued)	FF
72	Manufacturing location	01–12	01–0C
73–90	Module part number (ASCII)		Variable data
91	PCB identification code	1–9	01–09
92	Identification code (continued)	0	00
93	Year of manufacture in BCD		Variable data
94	Week of manufacture in BCD		Variable data
95–98	Module serial number		Variable data
99–127	Manufacturer-Specific data (RSVD)		–

Notes: 1. The ^{t}RAS SPD value shown is based on the JEDEC standard value of 45 ns; the actual device specification is ^{t}RAS = 40ns.

Module Dimensions

Figure 8: 200-pin DDR2 SODIMM Module Dimensions



Notes:
1. All dimensions are in inches (millimeters); MAX/MIN or TYP where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

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