

DDR2 SDRAM FBDIMM

MT18HTF12872FD – 1GB

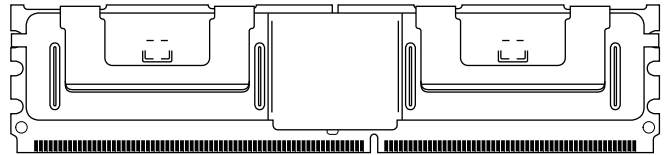
MT18HTF25672FD – 2GB

Features

- 240-pin, DDR2 fully buffered dual in-line memory module (FBDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 1GB (128 Meg x 72), 2GB (256 Meg x 72)
- 3.2 Gb/s, 4 Gb/s, or 4.8 Gb/s link transfer rates
- High-speed, 1.5V differential, point-to-point link between the host controller and advanced memory buffer (AMB)
- Fault-tolerant; can work around a bad bit lane in each direction
- High-density scaling with up to eight FBDIMM devices per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
 - Enables memory controller to optimize DRAM accesses for maximum performance
 - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI
- MBIST and IBIST test functions
- Transparent mode for DRAM test support
- $V_{DD} = V_{DDQ} = 1.8V$ for DRAM
- $V_{REF} = 0.9V$ SDRAM command/address termination
- $V_{CC} = 1.5V$ for AMB
- $V_{DDSPD} = 3-3.6V$ for AMB and EEPROM
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank
- Supports 95°C operation with 2X refresh

Figure 1: 240-Pin FBDIMM (MO-256 R/C B)

Module height: 30.35mm (1.19in)



Options

- Package
 - 240-pin DIMM (Pb-free)
- Frequency/CAS latency
 - 2.5ns @ CL = 5 (DDR2-800)
 - 3.0ns @ CL = 5 (DDR2-667)
 - 3.75ns @ CL = 4 (DDR2-533)¹

Marking

Y
-80E
-667
-53E

Note: 1. Not recommended for new designs.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | ^t RCD (ns) | ^t RP (ns) | ^t RC (ns) |
|-------------|-----------------------|------------------|--------|--------|-----------------------|----------------------|----------------------|
| | | CL = 5 | CL = 4 | CL = 3 | | | |
| -80E | PC2-6400 | 800 | 533 | – | 12.5 | 12.5 | 55 |
| -667 | PC2-5300 | 667 | 533 | 400 | 15 | 15 | 55 |
| -53E | PC2-4200 | – | 533 | 400 | 15 | 15 | 55 |

Table 2: Addressing

| Parameter | 1GB | 2GB |
|---------------------------|--------------------|-------------------|
| Refresh count | 8K | 8K |
| Device bank address | 4 BA[1:0] | 8 BA[2:0] |
| Device page size per bank | 1KB | 1KB |
| Device configuration | 512Mb (64 Meg x 8) | 1Gb (128 Meg x 8) |
| Row address | 16K A[13:0] | 16K A[13:0] |
| Column address | 2K A[9:0] | 2K A[9:0] |
| Module rank address | 2 S#[1:0] | 2 S#[1:0] |

Table 3: Part Numbers and Timing Parameters – 1GB

Base device: MT47H64M8,¹ 512Mb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) | Link Transfer Rate |
|--------------------------|----------------|---------------|------------------|------------------------|--|--------------------|
| MT18HTF12872FDY-80E__ | 1GB | 128 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 | 4.8 GT/s |
| MT18HTF12872FDY-667__ | 1GB | 128 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 | 4.0 GT/s |
| MT18HTF12872FDY-53E__ | 1GB | 128 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 | 3.2 GT/s |

Table 4: Part Numbers and Timing Parameters – 2GB

Base device: MT47H128M8,¹ 1Gb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) | Link Transfer Rate |
|--------------------------|----------------|---------------|------------------|------------------------|--|--------------------|
| MT18HTF25672FDY-80E__ | 2GB | 256 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 | 4.8 GT/s |
| MT18HTF25672FDY-667__ | 2GB | 256 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 | 4.0 GT/s |
| MT18HTF25672FDY-53E__ | 2GB | 256 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 | 3.2 GT/s |

- Notes:
1. Data sheets for the base devices can be found on Micron’s Web page.
 2. All part numbers end with a four-place code (not shown) that designates component, PCB, and AMB revisions. Consult factory for current revision codes. Example: MT18HTF25672FDY-667E1D4.

Pin Assignments and Descriptions

Table 5: Pin Assignments

| 240-Pin FBDIMM Front | | | | | | | | 240-Pin FBDIMM Back | | | | | | | |
|----------------------|-----------------|-----|--------------------|-----|------------------|-----|-------------------|---------------------|-----------------|-----|--------------------|-----|------------------|-----|--------------------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | V _{DD} | 31 | PN3 | 61 | PN9# | 91 | PS9# ¹ | 121 | V _{DD} | 151 | SN3 | 181 | SN9# | 211 | SS9# ¹ |
| 2 | V _{DD} | 32 | PN3# | 62 | V _{SS} | 92 | V _{SS} | 122 | V _{DD} | 152 | SN3# | 182 | V _{SS} | 212 | V _{SS} |
| 3 | V _{DD} | 33 | V _{SS} | 63 | PN10 | 93 | PS5 | 123 | V _{DD} | 153 | V _{SS} | 183 | SN10 | 213 | SS5 |
| 4 | V _{SS} | 34 | PN4 | 64 | PN10# | 94 | PS5# | 124 | V _{SS} | 154 | SN4 | 184 | SN10# | 214 | SS5# |
| 5 | V _{DD} | 35 | PN4# | 65 | V _{SS} | 95 | V _{SS} | 125 | V _{DD} | 155 | SN4# | 185 | V _{SS} | 215 | V _{SS} |
| 6 | V _{DD} | 36 | V _{SS} | 66 | PN11 | 96 | PS6 | 126 | V _{DD} | 156 | V _{SS} | 186 | SN11 | 216 | SS6 |
| 7 | V _{DD} | 37 | PN5 | 67 | PN11# | 97 | PS6# | 127 | V _{DD} | 157 | SN5 | 187 | SN11# | 217 | SS6# |
| 8 | V _{SS} | 38 | PN5# | 68 | V _{SS} | 98 | V _{SS} | 128 | V _{SS} | 158 | SN5# | 188 | V _{SS} | 218 | V _{SS} |
| 9 | V _{CC} | 39 | V _{SS} | 69 | V _{SS} | 99 | PS7 | 129 | V _{CC} | 159 | V _{SS} | 189 | V _{SS} | 219 | SS7 |
| 10 | V _{CC} | 40 | PN13 ¹ | 70 | PS0 | 100 | PS7# | 130 | V _{CC} | 160 | SN13 ¹ | 190 | SS0 | 220 | SS7# |
| 11 | V _{SS} | 41 | PN13# ¹ | 71 | PS0# | 101 | V _{SS} | 131 | V _{SS} | 161 | SN13# ¹ | 191 | SS0# | 221 | V _{SS} |
| 12 | V _{CC} | 42 | V _{SS} | 72 | V _{SS} | 102 | PS8 | 132 | V _{CC} | 162 | V _{SS} | 192 | V _{SS} | 222 | SS8 |
| 13 | V _{CC} | 43 | V _{SS} | 73 | PS1 | 103 | PS8# | 133 | V _{CC} | 163 | V _{SS} | 193 | SS1 | 223 | SS8# |
| 14 | V _{SS} | 44 | DNU | 74 | PS1# | 104 | V _{SS} | 134 | V _{SS} | 164 | DNU | 194 | SS1# | 224 | V _{SS} |
| 15 | V _{TT} | 45 | DNU | 75 | V _{SS} | 105 | DNU | 135 | V _{TT} | 165 | DNU | 195 | V _{SS} | 225 | DNU |
| 16 | DNU | 46 | V _{SS} | 76 | PS2 | 106 | DNU | 136 | DNU | 166 | V _{SS} | 196 | SS2 | 226 | DNU |
| 17 | RESET# | 47 | V _{SS} | 77 | PS2# | 107 | V _{SS} | 137 | M_Test (DNU) | 167 | V _{SS} | 197 | SS2# | 227 | V _{SS} |
| 18 | V _{SS} | 48 | PN12 ¹ | 78 | V _{SS} | 108 | V _{DD} | 138 | V _{SS} | 168 | SN12 ¹ | 198 | V _{SS} | 228 | SCK |
| 19 | DNU | 49 | PN12# ¹ | 79 | PS3 | 109 | V _{DD} | 139 | DNU | 169 | SN12# ¹ | 199 | SS3 | 229 | SCK# |
| 20 | DNU | 50 | V _{SS} | 80 | PS3# | 110 | V _{SS} | 140 | DNU | 170 | V _{SS} | 200 | SS3# | 230 | V _{SS} |
| 21 | V _{SS} | 51 | PN6 | 81 | V _{SS} | 111 | V _{DD} | 141 | V _{SS} | 171 | SN6 | 201 | V _{SS} | 231 | V _{DD} |
| 22 | PN0 | 52 | PN6# | 82 | PS4 | 112 | V _{DD} | 142 | SN0 | 172 | SN6# | 202 | SS4 | 232 | V _{DD} |
| 23 | PN0# | 53 | V _{SS} | 83 | PS4# | 113 | V _{DD} | 143 | SN0# | 173 | V _{SS} | 203 | SS4# | 233 | V _{DD} |
| 24 | V _{SS} | 54 | PN7 | 84 | V _{SS} | 114 | V _{SS} | 144 | V _{SS} | 174 | SN7 | 204 | V _{SS} | 234 | V _{SS} |
| 25 | PN1 | 55 | PN7# | 85 | V _{SS} | 115 | V _{DD} | 145 | SN1 | 175 | SN7# | 205 | V _{SS} | 235 | V _{DD} |
| 26 | PN1# | 56 | V _{SS} | 86 | DNU | 116 | V _{DD} | 146 | SN1# | 176 | V _{SS} | 206 | DNU | 236 | V _{DD} |
| 27 | V _{SS} | 57 | PN8 | 87 | DNU | 117 | V _{TT} | 147 | V _{SS} | 177 | SN8 | 207 | DNU | 237 | V _{TT} |
| 28 | PN2 | 58 | PN8# | 88 | V _{SS} | 118 | SA2 | 148 | SN2 | 178 | SN8# | 208 | V _{SS} | 238 | V _{DDSPD} |
| 29 | PN2# | 59 | V _{SS} | 89 | V _{SS} | 119 | SDA | 149 | SN2# | 179 | V _{SS} | 209 | V _{SS} | 239 | SA0 |
| 30 | V _{SS} | 60 | PN9 | 90 | PS9 ¹ | 120 | SCL | 150 | V _{SS} | 180 | SN9 | 210 | SS9 ¹ | 240 | SA1 |

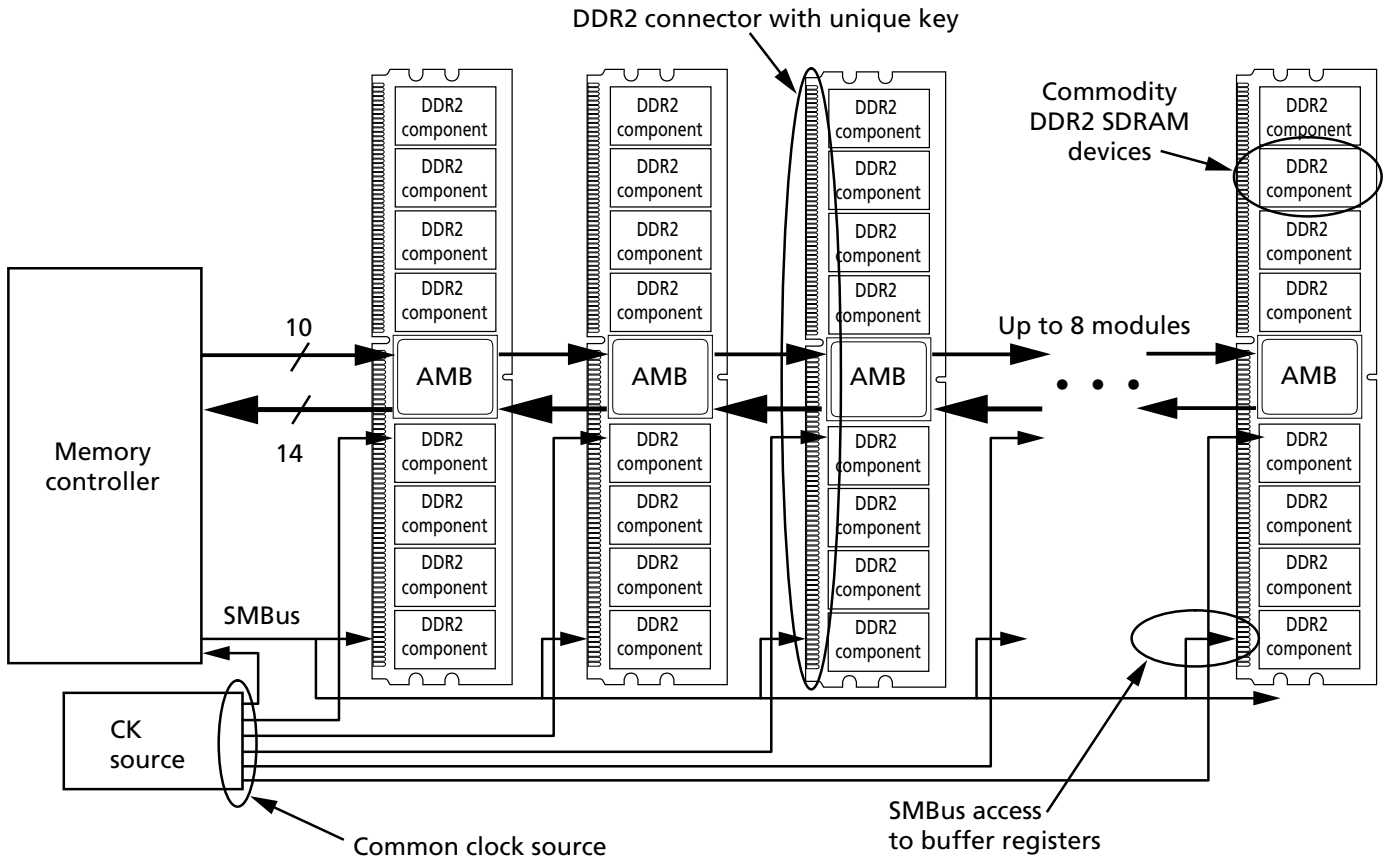
Note: 1. The following signals are cyclical redundancy code (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#.

Table 6: Pin Descriptions

| Symbol | Type | Description |
|--------------------|--------|---|
| PS[9:0] | Input | Primary southbound data, positive lines. |
| PS#[9:0] | Input | Primary southbound data, negative lines. |
| SCK | Input | System clock input, positive line. |
| SCK# | Input | System clock Input, negative line. |
| SCL | Input | Serial presence-detect (SPD) clock input. |
| SS[9:0] | Input | Secondary southbound data, positive lines. |
| SS#[9:0] | Input | Secondary southbound data, negative lines. |
| PN[13:0] | Output | Primary northbound data, positive lines. |
| PN#[13:0] | Output | Primary northbound data, negative lines. |
| SN[13:0] | Output | Secondary northbound data, positive lines. |
| SN#[13:0] | Output | Secondary northbound data, negative lines. |
| SA[2:0] | I/O | SPD address inputs, also used to select the FBDIMM number in the AMB. |
| SDA | I/O | SPD data input/output. |
| RESET# | Supply | AMB reset signal. |
| V _{CC} | Supply | AMB core power and AMB channel interface power (1.5V). |
| V _{DD} | Supply | DRAM power and AMB DRAM I/O power (1.8V). |
| V _{DDSPD} | Supply | SPD/AMB SMBUS power (3.3V). |
| V _{SS} | Supply | Ground. |
| V _{TT} | Supply | DRAM address/command/clock termination power ($V_{DD}/2$). |
| M_Test | – | The M_Test pin provides an external connection for testing the margin of V _{REF} , which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time. |
| DNU | – | Do not use. |

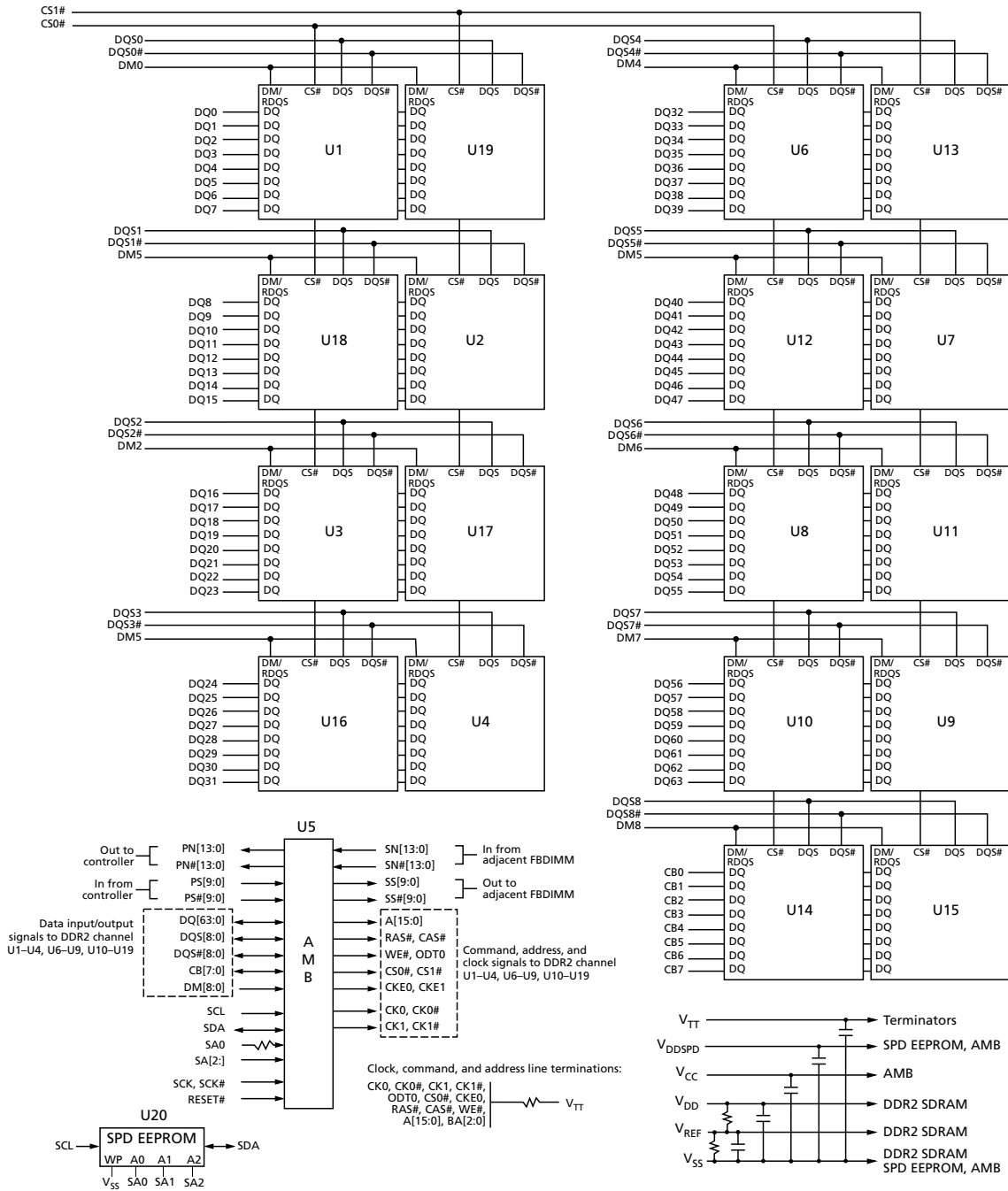
System Block Diagram

Figure 2: System Block Diagram



Functional Block Diagram

Figure 3: Functional Block Diagram



General Description

Micron’s FBDIMM devices adhere to the currently proposed industry specifications for FBDIMMs. The following specifications contain detailed information on FBDIMM design, interfaces, and theory of operation and are listed here for the system designers’ convenience. Refer to the JEDEC Web site for available specifications.

- FBDIMM Design Specification – pending JEDEC approval
- FBDIMM: Architecture and Protocol – JESD206
- FBDIMM: Advanced Memory Buffer (AMB) – JESD82-20
- Design for Test, Design for Validation (DFx) Specification
- Serial Presence-Detect (SPD) for Fully Buffered DIMM – JEDEC Standard No. 21-C, page 4.1.2.7-1

This DDR2 SDRAM module is a high-bandwidth, large-capacity channel solution that has a narrow host interface. FBDIMM devices use DDR2 SDRAM devices isolated from the channel behind an AMB buffer on the FBDIMM. Memory device capacity remains high, and total memory capacity scales with DDR2 SDRAM bit density.

As shown in the System Block Diagram, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enhances the communication path and significantly increases the reliability and availability of the memory subsystem.

Advanced Memory Buffer

The AMB isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged between the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, 1.5V, point-to-point interface. The AMB also enables buffering of memory traffic to support large memory capacities. Refer to the JEDEC JESD82-20 specification for further information.

I_{DD} Conditions and Specifications

Table 7: I_{DD} Conditions

| Symbol | Condition |
|--------------------------|---|
| I _{DD_IDLE_0} | Idle current, single, or last DIMM: L0 state; Idle (0% bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active |
| I _{DD_IDLE_1} | Idle current, first DIMM: L0 state; Idle (0% bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active |
| I _{DD_ACTIVE_1} | Active power: L0 state; 50% DRAM bandwidth; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH |
| I _{DD_ACTIVE_2} | Active power, data pass through: L0 state; 50% DRAM bandwidth to downstream DIMM; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable |



1GB, 2GB (x72, DR) 240-Pin DDR2 SDRAM FBDIMM I_{DD} Conditions and Specifications

Table 7: I_{DD} Conditions (Continued)

| Symbol | Condition |
|--------------------------|---|
| I _{DD_TRAINING} | Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DRAMs idle; 0% bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active |
| I _{DD_IBIST} | IBIST over all IBIST modes: DRAM idle (0% bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active |
| I _{DD_EI} | Electrical idle: DRAM idle (0% bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW |

Note: 1. Actual test conditions may vary from published JEDEC test conditions.

Table 8: I_{DD} Specifications – 1GB DDR2-533

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | 2200 | 3000 | 3400 | 3200 | 3500 | 3800 | 2000 | A |
| I _{DD} | 1420 | 1420 | 2545 | 1420 | 1420 | 1420 | 326 | A |
| Total power | 6.2 | 7.4 | 10.2 | 7.7 | 8.2 | 8.7 | 3.8 | W |

Table 9: I_{DD} Specifications – 1GB DDR2-667

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | 2600 | 3400 | 3900 | 3700 | 4000 | 4500 | 2500 | A |
| I _{DD} | 1510 | 1510 | 2777 | 1510 | 1510 | 1510 | 326 | A |
| Total power | 7.0 | 8.2 | 11.4 | 8.7 | 9.2 | 10.0 | 4.6 | W |

Table 10: I_{DD} Specifications – 1GB DDR2-800

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | TBD | TBD | TBD | TBD | TBD | TBD | TBD | A |
| I _{DD} | TBD | TBD | TBD | TBD | TBD | TBD | TBD | A |
| Total power | TBD | TBD | TBD | TBD | TBD | TBD | TBD | W |

Table 11: I_{DD} Specifications – 2GB DDR2-533

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | 2200 | 3000 | 3400 | 3200 | 3500 | 3800 | 2000 | A |
| I _{DD} | 1420 | 1420 | 2425 | 1420 | 1420 | 1420 | 326 | A |
| Total power | 6.2 | 7.4 | 10.0 | 7.7 | 8.2 | 8.7 | 3.8 | W |

Table 12: I_{DD} Specifications – 2GB DDR2-667

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | 2600 | 3400 | 3900 | 3700 | 4000 | 4500 | 2500 | A |
| I _{DD} | 1420 | 1420 | 2515 | 1420 | 1420 | 1420 | 326 | A |
| Total power | 6.8 | 8.1 | 11.0 | 8.5 | 9.0 | 9.8 | 4.6 | W |

Table 13: I_{DD} Specifications – 12B DDR2-800

| Symbol | I _{DD_IDLE_0} | I _{DD_IDLE_1} | I _{DD_ACTIVE_1} | I _{DD_ACTIVE_2} | I _{DD_TRAINING} | I _{DD_IBIST} | I _{DD_EI} | Units |
|-----------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|-----------------------|--------------------|-------|
| I _{CC} | TBD | TBD | TBD | TBD | TBD | TBD | TBD | A |
| I _{DD} | TBD | TBD | TBD | TBD | TBD | TBD | TBD | A |
| Total power | TBD | TBD | TBD | TBD | TBD | TBD | TBD | W |

Note: 1. Total power is based on maximum voltage levels, I_{CC} at 1.575V and I_{DD} at 1.9V.

Serial Presence-Detect

Table 14: Serial Presence-Detect EEPROM DC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|--------------------|--------------------------|--------------------------|-------|
| EEPROM and AMB supply voltage | V _{DDSPD} | 3 | 3.6 | V |
| Input high voltage: Logic 1; all inputs | V _{IH} | V _{DDSPD} × 0.7 | V _{DDSPD} + 0.5 | V |
| Input low voltage: Logic 0; all inputs | V _{IL} | -0.6 | V _{DDSPD} × 0.3 | V |
| Output low voltage: I _{OUT} = 3mA | V _{OL} | - | 0.4 | V |
| Input leakage current: V _{IN} = GND to V _{DD} | I _{LI} | 0.10 | 3 | μA |
| Output leakage current: V _{OUT} = GND to V _{DD} | I _{LO} | 0.05 | 3 | μA |
| Standby current | I _{SB} | 1.6 | 4 | μA |
| Power supply current, READ: SCL clock frequency = 100 kHz | I _{CCR} | 0.4 | 1 | mA |
| Power supply current, WRITE: SCL clock frequency = 100 kHz | I _{CCW} | 2 | 3 | mA |

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid | t _{AA} | 0.2 | 0.9 | μs | 1 |
| Time the bus must be free before a new transition can start | t _{BUF} | 1.3 | - | μs | |
| Data-out hold time | t _{DH} | 200 | - | ns | |
| SDA and SCL fall time | t _F | - | 300 | ns | 2 |
| Data-in hold time | t _{HD:DAT} | 0 | - | μs | |
| Start condition hold time | t _{HD:STA} | 0.6 | - | μs | |
| Clock HIGH period | t _{HIGH} | 0.6 | - | μs | |
| Noise suppression time constant at SCL, SDA inputs | t _I | - | 50 | ns | |
| Clock LOW period | t _{LOW} | 1.3 | - | μs | |

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions (Continued)

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|----------------------------|---------------------|-----|-----|---------------|-------|
| SDA and SCL rise time | t_R | – | 0.3 | μs | 2 |
| SCL clock frequency | f_{SCL} | – | 400 | kHz | |
| Data-in setup time | $t_{\text{SU:DAT}}$ | 100 | – | ns | |
| Start condition setup time | $t_{\text{SU:STA}}$ | 0.6 | – | μs | 3 |
| Stop condition setup time | $t_{\text{SU:STO}}$ | 0.6 | – | μs | |
| WRITE cycle time | t_{WRC} | – | 10 | ms | 4 |

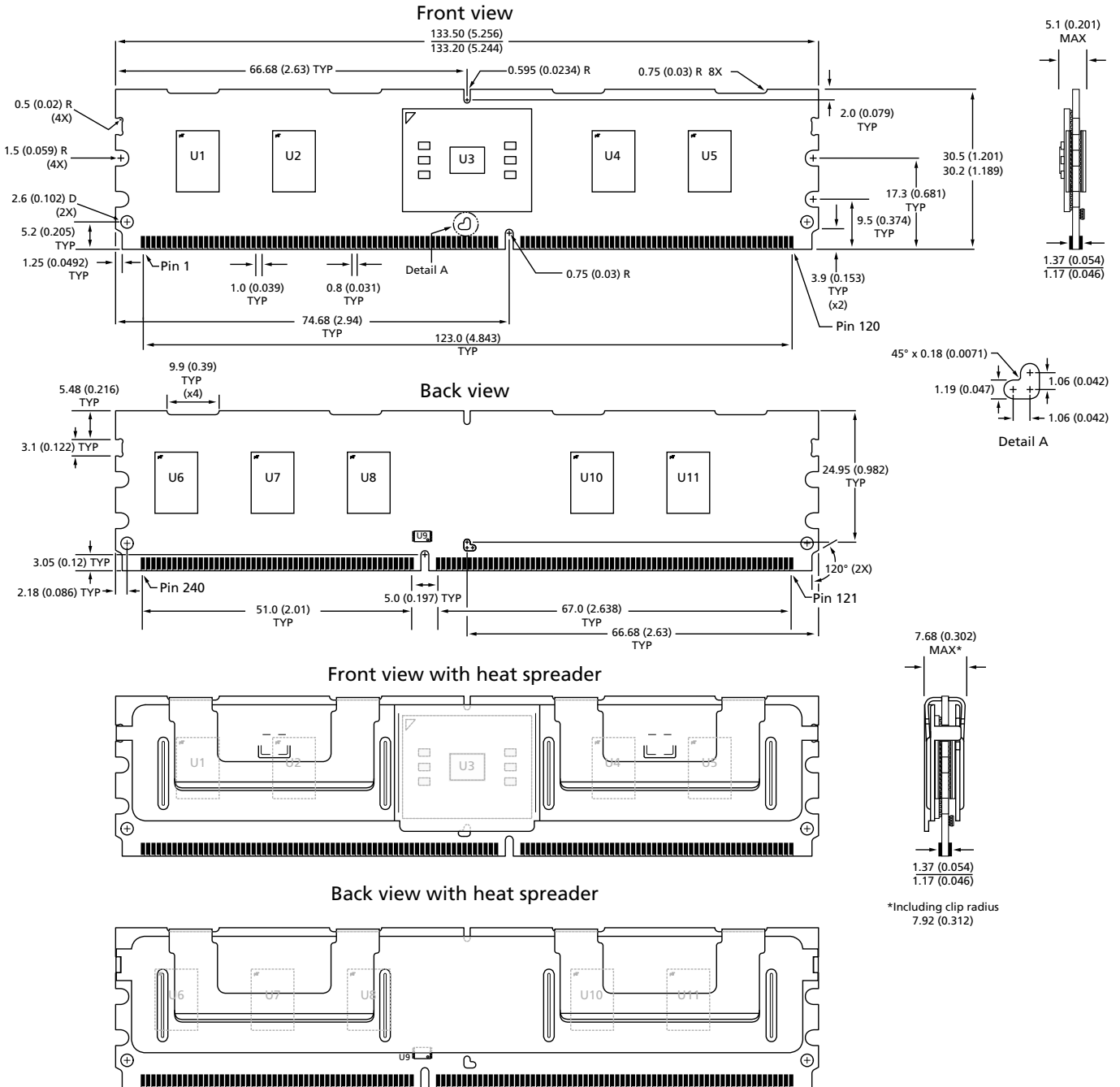
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 4: 240-Pin DDR2 FBDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.



1GB, 2GB (x72, DR) 240-Pin DDR2 SDRAM FBDIMM Module Dimensions

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization some-
times occur.