DDR SDRAM Unbuffered DIMM

MT8VDDT1664A – 128MB

MT8VDDT3264A – 256MB

MT8VDDT6464A – 512MB

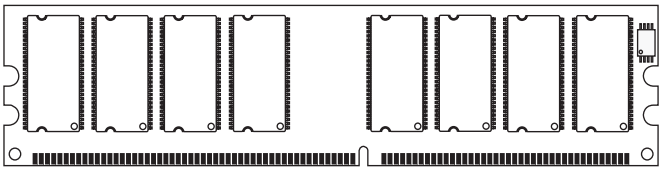
For the component specifications, refer to Micron's Web site: www.micron.com/products/ddrsdram

Features

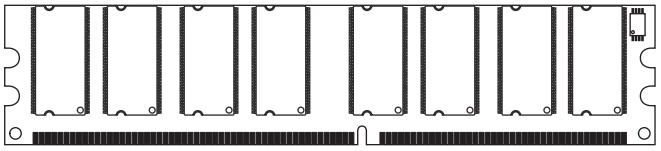
- 184-pin dual in-line memory module (DIMM)
- Fast data transfer rates: PC3200
- Utilizes 400 MT/s DDR SDRAM components
- 128MB (16 Meg x 64), 256MB (32 Meg x 64), and 512MB (64 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +2.6V
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes
- 15.625µs (128MB), 7.8125µs (256MB, 512MB) maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Programmable READ CAS latency
- Single rank
- Gold edge contacts

Figure 1: 184-Pin DIMM (MO-206)

Standard height: 1.25in (31.75mm)



Low-Profile height: 1.125in (28.58mm)



Options	Marking
• Package	
184-pin DIMM (standard)	G
184-pin DIMM (lead-free)[1]	Y
• Memory clock, speed, CL[2]	
5ns (200 MHz), 400 MT/s, CL = 3	-40B
• PCB height	
Standard 1.25in (31.75mm)	See page 2 note
Low-Profile 1.125in (29.21mm)	See page 2 note

Notes: 1. Consult Micron for product availability.
2. CL = CAS (READ) latency.

Table 1: Address Table

	128MB	256MB	512MB
Refresh count	4K	8K	8K
Row addressing	4K (A0–A11)	8K (A0–A12)	8K (A0–A12)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column addressing	1K (A0–A9)	1K (A0–A9)	2K (A0–A9, A11)
Module rank addressing	1 (S0#)	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

Part Number	Module Density	Configuration	Module Bandwith	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT8VDDT1664AG-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT1664AY-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT3264AG-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT3264AY-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT6464AG-40B__	512MB	64 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT6464AY-40B__	512MB	64 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult Micron for current revision codes. Example: MT8VDDT3264AG-40BC3.

Table of Contents

List of Figures

List of Tables

Pin Assignments and Descriptions

Table 3: Pin Assignment

184-Pin DIMM Front								184-Pin DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	24	DQ17	47	DNU	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DNU	163	NC
3	VSS	26	VSS	49	DNU	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DM2	142	DNU	165	DQ52
5	DQS0	28	DQ18	51	DNU	74	VSS	97	DM0	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	CK2#	98	DQ6	121	DQ22	144	DNU	167	NC
7	VDD	30	VDDQ	53	DQ32	76	CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DM6
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	NC	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DM4	172	VDD
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	NC	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	VSS
16	CK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS#	177	DM7
17	CK1#	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	DNU	134	DNU	157	S0#	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	DNU	158	DNU	181	SA0
21	CKE0	44	DNU	67	DQS5	90	NC	113	NC	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	DNU	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115[1]	NC/A12	138	CK0#	161	DQ46	184	VDDSPD

Notes: 1. Pin 115 is “No Connect” for 128MB, “A12” for 256MB and 512MB.

Figure 2: 184-Pin DIMM Pin Locations

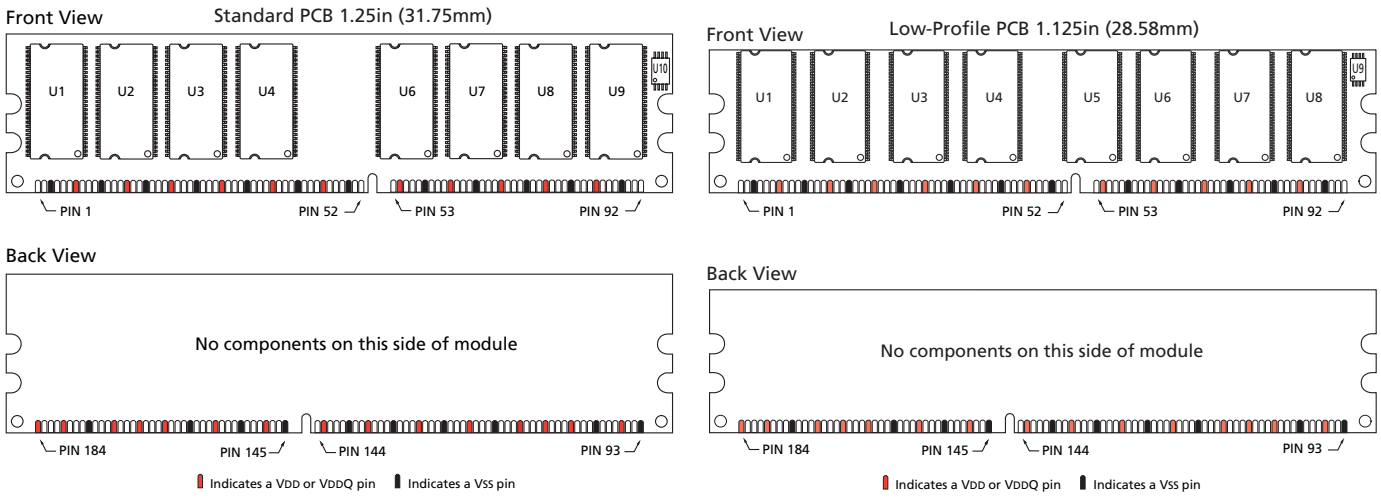


Table 4: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
63, 65, 154	WE#, CAS#, RAS#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21	CKE0	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides precharge power-down and SELF REFRESH operations (all device banks idle), or active power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
157	S0#	Input	Chip selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115 (256MB, 512MB), 118, 122, 125, 130, 141	A0–A11 (128MB) A0–A12 (256MB, 512MB)	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
5, 14, 25, 36, 56, 67, 78, 86	DQS0–DQS7	Input/ Output	Data strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
97, 107, 119, 129, 149, 159, 169, 177	DM0–DM7	Input	Data write mask: DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.

Table 4: Pin Descriptions (Continued)

Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
92	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181,182, 183	SA0–SA2	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
91	SDA	Input/ Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect device.
1	V_{REF}	Supply	SSTL_2 reference voltage.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	Supply	DQ power supply: +2.6V ±0.1V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power supply: +2.6V ±0.1V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
44, 45, 47, 49, 51, 134, 135, 140, 142, 144	DNU	–	Do not use: These pins are not connected on these modules, but are assigned pins on other modules in this product family.
9, 10, 71, 82, 90, 101, 102, 103, 111, 113, 115 (128MB), 158, 163, 167, 173	NC	–	No connect: These pins should be left unconnected.

Functional Block Diagrams

All resistor values are 22Ω unless otherwise specified. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

Standard (lead-containing) modules use the following DDR SDRAM devices: MT46V16M8TG (128MB), MT46V32M8TG (256MB), and MT46V64M8TG (512MB). Lead-free modules use the following DDR SDRAM devices: MT46V16M8TP (128MB), MT46V32M8TP (256MB), and MT46V64M8TP (512MB).

Figure 3: Functional Block Diagram – Standard PCB

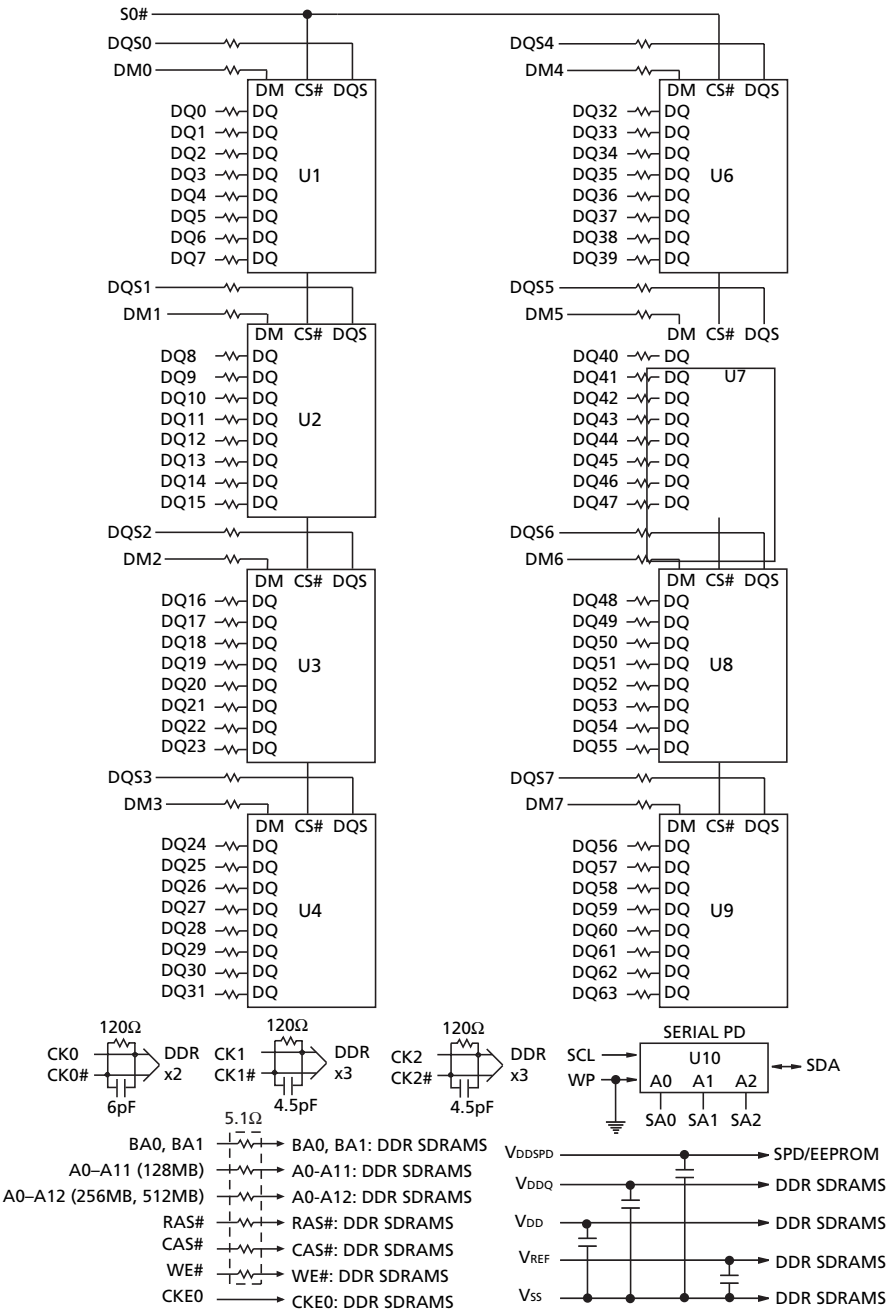
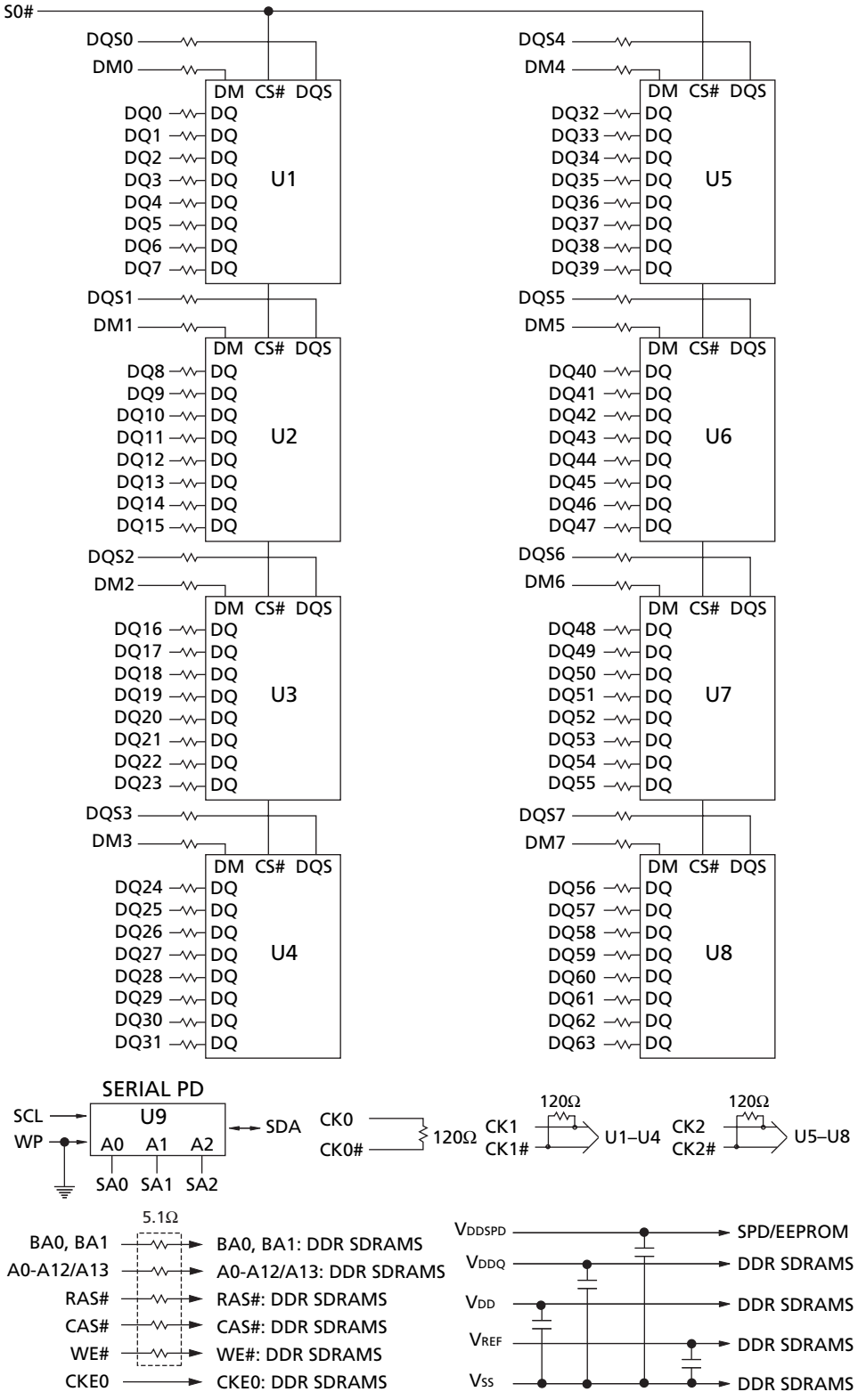


Figure 4: Functional Block Diagram – Low-Profile PCB



General Description

The MT8VDDT1664A, MT8VDDT3264A, and MT8VDDT6464A are high-speed CMOS, dynamic random-access, 128MB, 256MB, and 512MB memory modules organized in a x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from multiple differential clocks (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Table 5: CAS Latency (CL) Table

Speed	Allowable OperatingClock Frequency (MHz)		
	CL = 2	CL = 2.5	CL = 3
-40B	75 ≤ f ≤ 133	75 ≤ f ≤ 133	133 ≤ f ≤ 200

Electrical Specifications

Stresses greater than those listed Figure 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} voltage relative to V_{SS}	–1	3.6	V
V_{DDQ}	V_{DDQ} voltage relative to V_{SS}	–1	3.6	V
V_{REF}	V_{REF} and input voltage relative to V_{SS}	–1	3.6	V
I/O	I/O voltage relative to V_{SS}	–0.5	V_{DDQ} + 0.5V	V
T_A	Operating temperature (ambient)	0	70	°C
T_s	Storage temperature (plastic)	–55	150	°C
	Short circuit output current	–	50	mA

Table 7: DC Electrical Characteristics and Operating Conditions
Notes: 1–5, 13; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.5	2.7	V	19, 22, 31
I/O supply voltage		V_{DDQ}	2.5	2.7	V	19, 22, 23, 31
I/O reference voltage		V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	6, 23
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	7, 23
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	17
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	17
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	CMD/ADDR, RAS#, CAS#, WE#, S#, CKE	I_I	–16	16	µA	29
	CK0, CK0#		–4	4		
	CK1/CK1#, CK2/CK2#		–6	6		
	DM		–2	2		
Output leakage current (DQ disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ, DQS	I_{OZ}	–5	5	µA	29
Output levels: High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	–16.8	–	mA	20, 21
Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA	

Table 8: Capacitance
Note: 11; notes appear on pages 16–18

Parameter	Symbol	Min	Max	Units
Input/Output capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF
Input capacitance: command and address, S#, CKE	C_{I1}	16.0	24.0	pF
Input capacitance: CK0, CK0# (standard PCB)	C_{I2}	10.0	12.0	pF
Input capacitance: CK1, CK1#; CK2, CK2# (standard PCB)	C_{I3}	9.0	12.0	pF

Table 9: IDD Specifications and Conditions – 128MB

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 30; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

Parameter/Condition		Symbol	Max -40B	Units	Notes
Operating current: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	920	mA	14, 25
Operating current: One device bank; Active-Read-Pre-charge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,080	mA	14, 25
PRECHARGE power-down standby current: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P	24	mA	15, 18, 27
Idle standby current: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	400	mA	28
ACTIVE power-down standby current: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	200	mA	15, 18, 27
ACTIVE standby current: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	400	mA	14, 24
Operating current: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,080	mA	14, 25
Operating current: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,240	mA	14
AUTO REFRESH current	tREFC = tRFC (MIN)	IDD5	1,920	mA	14, 27
	tREFC = 15.625µs	IDD5A	48	mA	16, 27
SELF REFRESH current: CKE ≤ 0.2V		IDD6	32	mA	9
Operating current: Four device bank interleaving READs (BL= 4) with auto precharge,tRC = MIN tRC allowed; tCK = tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		IDD7	2,840	mA	14, 26

Table 10: IDD Specifications and Conditions – 256MB

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 30; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

Parameter/Condition		Symbol	Max -40B	Units	Notes
Operating current: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,080	mA	14, 25
Operating current: One device bank; Active-Read-Pre-charge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,360	mA	14, 25
PRECHARGE power-down standby current: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P	32	mA	15, 18, 27
Idle standby current: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	480	mA	28
ACTIVE power-down standby current: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	320	mA	15, 18, 27
ACTIVE standby current: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	560	mA	14, 24
Operating current: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,600	mA	14, 25
Operating current: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,560	mA	14
AUTO REFRESH current	tREFC = tRFC (MIN)	IDD5	2,080	mA	14, 27
	tREFC = 7.8125µs	IDD5A	48	mA	16, 27
SELF REFRESH current: CKE ≤ 0.2V		IDD6	32	mA	9
Operating current: Four device bank interleaving READs (BL= 4) with auto precharge,tRC = MIN tRC allowed; tCK = tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		IDD7	3,760	mA	14, 26

Table 11: IDD Specifications and Conditions – 512MB

DDR SDRAM components only

Notes: 1–5, 8, 10, 12, 30; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

Parameter/Condition		Symbol	Max -40B	Units	Notes
Operating current: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,240	mA	14, 25
Operating current: One device bank; Active-Read-Pre-charge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,480	mA	14, 25
PRECHARGE power-down standby current: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P	40	mA	15, 18, 27
Idle standby current: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	440	mA	18
ACTIVE power-down standby current: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	360	mA	15, 18, 27
ACTIVE standby current: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	440	mA	24
Operating current: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,520	mA	14, 25
Operating current: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,560	mA	14
AUTO REFRESH current	tREFC = tRFC (MIN)	IDD5	2,760	mA	14, 27
	tREFC = 7.8125µs	IDD5A	88	mA	16, 27
SELF REFRESH current: CKE ≤ 0.2V		IDD6	40	mA	9
Operating current: Four device bank interleaving READs (BL= 4) with auto precharge,tRC = MIN tRC allowed; tCK = tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		IDD7	3,600	mA	14, 26

AC Operating Specifications

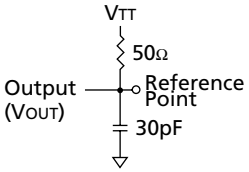
Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site: www.micron.com/products/ddrsdram. Module speed grades correlate with component speed grades as shown in the following table:

Table 12: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-40B	-5

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. From $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise, measured at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 for -40B with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.6V ±0.1V, $V_{DD}Q$ = +2.6V ±0.1V, V_{REF} = Vss, f = 100 MHz, T_A = 25°C, $V_{OUT}(DC) = V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates <1 V/ns and greater ≥0.5 V/ns. If slew rate is <0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from 500mV/ns, while ^{t}IH is unaffected. If slew rate exceeds 4.5 V/ns, functionality is uncertain. For -40B, slew rates must be ≥0.5 V/ns.
13. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 × $V_{DD}Q$ is recognized as LOW.
14. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
15. The refresh period is 64ms. This equates to an average refresh rate of 15.625µs (128MB), or 7.8125µs (256MB, 512MB). However, an AUTO REFRESH command must be asserted at least once every 140.6µs (128MB) or 70.3µs (256MB, 512MB); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.

16. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
17. To maintain a valid level, the transitioning edge of the input must:
    17a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
    17b. Reach at least the target AC level.
    17c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
18. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
19. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +300mV or 2.9V, whichever is less. Any negative glitch must be <1/3 of the clock cycle and not exceed either -200mV or 2.4V, whichever is more positive.
20. Normal Output Drive Curves:
    20a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 5.
    20b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 5.
    20c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 6 on page 18.
    20d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 6 on page 18.
    20e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    20f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 5: Pull-Down Characteristics

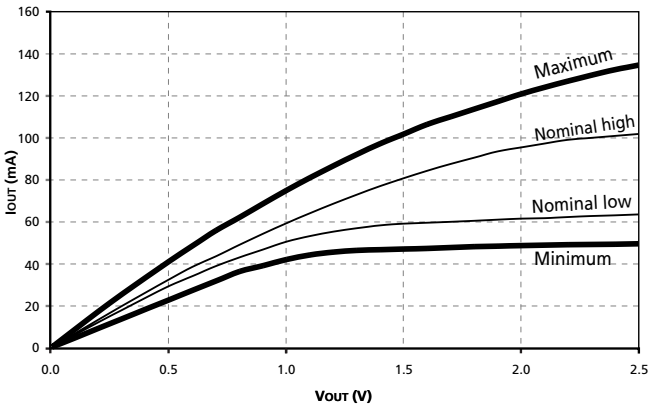
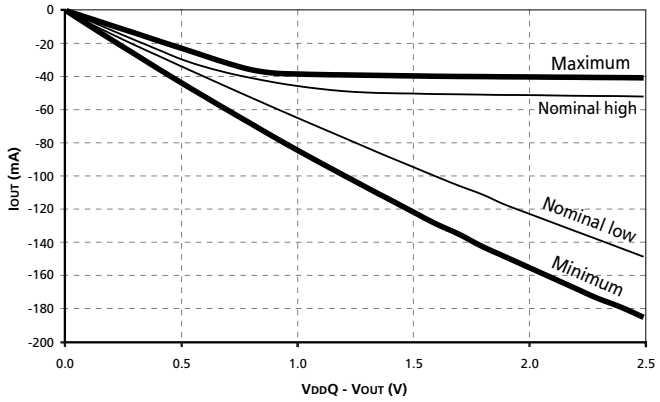


Figure 6: Pull-Up Characteristics



21. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
22. VDD and VDDQ must track each other.
23. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.
24. For -40B modules, IDD3N is specified to be 35mA per DDR SDRAM device at 100 MHz.
25. Random addressing changing and 50 percent of data changing at every transfer.
26. Random addressing changing and 100 percent of data changing at every transfer.
27. CKE must be active (HIGH) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC has been satisfied.
28. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
29. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
30. When an input signal is HIGH or LOW, it is defined as a steady state logic high or low.
31. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM device generated from any source other than that of the DRAM itself may not exceed the DC voltage range of 2.6V ±100mV.

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7 and Figure 8 on page 20).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 9 on page 20).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 7: Data Validity

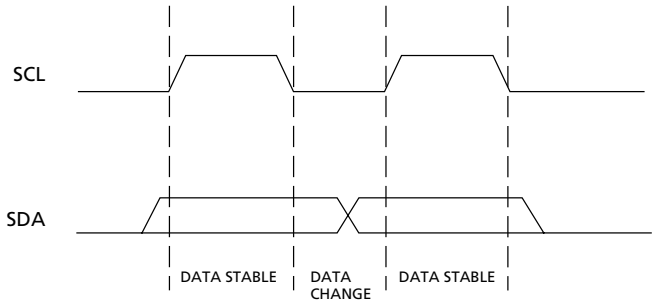


Figure 8: Definition of Start and Stop

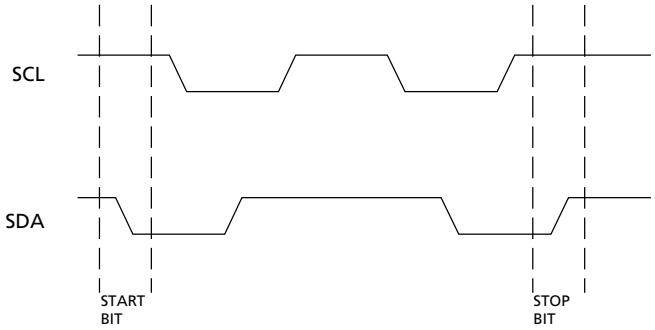


Figure 9: Acknowledge Response From Receiver

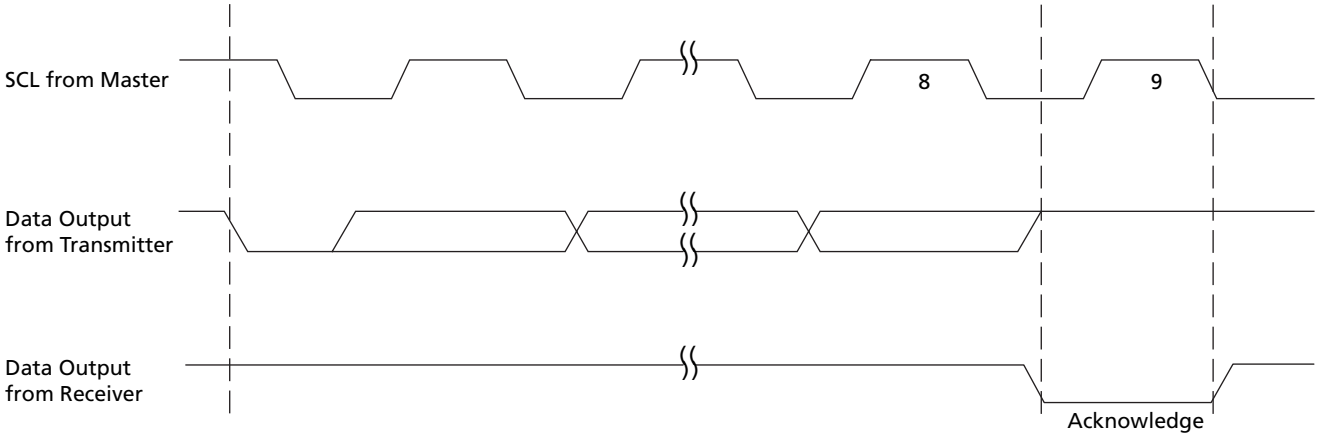


Table 13: EEPROM Device Select Code
Most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection register select code	0	1	1	0	SA2	SA1	SA0	RW

Table 14: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	START, device select, RW = "1"
Random address read	0	VIH or VIL	1	START, device select, RW = "0", address
	1	VIH or VIL	1	reSTART, device select, RW = "1"
Sequential read	1	VIH or VIL	≥ 1	Similar to current or random address read
Byte write	0	VIL	1	START, device select, RW = "0"
Page write	0	VIL	≤ 16	START, device select, RW = "0"

Figure 10: SPD EEPROM Timing Diagram

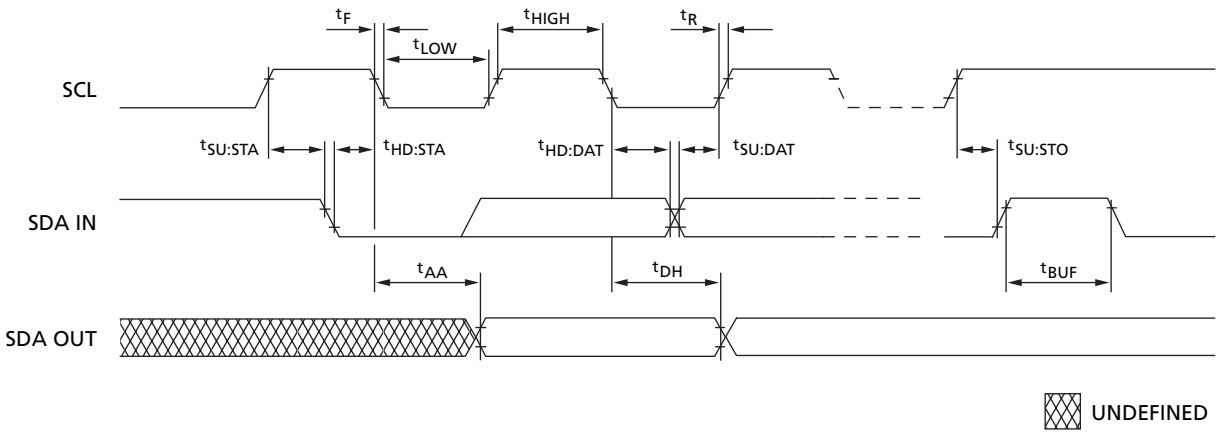


Table 15: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	Vih	$V_{DDSPD} \times 0.7$	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1	$V_{DDSPD} \times 0.3$	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{DD} or V_{SS}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 17: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT8VDDT1664A	MT8VDDT3264A	MT8VDDT6464A
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	SDRAM DDR	07	07	07
3	Number of row addresses on assembly	12 or 13	0C	0D	0D
4	Number of column addresses on assembly	10 or 11	0A	0A	0B
5	Number of ranks on DIMM	1	01	01	01
6	Module data width	64	40	40	40
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	SSTL 2.5V	04	04	04
9	DDR cycle time, ^{t}CK, (CL = 3)	5ns (-40B)	50	50	50
10	DDR access from clock, ^{t}AC, (CL = 3)	0.7 (-40B)	70	70	70
11	Module configuration type	Unbuffered	00	00	00
12	Refresh rate/type	15.6, 7.81µs/SELF	80	82	82
13	DDR device width (primary DDR)	8	08	08	08
14	Error-checking DDR data width	None	00	00	00
15	MIN clock delay, back-to-back random column access	1 clock	01	01	01
16	Burst lengths supported	2, 4, 8	0E	0E	0E
17	Number of banks on SDRAM device	4	04	04	04
18	CAS latencies supported	3, 2.5, 2	1C	1C	1C
19	CS latency	0	01	01	01
20	WE latency	1	02	02	02
21	DDR module attributes	Unbuffered	20	20	20
22	DDR device attributes: general	Fast/Concurrent auto precharge	C0	C0	C0
23	DDR cycle time, ^{t}CK (CL = 2.5)	6ns (for PC2700 compat.)	60	60	60
24	DDR access from CK, ^{t}AC (CL = 2.5)	0.7ns (for PC2700 compat.)	70	70	70
25	DDR cycle time, ^{t}CK, (CLy = 2)	7.5ns (PC2100, PC1600)	75	75	75
26	DDR access from CK, ^{t}AC, (CL = 2)	0.75ns (PC2100, PC1600)	75	75	75
27	MIN row precharge time, ^{t}RP	15ns (-40B)	3C	3C	3C
28	MIN row active-to-row active, ^{t}RRD	10ns (-40B)	28	28	28
29	MIN RAS#-to-CAS# delay, ^{t}RCD	15ns (-40B)	3C	3C	3C
30	MIN RAS# pulse width, ^{t}RAS	40ns (-40B)	28	28	28
31	Module rank density	128MB, 256MB or 512MB	20	40	80
32	Address and command setup time, ^{t}IS	0.6ns (-40B)	60	60	60
33	Address and command hold time, ^{t}IH	0.6ns (-40B)	60	60	60
34	Data/Data mask input setup time, ^{t}DS	0.4ns (-40B)	40	40	40
35	Data/Data mask input hold time, ^{t}DH	0.4ns (-40B)	40	40	40
36-40	Reserved		00	00	00

Table 17: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT8VDDT1664A	MT8VDDT3264A	MT8VDDT6464A
41	MIN ACTIVE/AUTO REFRESH time, ^{t}RC	55ns (-40B)	37	37	37
42	MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period, ^{t}RFC	70ns (-40B)	46	46	46
43	MAX cycle time, ^{t}CK (MAX)	12ns (-40B)	30	30	30
44	MAX DQS-DQ skew time, ^{t}DQSQ	0.4ns (-40B)	28	28	28
45	MAX read data hold skew factor, ^{t}QHS	0.5ns (-40B)	50	50	50
46	Reserved		00	00	00
47	DIMM height	Standard/Low-Profile	01/11	01/11	01/11
48–61	Reserved		00	00	00
62	SPD revision	Release 1.1	11	11	11
63	Checksum for bytes 0–62	-40B	5D/6D	80/90	C1/D1
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code	(Continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73-90	Module part number (ASCII)		Variable Data	Variable Data	Variable Data
91	PCB identification code		Variable Data	Variable Data	Variable Data
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable Data	Variable Data	Variable Data
94	Week of manufacture in BCD		Variable Data	Variable Data	Variable Data
95-98	Module serial number		Variable Data	Variable Data	Variable Data
99-127	Manufacturer-Specific data (RSVD)		–	–	–

Package Dimensions

All dimensions in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 11: 184-Pin DIMM Dimensions – Standard PCB

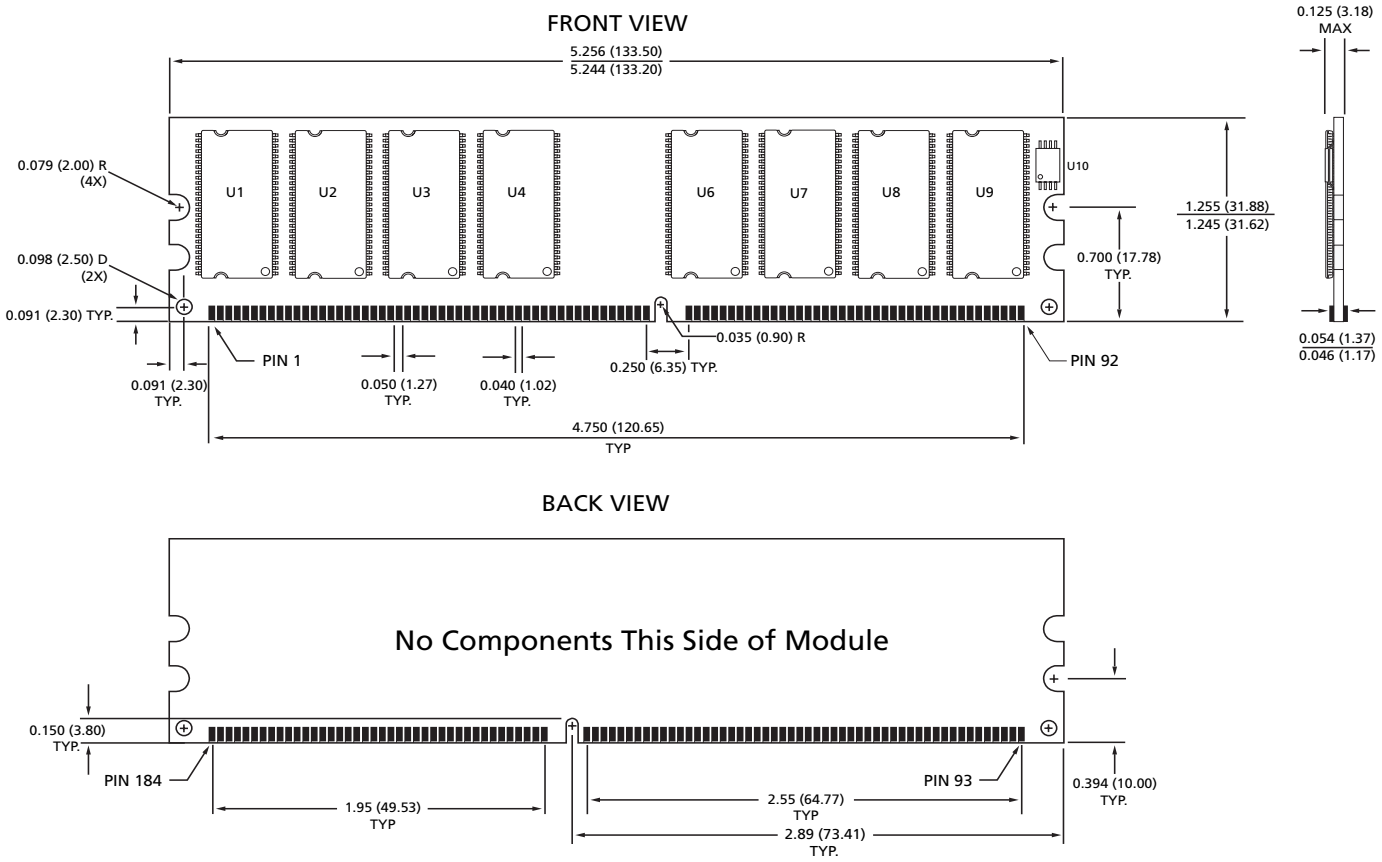
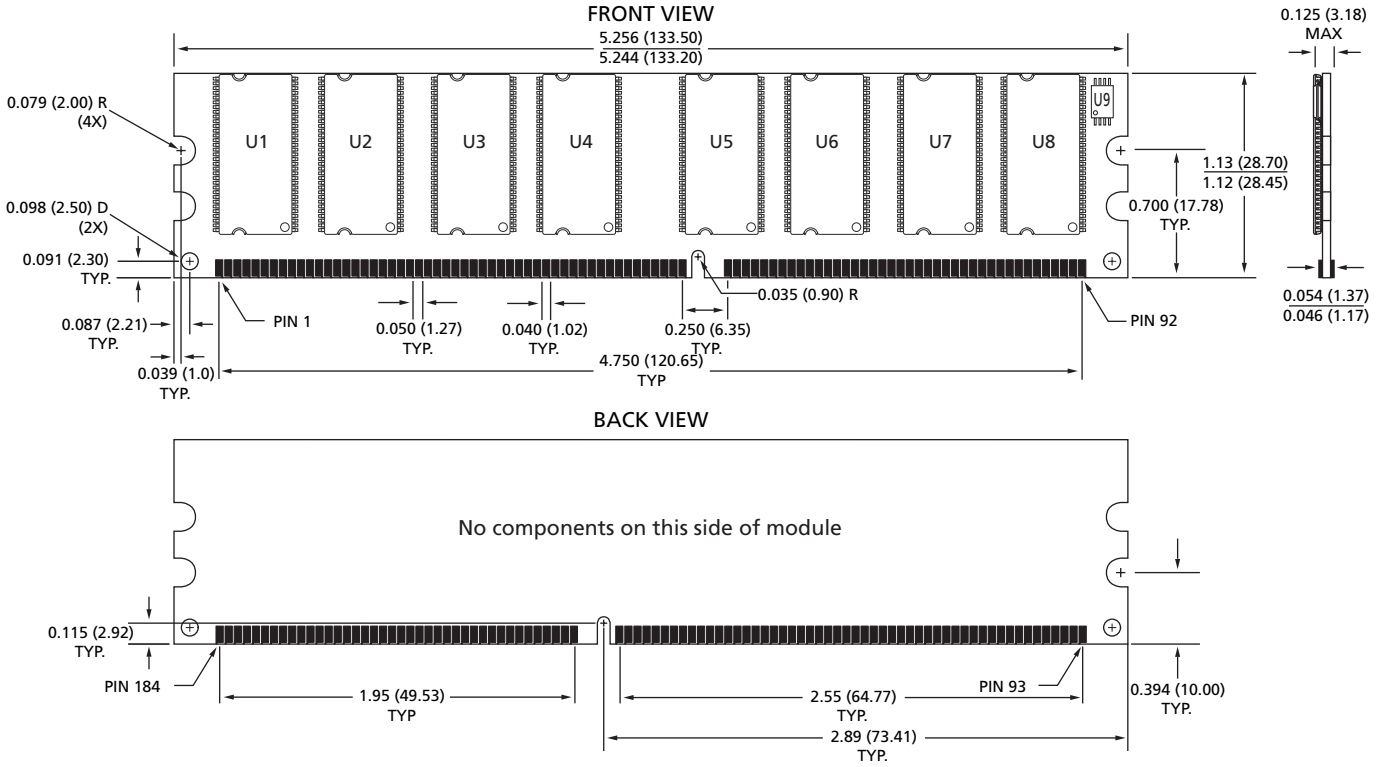


Figure 12: 184-Pin DIMM Dimensions – Low-Profile PCB



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992