TH58NS512DC

TENTATIVE  TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT  SILICON GATE CMOS

512-MBIT (64M × 8 BITS) CMOS NAND E²PROM (64M BYTE SmartMedia™)

DESCRIPTION

The TH58NS512 is a single 3.3-V 512-Mbit (553,648,128) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as 528 bytes × 32 pages × 4096 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages).

The TH58NS512 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed.

The TH58NS512DC is a SmartMedia™ with ID and each device has 128 bit unique ID number embedded in the device. This unique ID number is applicable to image files, music files, electronic books, and so on where copyright protection is required.

The data stored in the TH58NS512DC needs to comply with the data format standardized by the SSFDC Forum in order to maintain compatibility with other SmartMedia™ systems.

FEATURES

- **Organization**
  - Memory cell array: 528 × 64K × 8 × 2
  - Register: 528 × 8
  - Page size: 528 bytes
  - Block size: (16K + 512) bytes
- **Modes**
  - Read, Reset, Auto Page Program,
  - Auto Block Erase, Status Read
- **Mode control**
  - Serial input/output, Command control
- **Complies with the SmartMedia™ Electrical Specification and Data Format Specification issued by the SSFDC Forum**
- **Power supply**
  - \( V_{CC} = 3.3 \, \text{V} \pm 0.3 \, \text{V} \)
- **Access time**
  - Cell array-register: 25 \( \mu \text{s} \) max
  - Serial Read cycle: 80 ns min
- **Operating current**
  - Read (80-ns cycle): 10 mA typ.
  - Program (avg.): 10 mA typ.
  - Erase (avg.): 10 mA typ.
  - Standby: 100 \( \mu \text{A} \) max
- **Packages**
  - TH58NS512DC: FDC-22C (Weight: 2.2 g typ.)

PIN ASSIGNMENT (TOP VIEW)

PIN NAMES

<table>
<thead>
<tr>
<th>I/O1~I/O8</th>
<th>I/O port</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
<td>Chip enable</td>
</tr>
<tr>
<td>WE</td>
<td>Write enable</td>
</tr>
<tr>
<td>RE</td>
<td>Read enable</td>
</tr>
<tr>
<td>CLE</td>
<td>Command latch enable</td>
</tr>
<tr>
<td>ALE</td>
<td>Address latch enable</td>
</tr>
<tr>
<td>WP</td>
<td>Write protect</td>
</tr>
<tr>
<td>BY/RY</td>
<td>Ready/Busy</td>
</tr>
<tr>
<td>GND</td>
<td>Ground Input</td>
</tr>
<tr>
<td>LVD</td>
<td>Low Voltage Detect</td>
</tr>
<tr>
<td>VCC</td>
<td>Power supply</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
</tbody>
</table>

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2000-08-27  1/33
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power Supply Voltage</td>
<td>−0.6~4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input Voltage</td>
<td>−0.6~4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Input/Output Voltage</td>
<td>−0.6 V~VCC + 0.3 V (≤ 4.6 V)</td>
<td>V</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation</td>
<td>0.3</td>
<td>W</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature</td>
<td>−20~65</td>
<td>°C</td>
</tr>
<tr>
<td>Topr</td>
<td>Operating Temperature</td>
<td>0~55</td>
<td>°C</td>
</tr>
</tbody>
</table>

CAPACITANCE *(Ta = 25°C, f = 1 MHz)*

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 0 V</td>
<td>—</td>
<td>50</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; = 0 V</td>
<td>—</td>
<td>50</td>
<td>pF</td>
</tr>
</tbody>
</table>

* This parameter is periodically sampled and is not tested for every device.

TOSHIBA CORPORATION reserves the right to make changes without further notice.

000707EBAZ

2000-08-27 2/33
VALID BLOCKS (1)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVB</td>
<td>Number of Valid Blocks</td>
<td>4016</td>
<td>—</td>
<td>4096</td>
<td>Blocks</td>
</tr>
</tbody>
</table>

(1) The TH58NS512 occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

RECOMMENDED DC OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Power Supply Voltage</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td>2</td>
<td>—</td>
<td>VCC + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>−0.3*</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

* −2 V (pulse width ≤ 20 ns)

DC CHARACTERISTICS (Ta = 0°C~55°C, VCC = 3.3 V ± 0.3 V)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IIL</td>
<td>Input Leakage Current</td>
<td>V IN = 0 V~VCC</td>
<td>—</td>
<td>—</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>VOUT = 0.4 V~VCC</td>
<td>—</td>
<td>—</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>ICCO1</td>
<td>Operating Current (Serial Read)</td>
<td>CE = VIL, IOUT = 0 mA, t cycle = 80 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO3</td>
<td>Operating Current (Command Input)</td>
<td>t cycle = 80 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO4</td>
<td>Operating Current (Data Input)</td>
<td>t cycle = 80 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO5</td>
<td>Operating Current (Address Input)</td>
<td>t cycle = 80 ns</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO7</td>
<td>Programming Current</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCO6</td>
<td>Erasing Current</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>ICCS1</td>
<td>Standby Current</td>
<td>CE = VIH</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>ICCS2</td>
<td>Standby Current</td>
<td>CE = VCC − 0.2 V</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>IOH = −400 µA</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>IOL = 2.1 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>IO (RY/BY)</td>
<td>Output Current of RY/BY Pin</td>
<td>VOL = 0.4 V</td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>mA</td>
</tr>
</tbody>
</table>
### AC CHARACTERISTICS AND OPERATING CONDITIONS

**(Ta = 0°C~55°C, VCC = 3.3 V ± 0.3 V)**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCLS</td>
<td>CLE Setup Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCLH</td>
<td>CLE Hold Time</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCS</td>
<td>CE Setup Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCH</td>
<td>CE Hold Time</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tALS</td>
<td>ALE Setup Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tALH</td>
<td>ALE Hold Time</td>
<td>40</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>80</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWH</td>
<td>WE -High Hold Time</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWR</td>
<td>Read Pulse Width</td>
<td>60</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>80</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tREA</td>
<td>RE Access Time (Serial Data Access)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCEH</td>
<td>CE -High Time for Last Address in Serial Read Cycle</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td>(2)</td>
</tr>
<tr>
<td>tREAD</td>
<td>RE Access Time (ID Read)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tOH</td>
<td>Data Output Hold Time</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tOHZ</td>
<td>RE -High-to-Output-High Impedance</td>
<td>—</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCHZ</td>
<td>CE -High-to-Output-High Impedance</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tREH</td>
<td>RE -High Hold Time</td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tIR</td>
<td>Output-High-Impedance-to-RE Rising Edge</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRSTO</td>
<td>RE Access Time (Status Read)</td>
<td>—</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCSTO</td>
<td>CE Access Time (Status Read)</td>
<td>—</td>
<td>55</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRW</td>
<td>RE High to WE Low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWCH</td>
<td>WE High to CE Low</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWR</td>
<td>WE High to RE Low</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAR1</td>
<td>ALE Low to RE Low (ID Read)</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCR</td>
<td>CE Low to RE Low (ID Read)</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tB</td>
<td>Memory Cell Array to Starting Address</td>
<td>—</td>
<td>25</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>tWB</td>
<td>WE High to Busy</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAR2</td>
<td>ALE Low to RE Low (Read Cycle)</td>
<td>50</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRB</td>
<td>RE Last Clock Rising Edge to Busy (in Sequential Read)</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tCRY</td>
<td>CE High to Ready (When interrupted by CE in Read Mode)</td>
<td>—</td>
<td>600 + tB (RY/RY)</td>
<td>ns</td>
<td>(1)</td>
</tr>
<tr>
<td>tRST</td>
<td>Device Reset Time (Read/Program/Erase)</td>
<td>—</td>
<td>6/10/500</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

### AC TEST CONDITIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input level</td>
<td>2.4 V, 0.4 V</td>
</tr>
<tr>
<td>Input pulse rise and fall time</td>
<td>3 ns</td>
</tr>
<tr>
<td>Input comparison level</td>
<td>1.5 V, 1.5 V</td>
</tr>
<tr>
<td>Output data comparison level</td>
<td>1.5 V, 1.5 V</td>
</tr>
<tr>
<td>Output load</td>
<td>( C_L ) (100 pF) + 1 TTL</td>
</tr>
</tbody>
</table>
Notes:
(1)  **CE** High to Ready time depends on the pull-up resistor tied to the **RY/BY** pin.
     (Refer to Application Note (7) toward the end of this document.)

(2) Sequential Read is terminated when \( t_{CEH} \) is greater than or equal to 100 ns.
    If the **RE** to **CE** delay is less than 30 ns, **RY/BY** signal stays Ready.

![Diagram](image)

**PROGRAMMING AND ERASING CHARACTERISTICS**

\( (Ta = 0^\circ\text{C} \sim 55^\circ\text{C}, \ V_{CC} = 3.3 \ \text{V} \pm 0.3 \ \text{V}) \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPROG</td>
<td>Programming Time</td>
<td>—</td>
<td>200</td>
<td>1000</td>
<td>( \mu\text{s} )</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>Number of Programming Cycles on Same Page</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td></td>
<td>(1)</td>
</tr>
<tr>
<td>tERASE</td>
<td>Block Erasing Time</td>
<td>—</td>
<td>3</td>
<td>4</td>
<td>( \text{ms} )</td>
<td></td>
</tr>
<tr>
<td>P/E</td>
<td>Number of Program/Erase Cycles</td>
<td>—</td>
<td>—</td>
<td>( 2.5 \times 10^5 )</td>
<td></td>
<td>(2)</td>
</tr>
</tbody>
</table>

(1) Refer to Application Note (12) toward the end of this document.
(2) Refer to Application Note (15) toward the end of this document.
TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data

Command Input Cycle Timing Diagram

\[\text{CLE, ALE, CE, RE}\]

- Setup time: \(t_{DS}\)
- Hold time: \(t_{DH}\)
- \(\text{I/O1 to I/O8}\): VIH or VIL

\[\overline{\text{CE}}\]

- \(t_{WP}\)
- \(t_{ALS}\)
- \(t_{ALH}\)

\[\overline{\text{WE}}\]

- \(t_{CS}\)
- \(t_{CLH}\)

\[\text{CLE}\]

- \(t_{CLS}\)
- \(t_{CLH}\)

\[\text{I/O1 to I/O8}\]

\[\overline{\text{I/O8}}\]

\[\text{CLE, ALE, CE, RE}\]

\[\overline{\text{CE}}\]

- \(t_{WP}\)
- \(t_{ALS}\)
- \(t_{ALH}\)

\[\overline{\text{WE}}\]

- \(t_{CS}\)
- \(t_{CLH}\)

\[\text{CLE}\]

- \(t_{CLS}\)
- \(t_{CLH}\)

\[\text{I/O1 to I/O8}\]

\[\overline{\text{I/O8}}\]

\[\text{CLE, ALE, CE, RE}\]

\[\overline{\text{CE}}\]

- \(t_{WP}\)
- \(t_{ALS}\)
- \(t_{ALH}\)

\[\overline{\text{WE}}\]

- \(t_{CS}\)
- \(t_{CLH}\)

\[\text{CLE}\]

- \(t_{CLS}\)
- \(t_{CLH}\)

\[\text{I/O1 to I/O8}\]

\[\overline{\text{I/O8}}\]

\[\text{CLE, ALE, CE, RE}\]

\[\overline{\text{CE}}\]

- \(t_{WP}\)
- \(t_{ALS}\)
- \(t_{ALH}\)

\[\overline{\text{WE}}\]

- \(t_{CS}\)
- \(t_{CLH}\)

\[\text{CLE}\]

- \(t_{CLS}\)
- \(t_{CLH}\)

\[\text{I/O1 to I/O8}\]

\[\overline{\text{I/O8}}\]
Address Input Cycle Timing Diagram

Data Input Cycle Timing Diagram
Serial Read Cycle Timing Diagram

Status Read Cycle Timing Diagram

* 70H represents the hexadecimal number 70.

: $V_{IH}$ or $V_{IL}$
Read Cycle (1) Timing Diagram

Read Cycle (1) Timing Diagram: When Interrupted by CE

* Read Operation using 00H Command  N: 0~255

: V_H or V_L
Read Cycle (2) Timing Diagram

Read Operation using 01H Command  N: 0–255

Read Cycle (3) Timing Diagram

Read Operation using 50H Command  N: 0–15
Sequential Read (3) Timing Diagram

CLE

CE

WE

ALE

RE

I/O1

I/O8

Column address
N

A0 - A7

A9 - A16

A17 - A24

A25

Page address
M

Page M access

Page M + 1 access

512 + N

512 + N + 1

512 + N + 2

512

513

514

527

527

527

Vih or Vil

RY/BY
Auto-Program Operation Timing Diagram

Auto Block Erase Timing Diagram
ID Read Operation Timing Diagram

CLE

CE

WE

ALE

RE

I/O1

- I/O8

90H

00

98H

76H

A5H

Address input

Maker code

Device code

Option code

\[ \text{V}_{\text{IH}} \text{ or } \text{V}_{\text{IL}} \]
PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of WE if ALE is High. Input data is latched if ALE is Low.

Chip Enable: CE

The device goes into a low-power Standby mode when CE goes High during a Read operation. The CE signal is ignored when device is in Busy state (RY/BY = L), such as during a Program or Erase operation, and will not enter Standby mode even if the CE input goes High. The CE signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

Write Enable: WE

The WE signal is used to control the acquisition of data from the I/O port.

Read Enable: RE

The RE signal controls serial data output. Data is available to A after the falling edge of RE. The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1~I/O8

The I/O1 to I/O8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: WP

The WP signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WP is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY/BY

The RY/BY output signal is used to indicate the operating condition of the device. The RY/BY signal is in Busy state (RY/BY = L) during the Program, Erase and Read operations and will return to Ready state (RY/BY = H) after completion of the operation. The output buffer for this signal is an open drain.

Low Voltage Detect: LVD

The LVD signal is used to detect the power supply voltage level.
Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 32 pages = (16K + 512) bytes
Capacity = 528 bytes × 32 pages × 4096 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

<table>
<thead>
<tr>
<th>I/O8</th>
<th>I/O7</th>
<th>I/O6</th>
<th>I/O5</th>
<th>I/O4</th>
<th>I/O3</th>
<th>I/O2</th>
<th>I/O1</th>
<th>A0~A7: Column address</th>
<th>A9~A25: Page address</th>
<th>A14~A25: Block address</th>
<th>A9~A13: NAND address in block</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A8</td>
<td>*</td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>First cycle</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Second cycle</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A11</td>
<td>A10</td>
<td>A9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Third cycle</td>
<td>A24</td>
<td>A23</td>
<td>A22</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*: A8 is automatically set to Low or High by a 00H command or a 01H command.
*: I/O2~I/O8 must be set to Low in the fourth cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, CE, WE, RE and WP signals, as shown in Table 2.

Table 2. Logic table

<table>
<thead>
<tr>
<th></th>
<th>CLE</th>
<th>ALE</th>
<th>CE</th>
<th>WE</th>
<th>RE</th>
<th>WP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command Input</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>Data Input</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td></td>
<td>H</td>
<td>*</td>
</tr>
<tr>
<td>Address Input</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H</td>
<td>*</td>
</tr>
<tr>
<td>Serial Data</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>During Programming (Busy)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>During Erasing (Busy)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>Program, Erase Inhibit</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>L</td>
</tr>
</tbody>
</table>

H: VIH, L: VIL. *: VISH or VIL
Table 3. Command table (HEX)

<table>
<thead>
<tr>
<th>Command</th>
<th>First Cycle</th>
<th>Second Cycle</th>
<th>Acceptable while Busy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Data Input</td>
<td>80</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (1)</td>
<td>00</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (2)</td>
<td>01</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Read Mode (3)</td>
<td>50</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>FF</td>
<td>—</td>
<td>○</td>
</tr>
<tr>
<td>Auto Program</td>
<td>10</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Auto Block Erase</td>
<td>60</td>
<td>D0</td>
<td></td>
</tr>
<tr>
<td>Status Read</td>
<td>70</td>
<td>—</td>
<td>○</td>
</tr>
<tr>
<td>ID Read</td>
<td>90</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

Once the device has been set to Read mode by a 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

<table>
<thead>
<tr>
<th></th>
<th>CLE</th>
<th>ALE</th>
<th>CE</th>
<th>WE</th>
<th>RE</th>
<th>I/O1~I/O8</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Select</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Data output</td>
<td>Active</td>
</tr>
<tr>
<td>Output Deselect</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>High impedance</td>
<td>Active</td>
</tr>
<tr>
<td>Standby</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>*</td>
<td>High impedance</td>
<td>Standby</td>
</tr>
</tbody>
</table>

H: $V_{IH}$, L: $V_{IL}$, *: $V_{IH}$ or $V_{IL}$

HEX data bit assignment (Example)

Serial data input: 80H

```
1 0 0 0 0 0 0 0
I/O8 7 6 5 4 3 2 1/O1
```
DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.

A data transfer operation from the cell array to the register starts on the rising edge of WE in the fourth cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The CE signal must stay Low after the fourth address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start pointer designated in the address input cycle.

Read Mode (2)

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

However, for a Sequential Read, output of the next page starts from column address 0.
Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.

Sequential Read modes (1) and (2) output the contents of addresses 0~527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the page address reaches the next block address, read command (00H/01H/50H) and address input are needed.
Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the RE clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

<table>
<thead>
<tr>
<th>STATUS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O1 Pass/Fail</td>
<td>Pass: 0 Fail: 1</td>
</tr>
<tr>
<td>I/O2 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O3 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O4 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O5 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O6 Not Used</td>
<td>0</td>
</tr>
<tr>
<td>I/O7 Ready/Busy</td>
<td>Ready: 1 Busy: 0</td>
</tr>
<tr>
<td>I/O8 Write Protect</td>
<td>Protect: 0 Not Protected: 1</td>
</tr>
</tbody>
</table>

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

System Design Note: If the RY/BY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.
Auto Page Program

The device carries out an Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE after the Erase Start command D0H which follows the Erase Setup command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The address and data registers are set as follows after a Reset:

- Address Register: All 0
- Data Register: All 1
- Operation Mode: Wait state

The response to an FFH Reset command input during the various device operations is as follows:

When a Reset (FFH) command is input during programming

![Diagram](image1)

When a Reset (FFH) command is input during erasing

![Diagram](image2)

When a Reset (FFH) command is input during a Read operation

![Diagram](image3)
When a Status Read command (70H) is input after a Reset

Fig. 11. I/O status: Pass/Fail → Pass
Ready/Busy → Ready

RY/BY

However, the following operation is prohibited. If the following operation is executed, correct resetting of the address and data register cannot be guaranteed.

RY/BY

I/O status: Ready/Busy → Busy

When two or more Reset commands are input in succession

Fig. 12. I/O status: Ready/Busy → Busy

RY/BY

The second FF command is invalid, but the third FF command is valid.
ID Read

The TH58NS512 contains ID codes which identify the device type and the manufacturer. The ID codes can be read out under the following timing conditions:

Table 6. Code table

<table>
<thead>
<tr>
<th>Maker code</th>
<th>Device code</th>
<th>Option code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 0 1 1 0 0 0</td>
<td>0 1 1 1 0 1 1 0</td>
<td>1 0 1 0 0 1 0 1</td>
</tr>
<tr>
<td>98H</td>
<td>76H</td>
<td>A5H</td>
</tr>
<tr>
<td>*</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The A5H for the 3rd byte of ID read means the existence of 128 bit unique ID number in the device.

How to read out unique ID number

The 128 bit unique ID number is embedded in the device. The procedure to read out the ID number is available using special command which is provided under a non-disclosure agreement.
APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(3) Pointer control for 00H, 01H and 50H

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

<table>
<thead>
<tr>
<th>Read Mode</th>
<th>Command</th>
<th>Pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>00H</td>
<td>0~255</td>
</tr>
<tr>
<td>(2)</td>
<td>01H</td>
<td>256~511</td>
</tr>
<tr>
<td>(3)</td>
<td>50H</td>
<td>512~527</td>
</tr>
</tbody>
</table>

The pointer is set to region A by the 00H command, to region B by the 01H command, and to region C by the 50H command.

(Example)

The 00H command must be input to set the pointer back to region A when the pointer is pointing to region C.

To program region C only, set the start point to region C using the 50H command.

Figure 14. Pointer control

Figure 15. Example of How to Set the Pointer
(4) Acceptable commands after Serial Input command 80H

Once the Serial Input command 80H has been input, do not input any command other than the Program Execution command 10H or the Reset command FFH.

![Diagram](image)

If a command other than 10H or FFH is input, the Program operation is not performed.

![Diagram](image)

(5) Status Read during a Read operation

The device status can be read out by inputting the Status Read command 70H in Read mode. Once the device has been set to Status Read mode by a 70H command, the device will not return to Read mode. Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command 00H is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(6) Auto programming failure

If the programming result for page address M is Fail, do not try to program the page to address N in another block. Because the previous input data has been lost, the same input sequence of 80H command, address and data is necessary.
(7) **RY/BY**: termination for the Ready/Busy pin (RY/BY)

A pull-up resistor needs to be used for termination because the RY/BY buffer consists of an open drain circuit.

![Image](image1)

Figure 19.

This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.

(8) **Status after power-on**

The following sequence is necessary because some input signals may not be stable at power-on.

![Image](image2)

Figure 20.

(9) **Power-on/off sequence**:

The WP signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary:

![Image](image3)

Figure 21. Power-on/off Sequence
(10) Note regarding the WP signal

The Erase and Program operations are automatically reset when WP goes Low. The operations are enabled and disabled as follows:

Enable Programming

Enable Erasing

Disable Erasing

Disable Programming
(11) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

**Read operation**

![Read operation diagram]

Internal read operation starts when WE goes High in the third cycle.

Figure 22.

**Program operation**

![Program operation diagram]

Figure 23.
(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as follows:

| First programming | Data Pattern 1 | All 1s |
| Second programming | All 1s | Data Pattern 2 | All 1s |
| Tenth programming | All 1s | Data Pattern 10 |

![Figure 24.](image)

Note: The input data for unprogrammed or previously programmed page segments must be 1 (i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all 1).

(13) Note regarding the RE signal

The internal column address counter is incremented synchronously with the RE clock in Read mode. Therefore, once the device has been set to Read mode by a 00H, 01H or 50H command, the internal column address counter is incremented by the RE clock independently of the address input timing. If the RE clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array → register) will occur and the device will enter Busy state. (Refer to Figure 25.)

![Figure 25.](image)

Hence the RE clock input must start after the address input.
(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, the following issues must be recognized:

Referring to the Block status area in the redundant area allows the system to detect bad blocks in the accordance with the physical data format issued by the SSFDC Forum. Detect the bad blocks by checking the Block Status Area at the system power-on, and do not access the bad blocks in the following routine.

The number of valid blocks at the time of shipment is as follows:

<table>
<thead>
<tr>
<th>Valid (Good) Block Number</th>
<th>MIN</th>
<th>TYP.</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4016</td>
<td></td>
<td>4096</td>
<td>Block</td>
</tr>
</tbody>
</table>

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.

<table>
<thead>
<tr>
<th>FAILURE MODE</th>
<th>DETECTION AND COUNTERMEASURE SEQUENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block Erase Failure</td>
<td>Status Read after Erase → Block Replacement</td>
</tr>
<tr>
<td>Page Programming Failure</td>
<td>Status Read after Program → Block Replacement</td>
</tr>
<tr>
<td>Single Bit Programming Failure 1 → 0</td>
<td>(1) Block Verify after Program → Retry</td>
</tr>
</tbody>
</table>

- ECC: Error Correction Code
- Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs for an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) Chattering of Connector

There may be contact chattering when the TH58NS512DC is inserted or removed from a connector. This chattering may cause damage to the data in the TH58NS512DC. Therefore, sufficient time must be allowed for contact bouncing to subside when a system is designed with SmartMedia™.

(17) The TH58NS512DC is formatted to comply with the Physical and Logical Data Format of the SSFDC Forum at the time of shipping.
Handling Precaution

(1) Avoid bending or subjecting the card to sudden impact.
(2) Avoid touching the connectors so as to avoid damage from static electricity. 
    This card should be kept in the antistatic film case when not in use.
(3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data corruption 
    that may occur because of mishandling.

How to read out unique ID number

The 128 bit unique ID number is embedded in the device. The procedure to read out the ID number is available 
using special command which is provided under a non-disclosure agreement.

SSFDC Forum

The SSFDC Forum is a voluntary organization intended to promote the SmartMedia™, a small removable 
NAND flash memory card. The SSFDC Forum standardized the following specifications in order to keep the 
compatibility of SmartMedia™ in systems. The latest specifications issued by the Forum must be referenced when 
a system is designed with SmartMedia™, especially with large capacity SmartMedia™.

SmartMedia™ Electrical Specifications
SmartMedia™ Physical Format Specification
SmartMedia™ Logical Format Specification

Some electrical specifications in this data sheet show differences from the Forum's electrical specification. 
Complying with the Forum's electrical specification maintains compatibility with other SmartMedias.

Please refer folloing SSFDC Forum's URL to get the detailed information of each specification.

URL  http://www.ssfdc.or.jp
PACKAGE DIMENSIONS

- FDC-22C

Unit: mm

E: Write protect area
F: The distance between the surface of D and all contact areas is less than 0.1 mm.
G: Index area