TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

64-MBIT (8M × 8 BITS) CMOS NAND E^2PROM (8M BYTE SmartMedia™)

DESCRIPTION

The TC58V64A is a single 3.3-V 64-Mbit (69,206,016) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as 528 bytes × 16 pages × 1024 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (8 Kbytes + 512 bytes: 528 bytes × 16 pages).

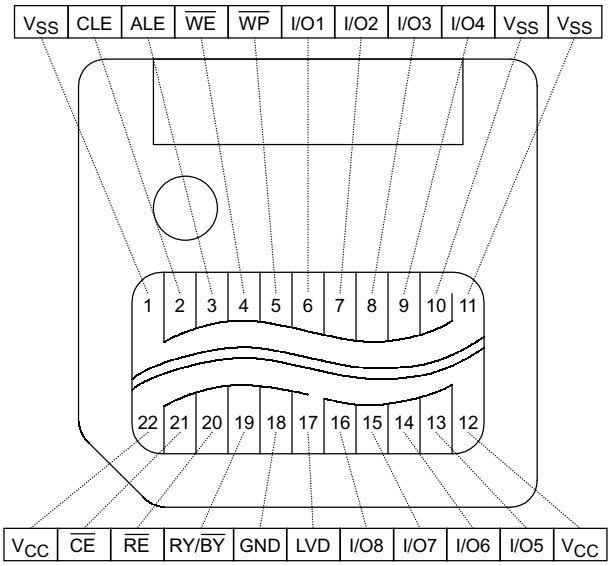
The TC58V64A is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

The data stored in the TC58V64ADC needs to comply with the data format standardized by the SSFDC Forum in order to maintain compatibility with other SmartMedia™ systems.

FEATURES

- Organization
  - Memory cell array 528 × 16K × 8
  - Register 528 × 8
  - Page size 528 bytes
  - Block size (8K + 512) bytes
- Modes
  - Read, Reset, Auto Page Program,
  - Auto Block Erase, Status Read
- Mode control
  - Serial input/output, Command control
- Complies with the SmartMedia™ Electrical Specification and Data Format Specification issued by the SSFDC Forum
- Power supply
  - V_{CC} = 3.3 V ± 0.3 V
- Access time
  - Cell array-register 25 μs max
  - Serial Read cycle 50 ns min
- Operating current
  - Read (50-ns cycle) 10 mA typ.
  - Program (avg.) 10 mA typ.
  - Erase (avg.) 10 mA typ.
  - Standby 100 μA max
- Package
  - TC58V64ADC: FDC-22A (Weight: 1.8 g typ.)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1~I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
GND	Ground Input
LVD	Low Voltage Detect
V_{CC}	Power supply
V_{SS}	Ground

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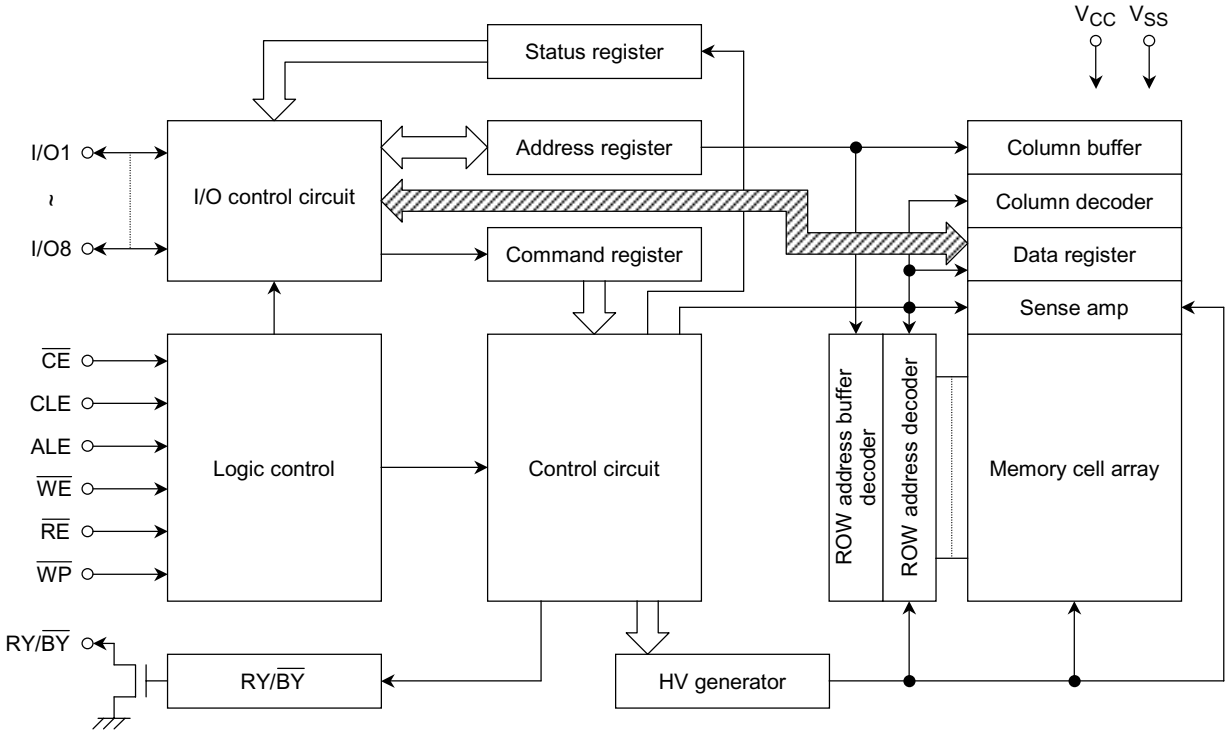
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.6~4.6	V
V_{IN}	Input Voltage	−0.6~4.6	V
$V_{I/O}$	Input/Output Voltage	−0.6 V~V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{stg}	Storage Temperature	−20~65	°C
T_{opr}	Operating Temperature	0~55	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

000707EBA2

VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1014	—	1024	Blocks

(1) The TC58V64A occasionally contains unusable blocks. Refer to Application Note 14 toward the end of this document.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	3	3.3	3.6	V
V_{IH}	High Level Input Voltage	2	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	0.8	V

* −2 V (pulse width ≤ 20 ns)

DC CHARACTERISTICS (Ta = 0°~55°C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 V~V_{CC}	—	—	±10	μA
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	10	30	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO7}	Programming Current	—	—	10	30	mA
I_{CCO8}	Erasing Current	—	—	10	30	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	—	—	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V	—	—	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ Pin	V_{OL} = 0.4 V	—	8	—	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = 0°~55°C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ -High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready-to-$\overline{RE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	—	35	ns	
t_{CEH}	$\overline{CE}$ -High Time for Last Address in Serial Read Cycle	100	—	ns	(2)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	—	35	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ -High-to-Output-High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ -High-to-Output-High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ -High Hold Time	15	—	ns	
t_{IR}	Output-High-Impedance-to-$\overline{RE}$ Rising Edge	0	—	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	—	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	—	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	100	—	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	100	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	25	µs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	—	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	—	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (When interrupted by $\overline{CE}$ in Read Mode)	—	600 + t_f (RY/$\overline{BY}$)	ns	(1)
t_{RST}	Device Reset Time (Read/Program/Erase)	—	6/10/500	µs	

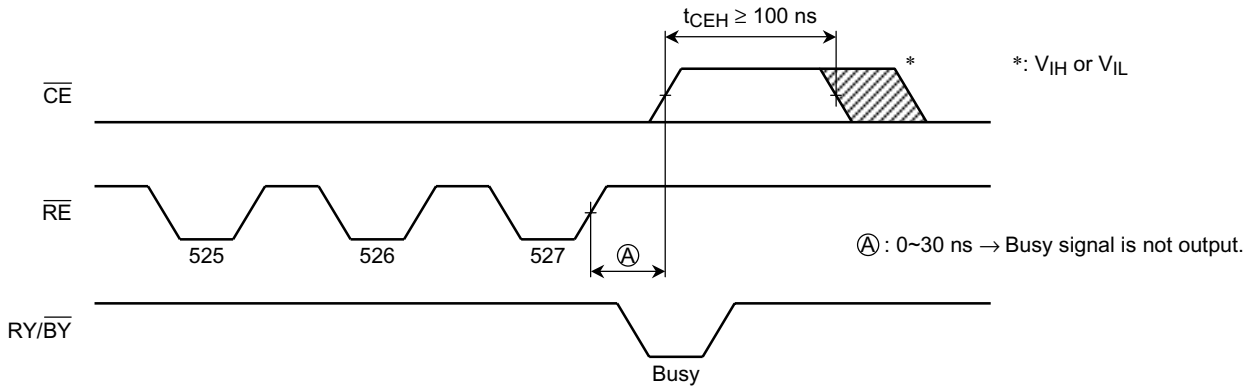
AC TEST CONDITIONS

PARAMETER	VALUES
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3 ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C_L (100 pF) + 1 TTL

Notes:

(1) $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin. (Refer to Application Note (7) toward the end of this document.)

(2) Sequential Read is terminated when t_{CEH} is greater than or equal to 100 ns. If the $\overline{RE}$ to $\overline{CE}$ delay is less than 30 ns, RY/$\overline{BY}$ signal stays Ready.



PROGRAMMING AND ERASING CHARACTERISTICS

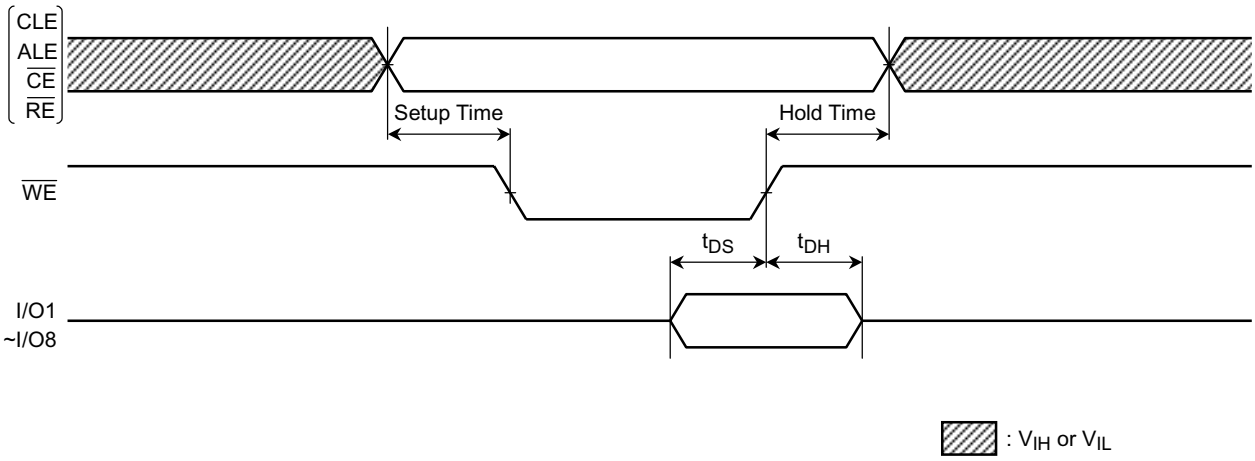
(Ta = 0°~55°C, V_{CC} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	200	1000	μs	
N	Number of Programming Cycles on Same Page	—	—	10		(1)
t_{BERASE}	Block Erasing Time	—	3	4	ms	
P/E	Number of Program/Erase Cycles	—	—	2.5×10^5		(2)

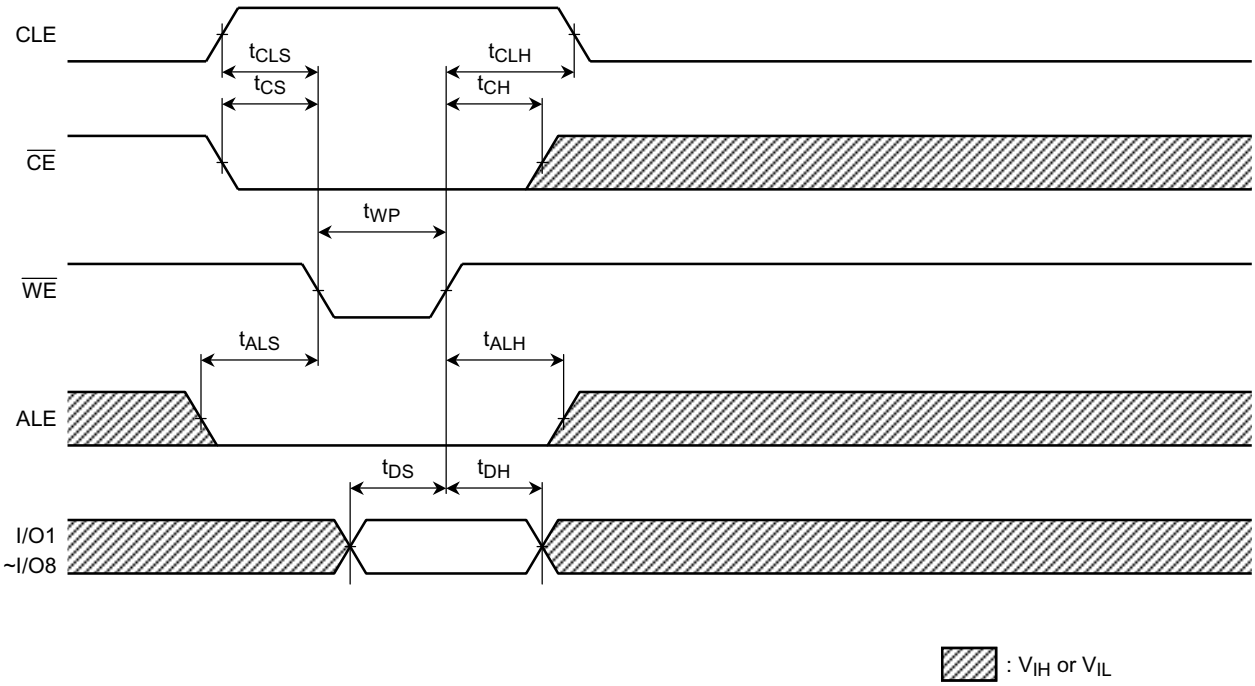
(1) Refer to Application Note 12 toward the end of this document.
(2) Refer to Application Note 15 toward the end of this document.

TIMING DIAGRAMS

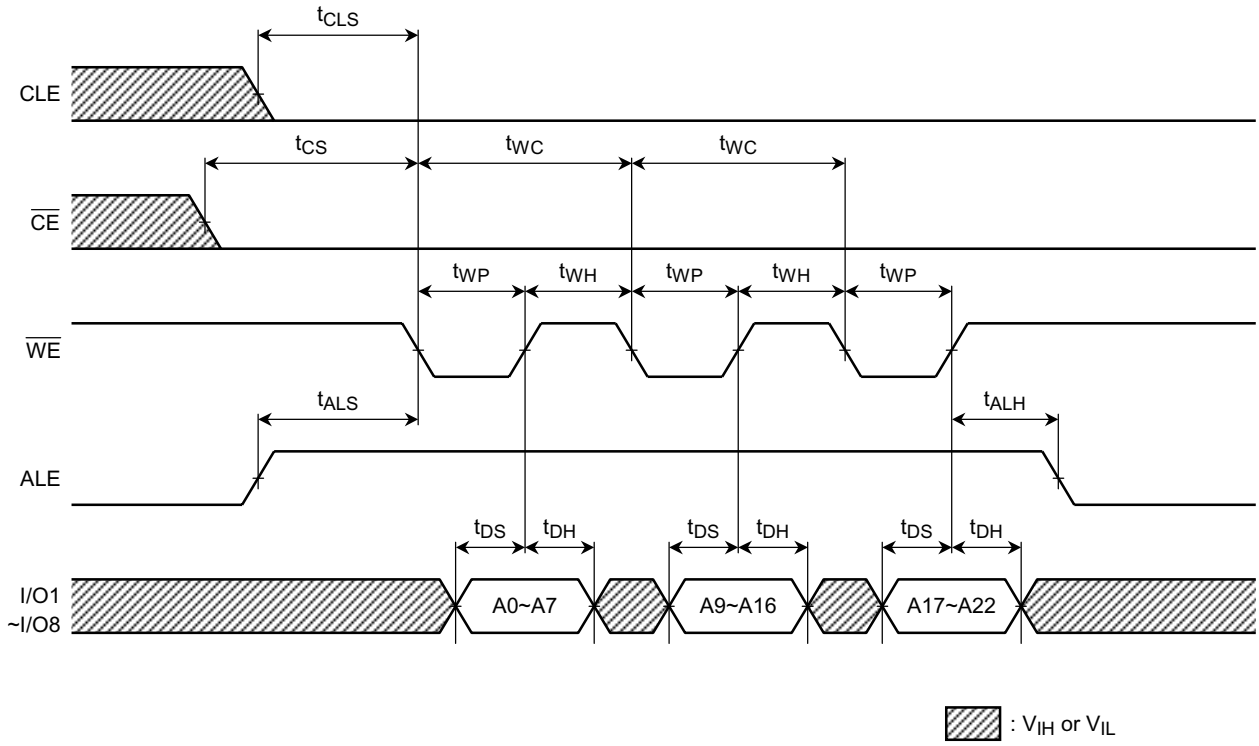
Latch Timing Diagram for Command/Address/Data



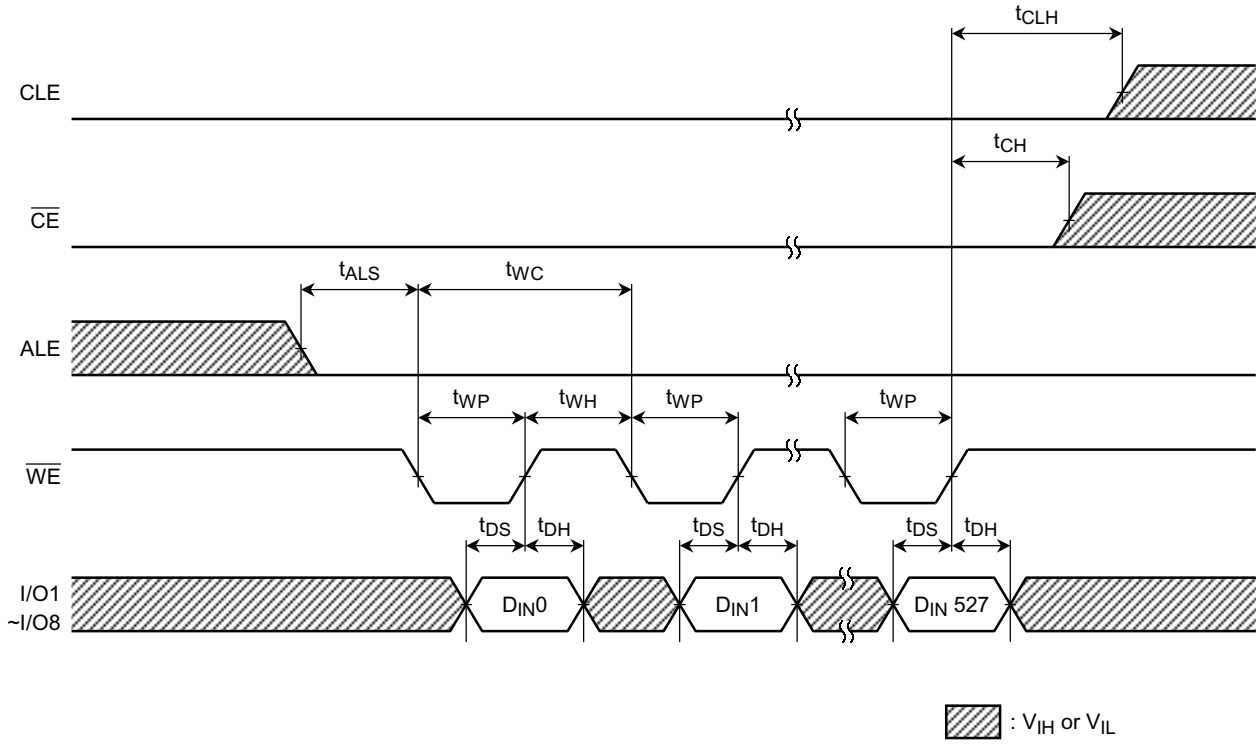
Command Input Cycle Timing Diagram



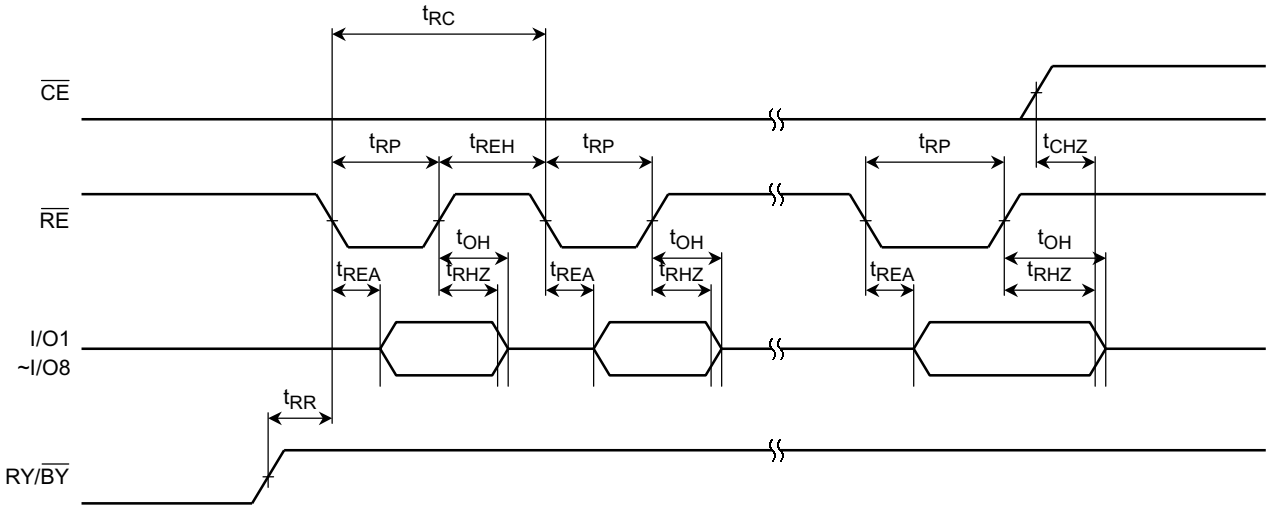
Address Input Cycle Timing Diagram



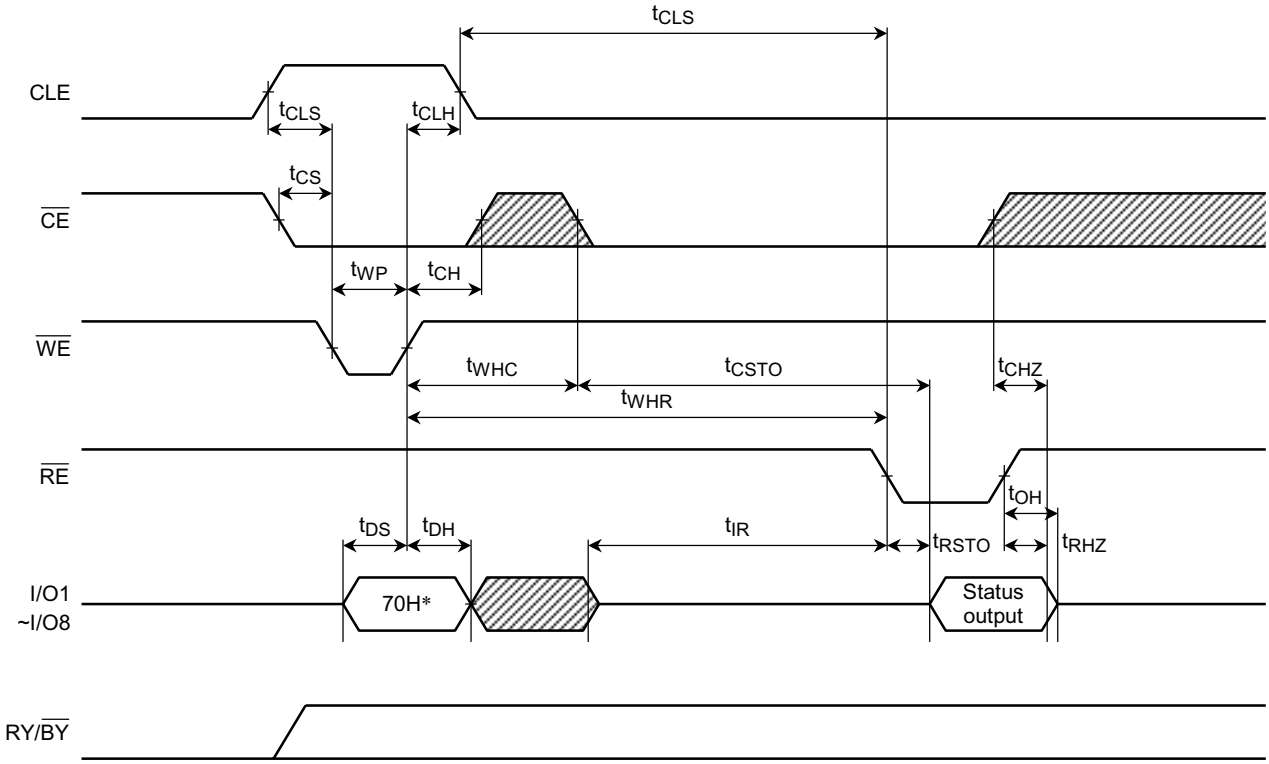
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



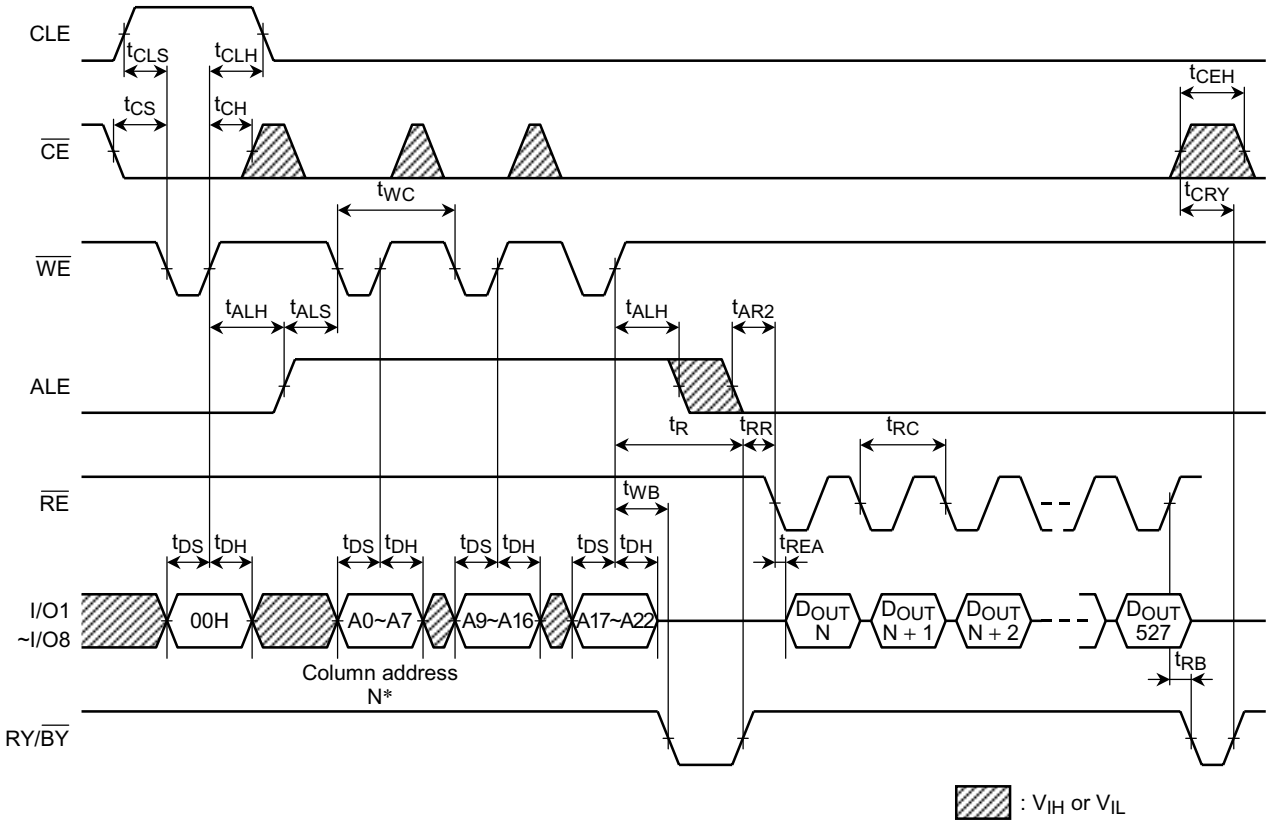
Status Read Cycle Timing Diagram



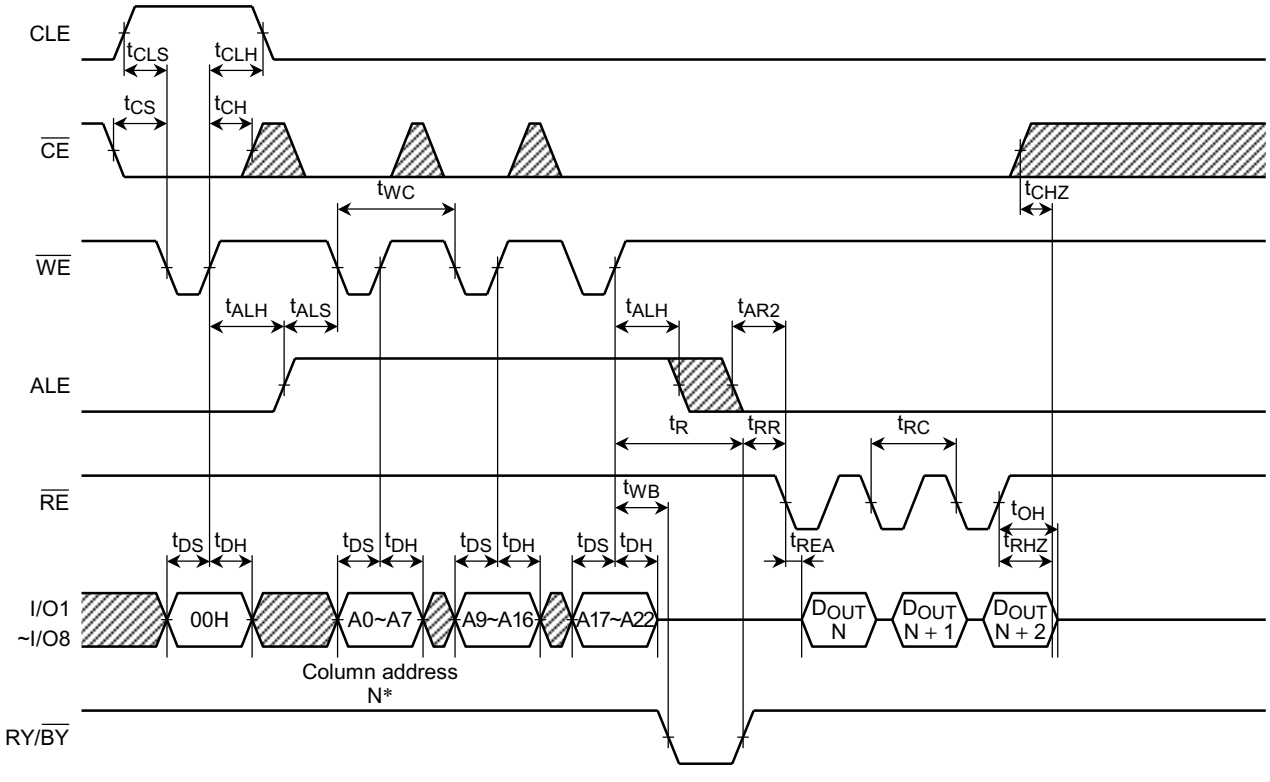
* 70H represents the hexadecimal number 70.

: V_{IH} or V_{IL}

Read Cycle (1) Timing Diagram

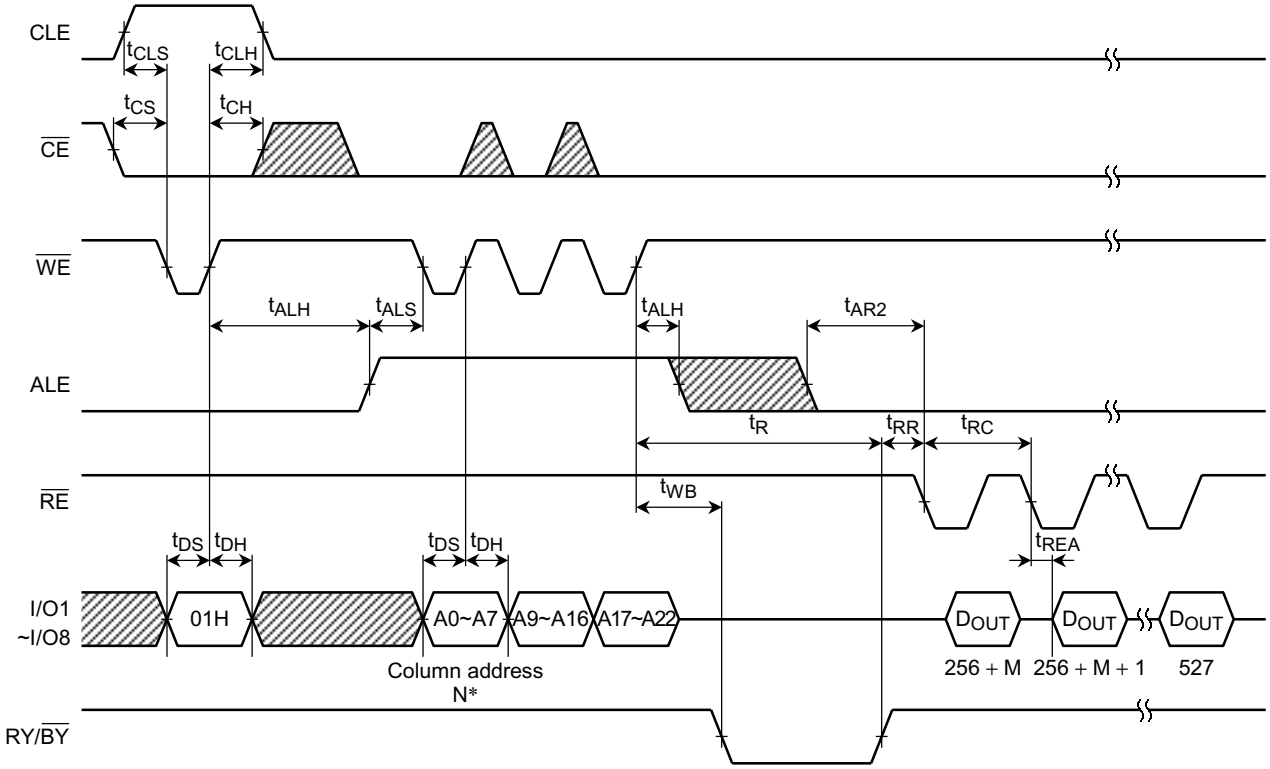


Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$



* Read Operation using 00H Command N: 0~255

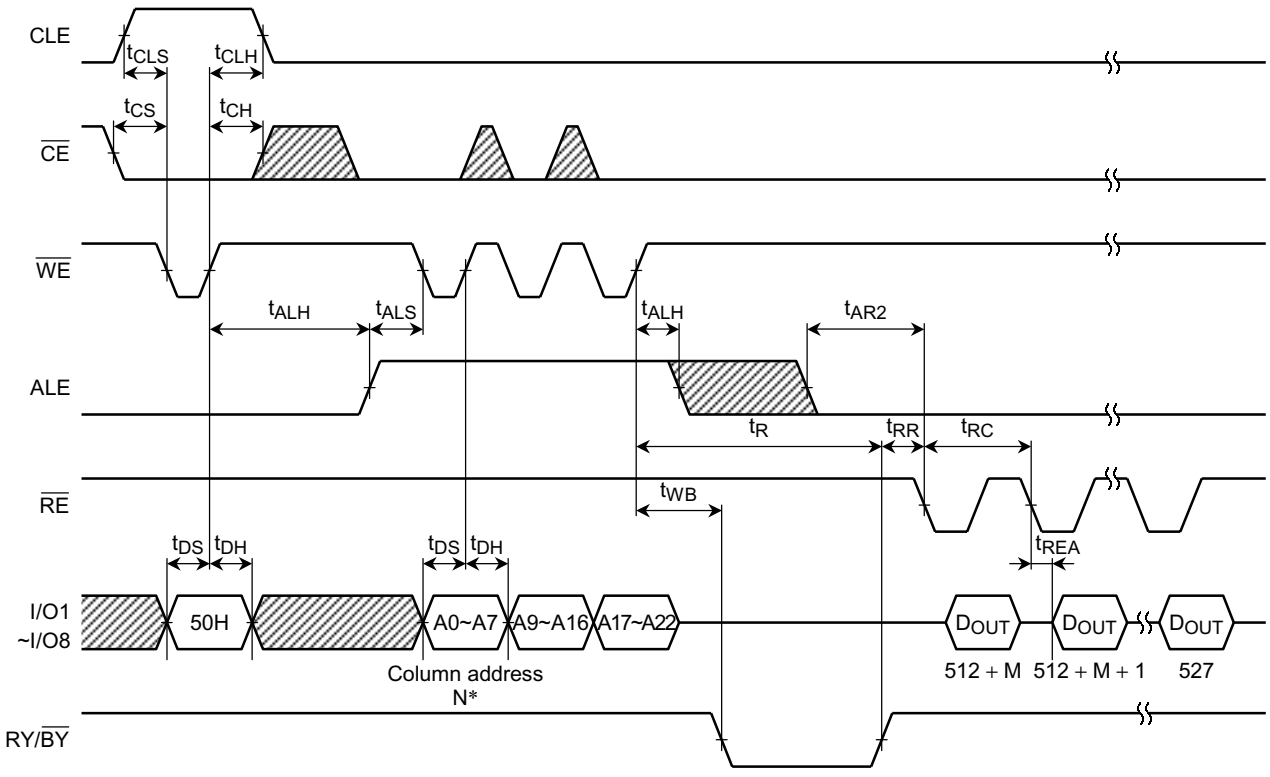
Read Cycle (2) Timing Diagram



* Read Operation using 01H Command N: 0~255

: V_{IH} or V_{IL}

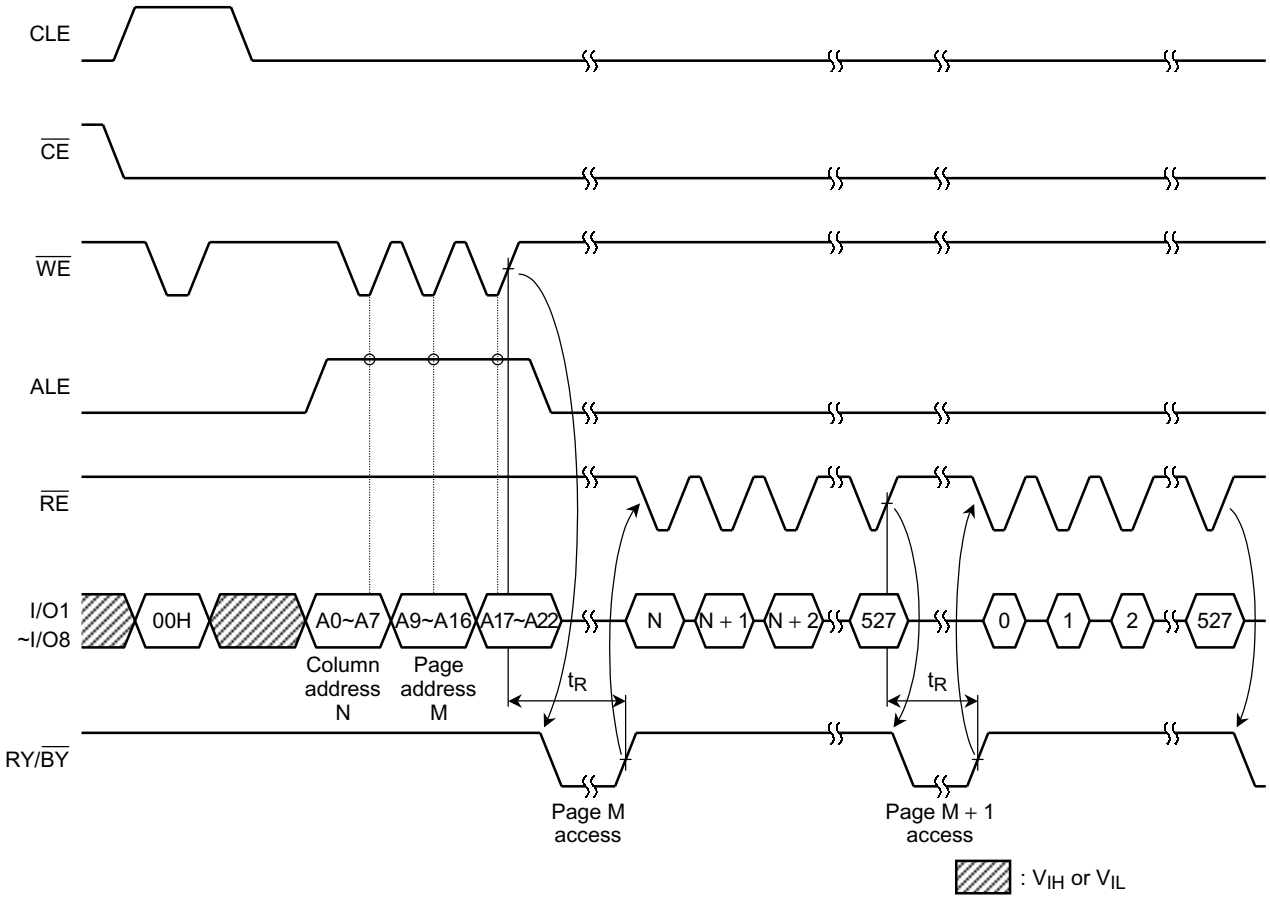
Read Cycle (3) Timing Diagram



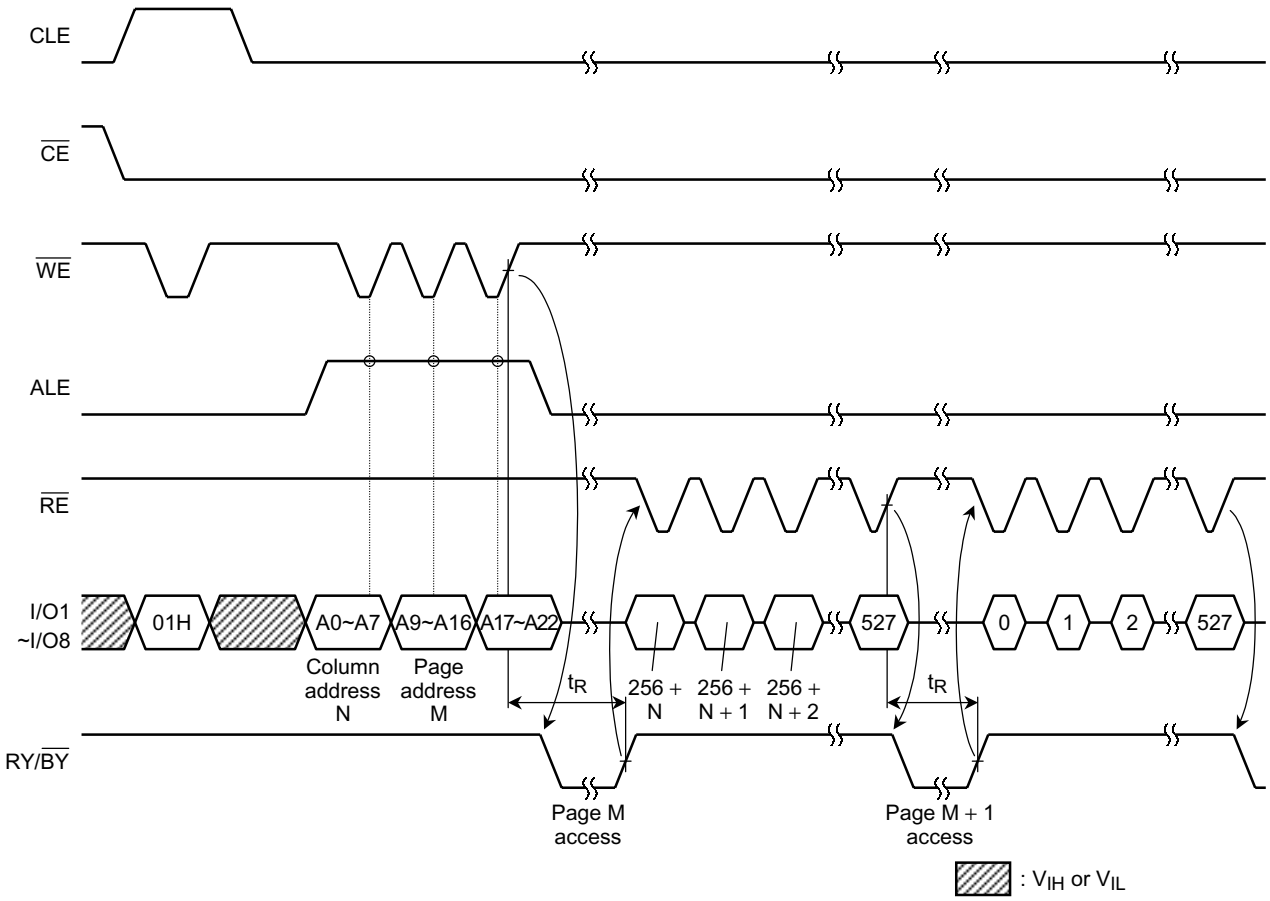
* Read Operation using 50H Command N: 0~15

: V_{IH} or V_{IL}

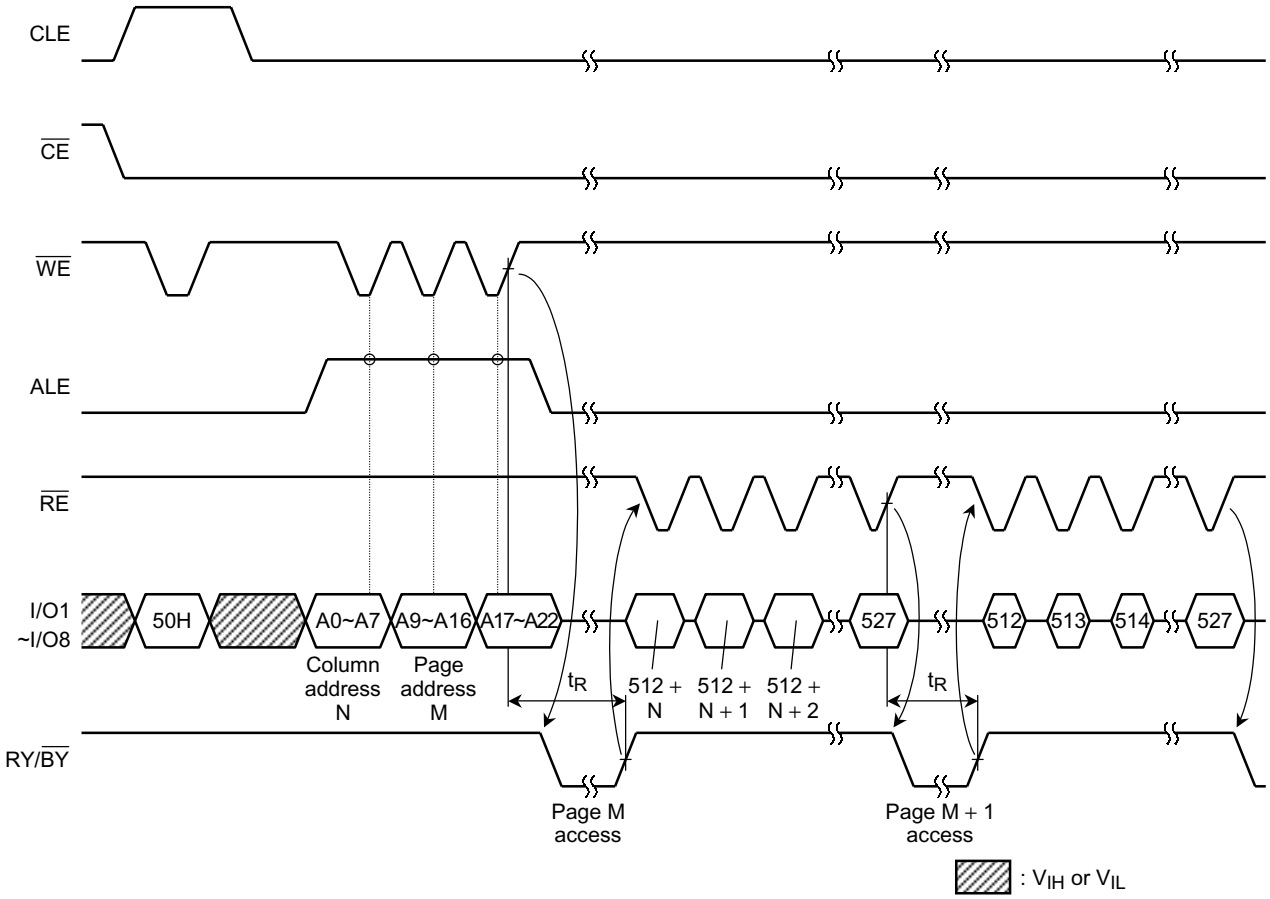
Sequential Read (1) Timing Diagram



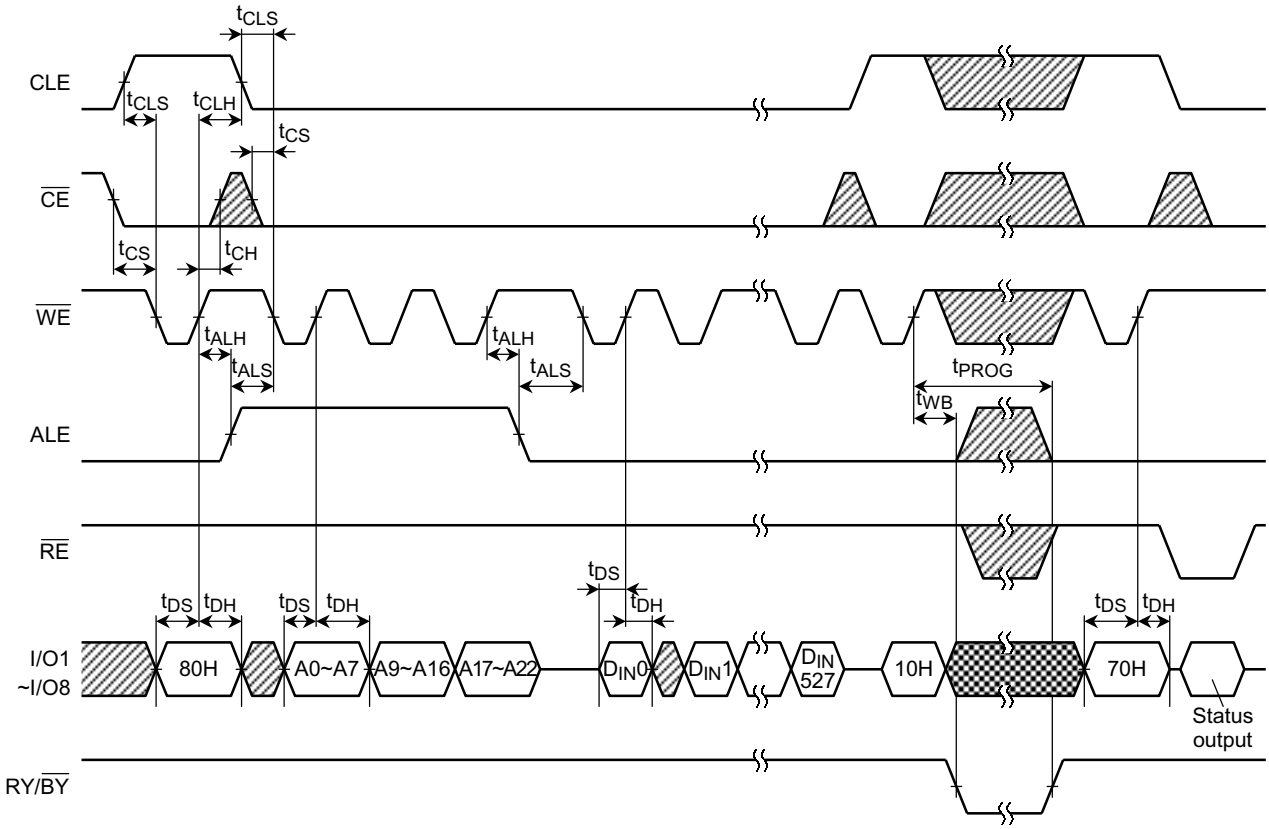
Sequential Read (2) Timing Diagram



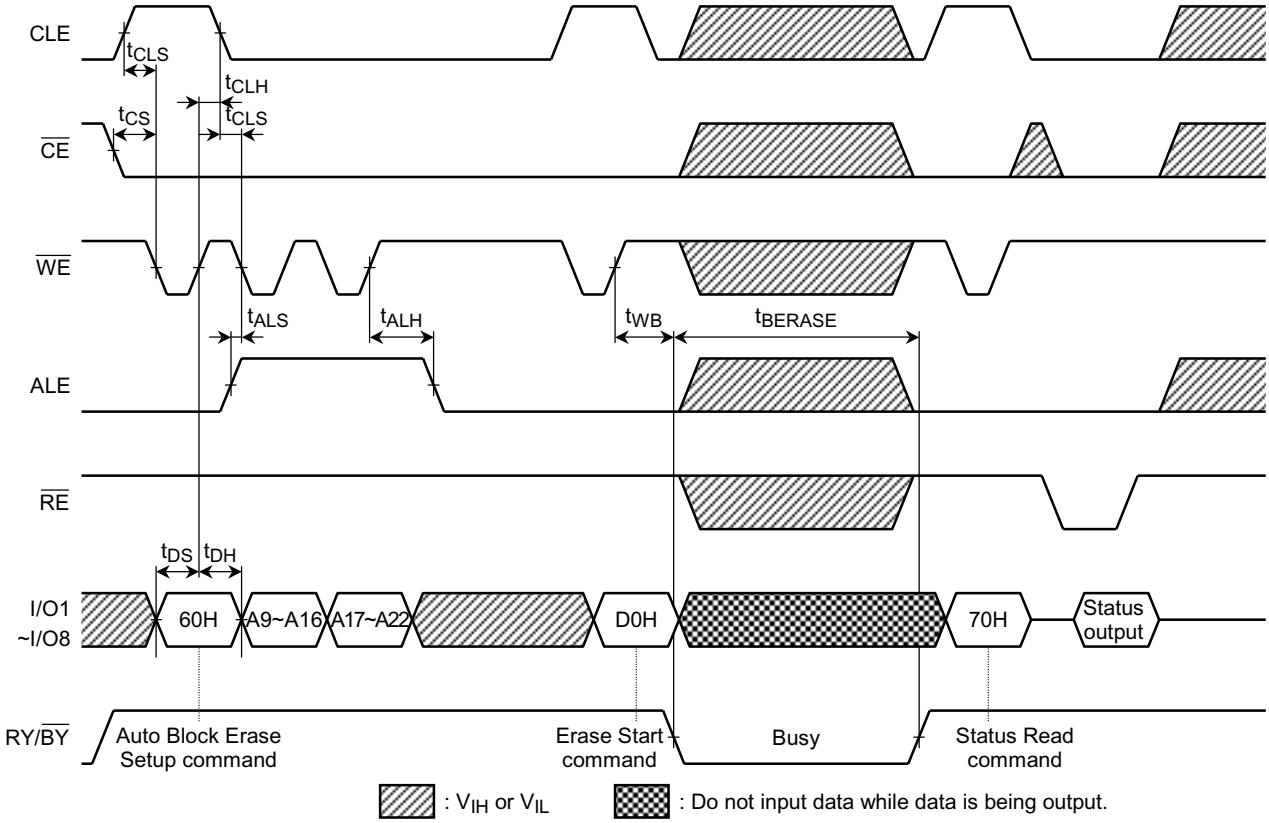
Sequential Read (3) Timing Diagram



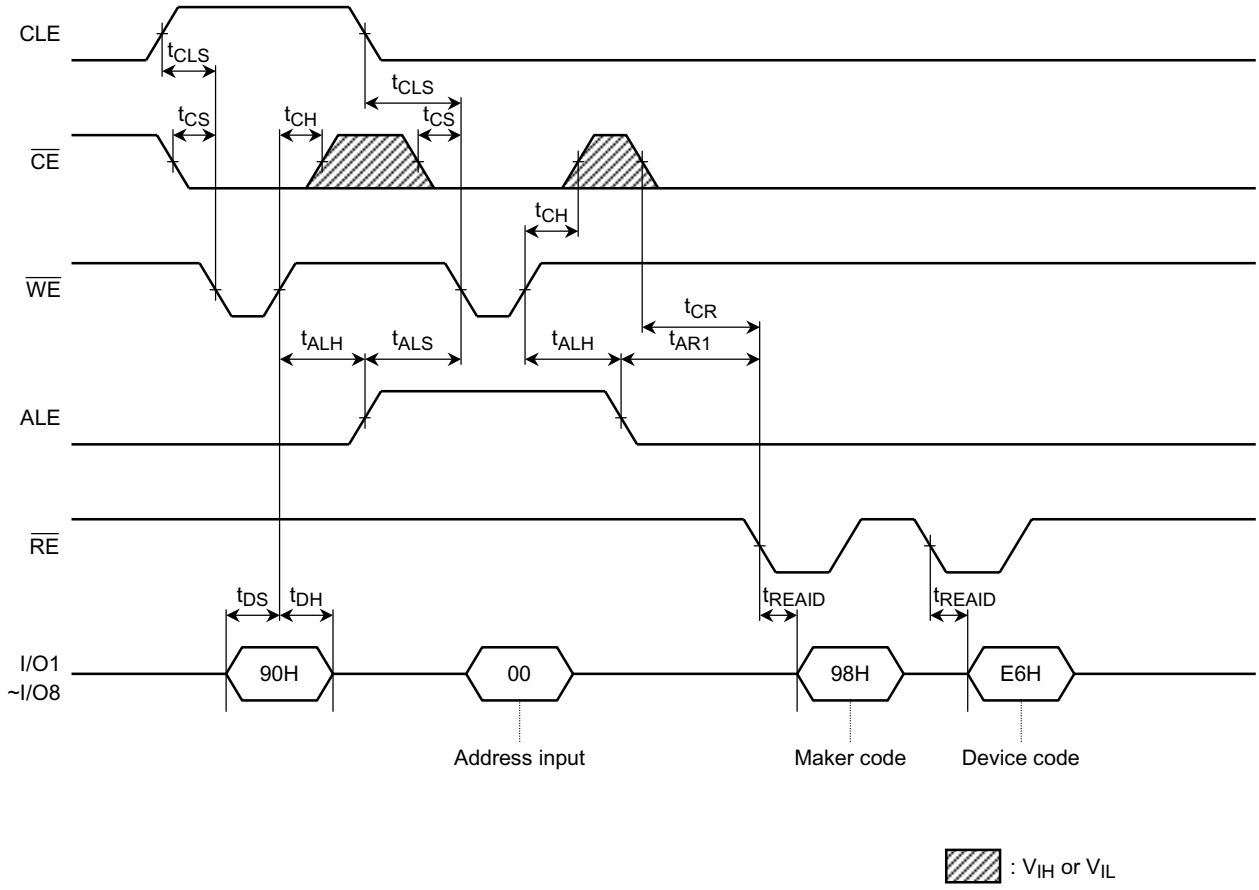
Auto-Program Operation Timing Diagram



Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

TC58V64ADC

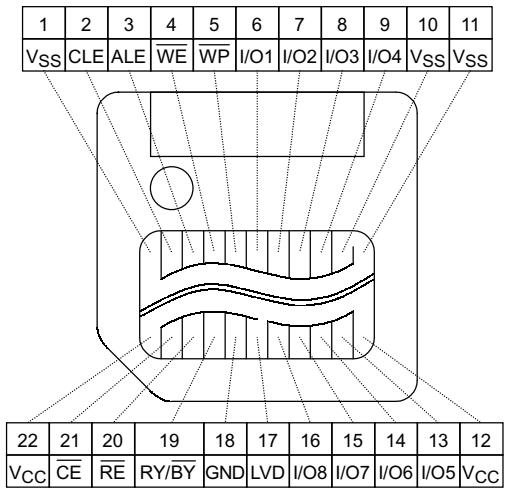


Figure 1. Pinout

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of $\overline{WE}$ if ALE is High. Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a Read operation. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High. The $\overline{CE}$ signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1~I/O8

The I/O1 to I/O8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Low Voltage Detect: LVD

The LVD signal is used to detect the power supply voltage level.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

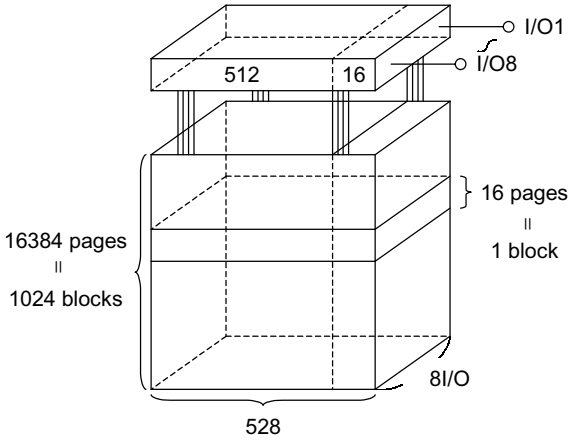


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 16 pages = (8K + 512) bytes
Capacity = 528 bytes × 16 pages × 1024 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	*L	*L	A22	A21	A20	A19	A18	A17

A0~A7: Column address
A9~A22: Page address
(A13~A22: Block address
A9~A12: NAND address in block)

*: A8 is automatically set to Low or High by a 00H command or a 01H command.

*: I/O7 and I/O8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic table

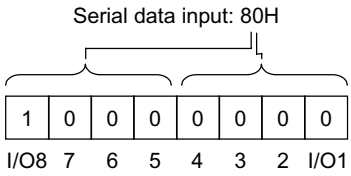
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⎍	H	*
Data Input	L	L	L	⎍	H	*
Address Input	L	H	L	⎍	H	*
Serial Data Output	L	L	L	H	⎌	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	O
Auto Program	10	—	
Auto Block Erase	60	D0	
Status Read	70	—	O
ID Read	90	—	

HEX data bit assignment
(Example)



Once the device has been set to Read mode by a 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

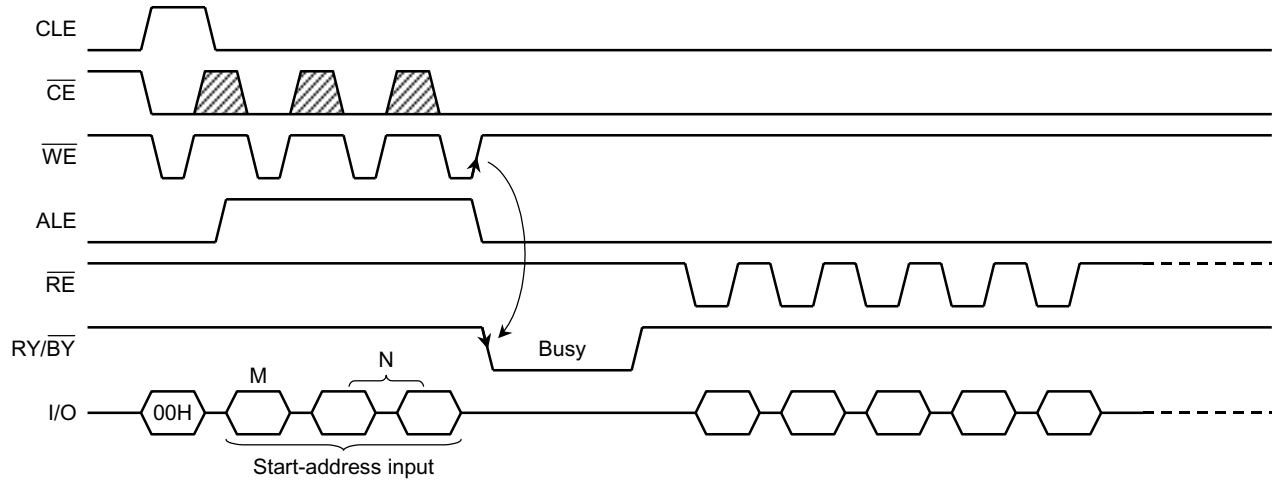
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1~I/O8	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.



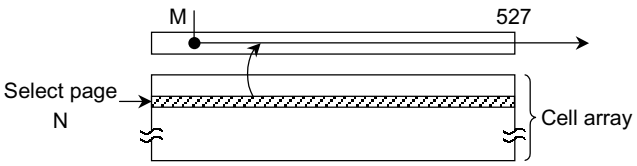
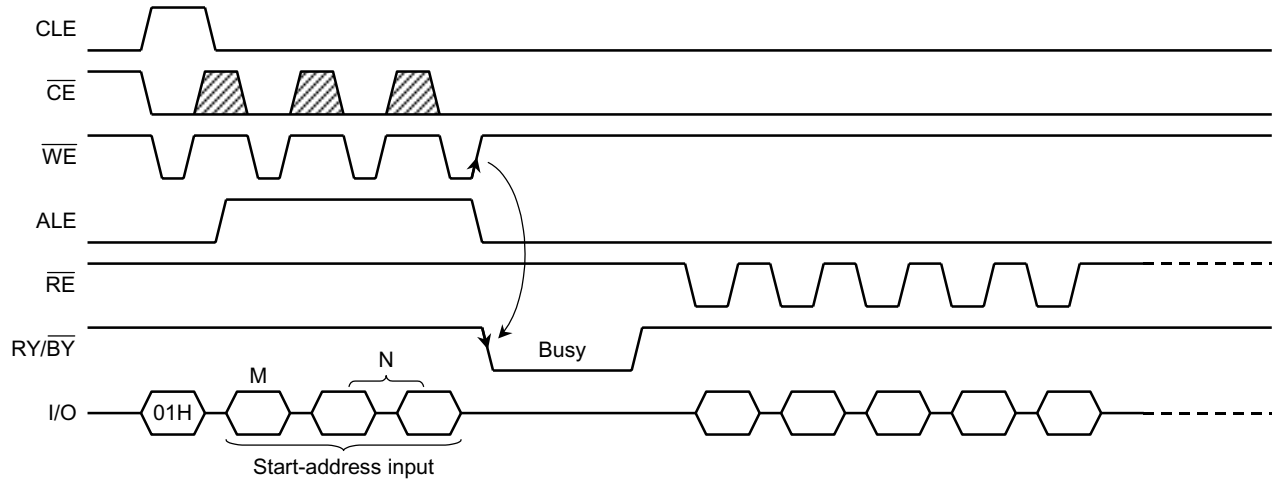


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)



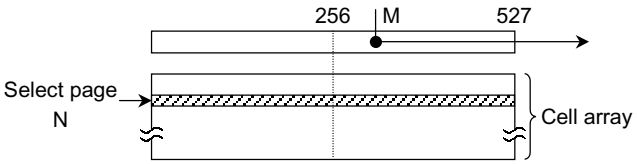


Figure 4. Read mode (2) operation

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

However, for a Sequential Read, output of the next page starts from column address 0.

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

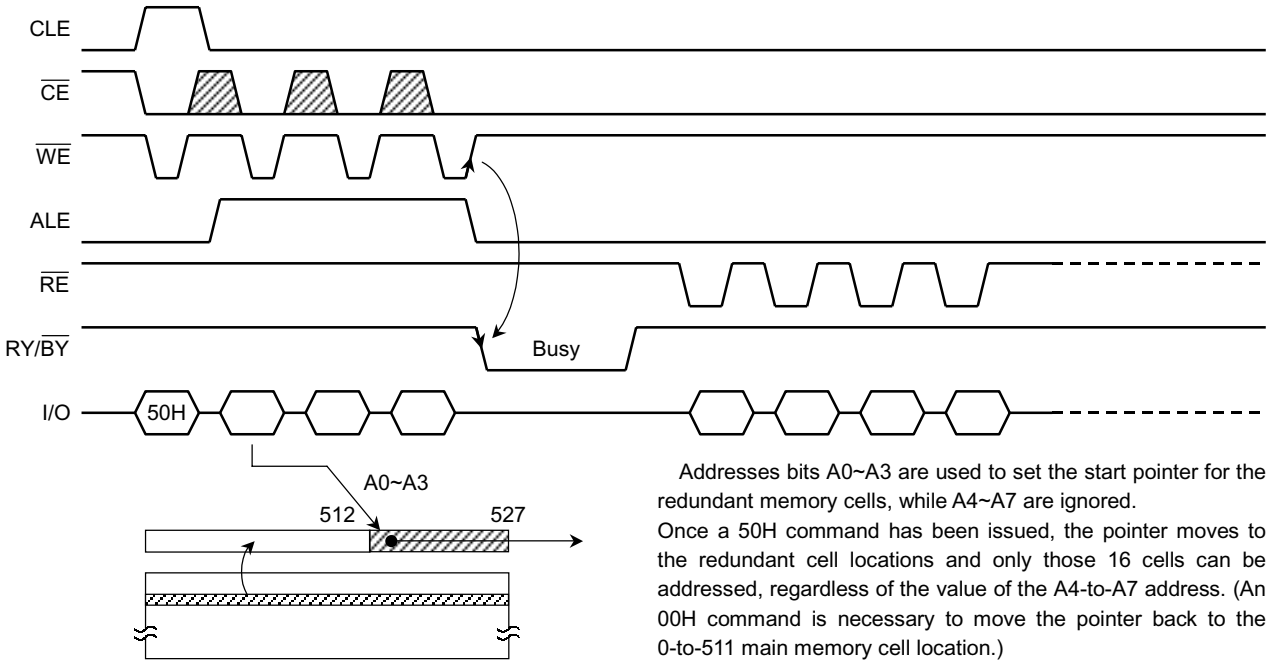
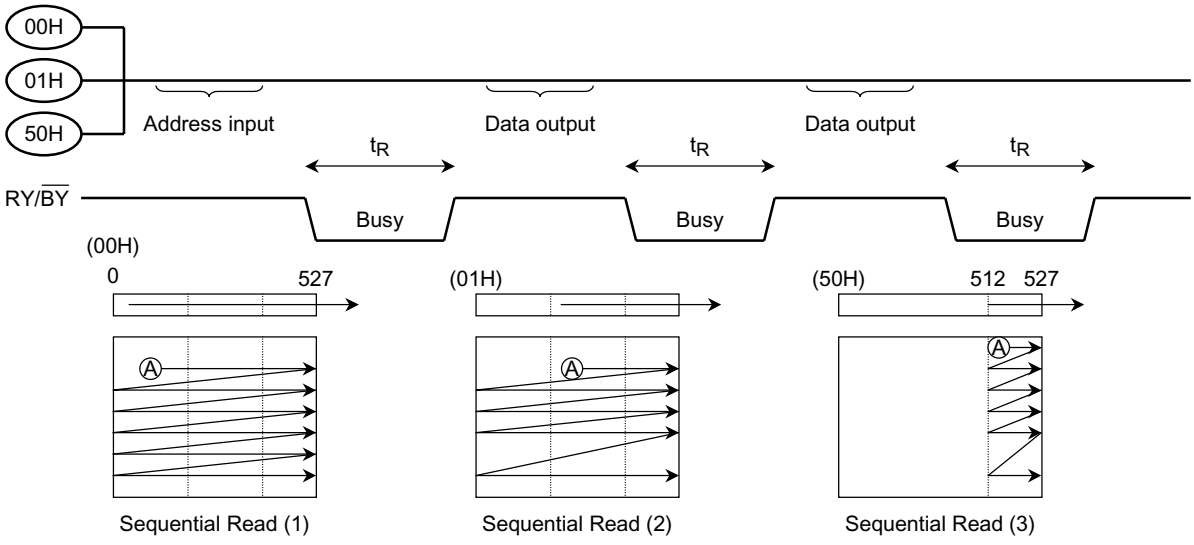


Figure 5. Read mode (3) operation

Addresses bits A0~A3 are used to set the start pointer for the redundant memory cells, while A4~A7 are ignored.
Once a 50H command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address. (An 00H command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output the contents of addresses 0~527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each $\overline{RE}$ clock signal.

** Column address 527 on the last page.

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

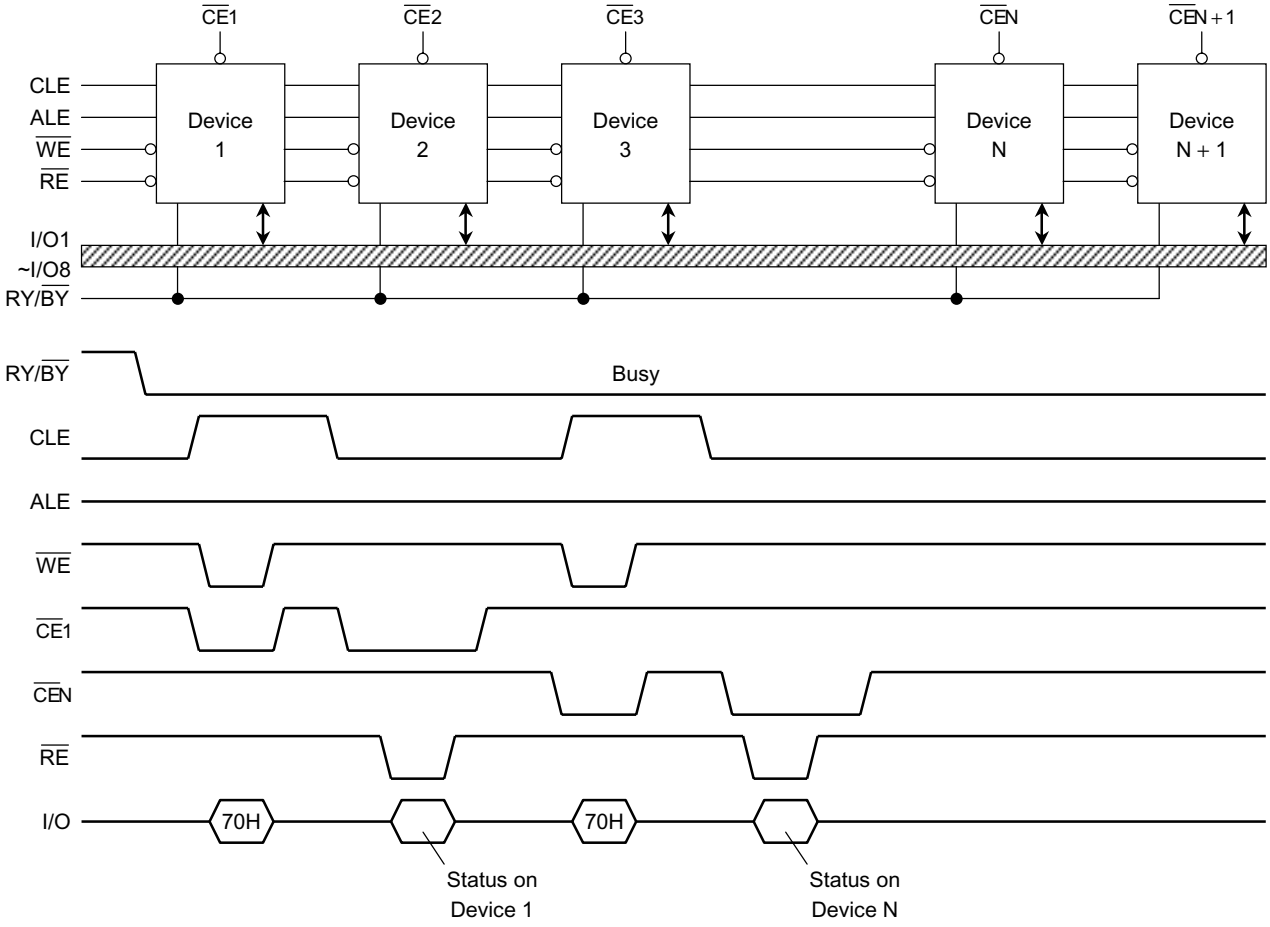


Figure 6. Status Read timing application example

System Design Note: If the RY/$\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

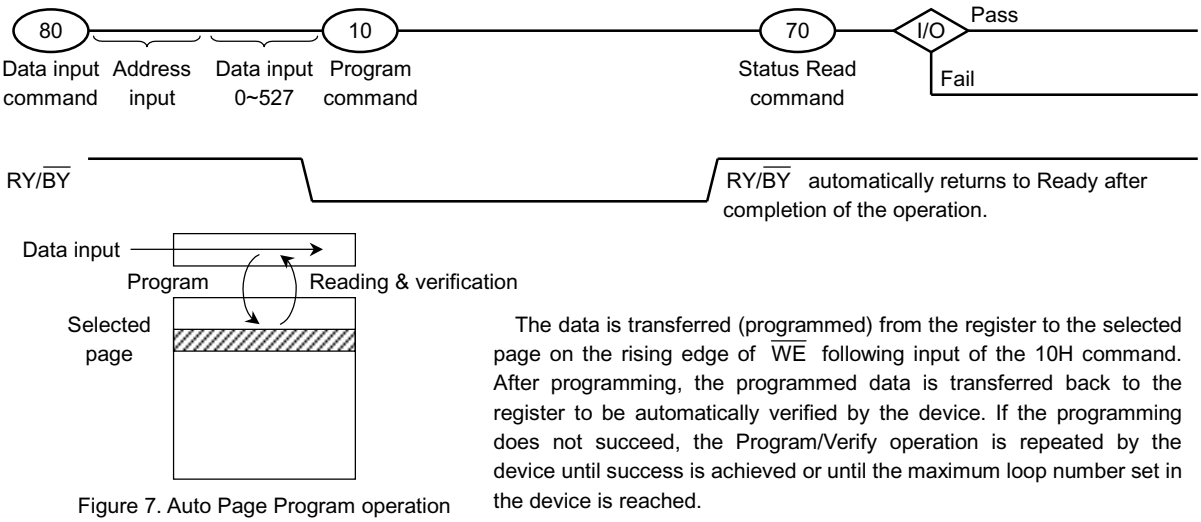
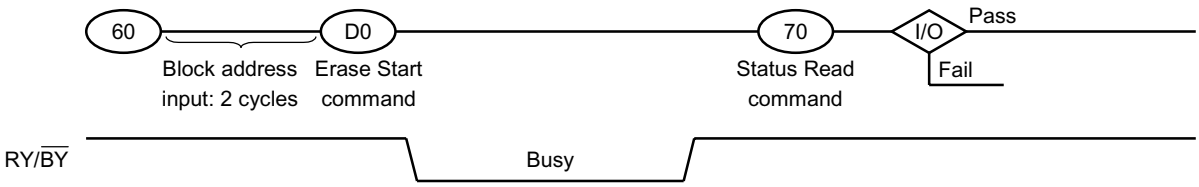


Figure 7. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the 10H command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command D0H which follows the Erase Setup command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Reset

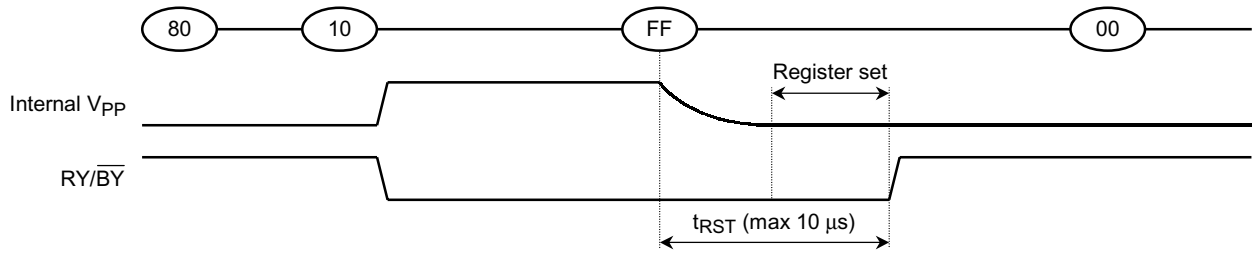
The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.
The address and data registers are set as follows after a Reset:

- Address Register: All 0
- Data Register: All 1
- Operation Mode: Wait state

The response to an FFH Reset command input during the various device operations is as follows:

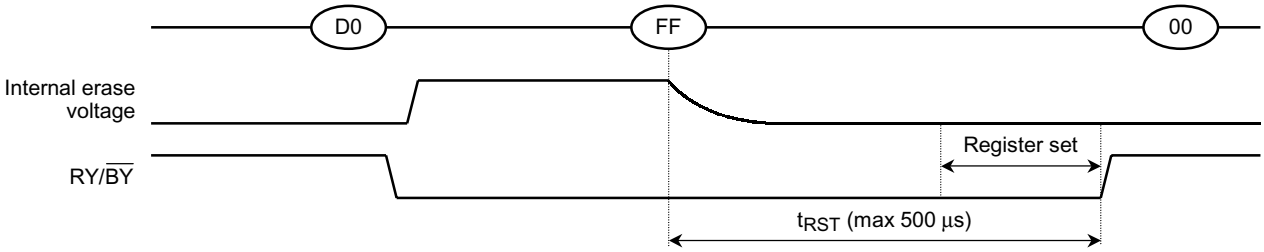
When a Reset (FFH) command is input during programming

Figure 8.



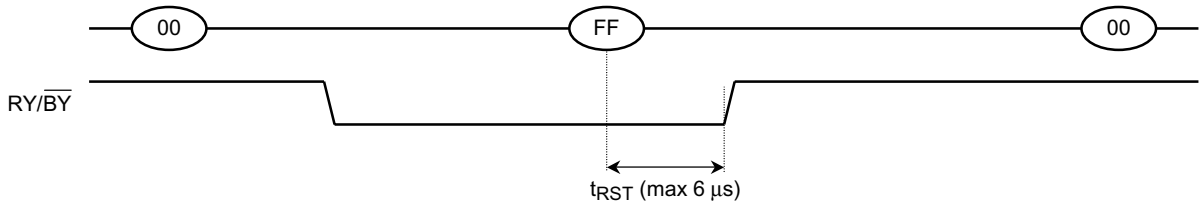
When a Reset (FFH) command is input during erasing

Figure 9.



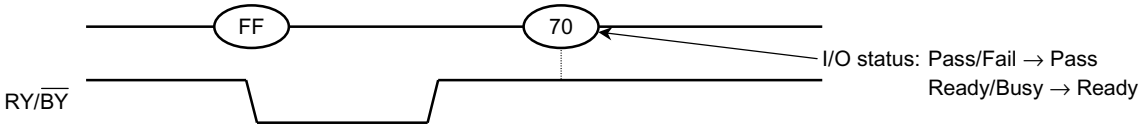
When a Reset (FFH) command is input during a Read operation

Figure 10.

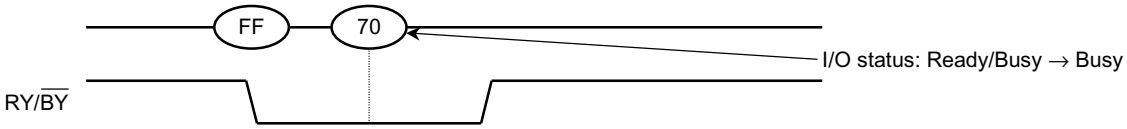


When a Status Read command (70H) is input after a Reset

Figure 11.

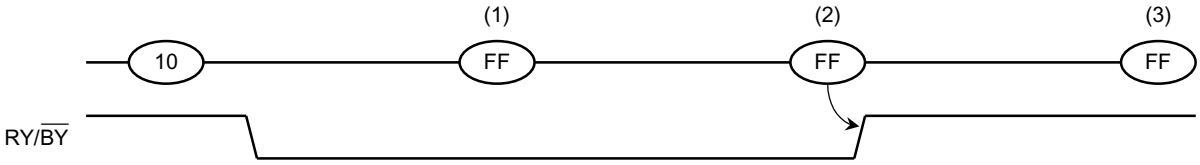


However, the following operation is prohibited. If the following operation is executed, correct resetting of the address and data register cannot be guaranteed.



When two or more Reset commands are input in succession

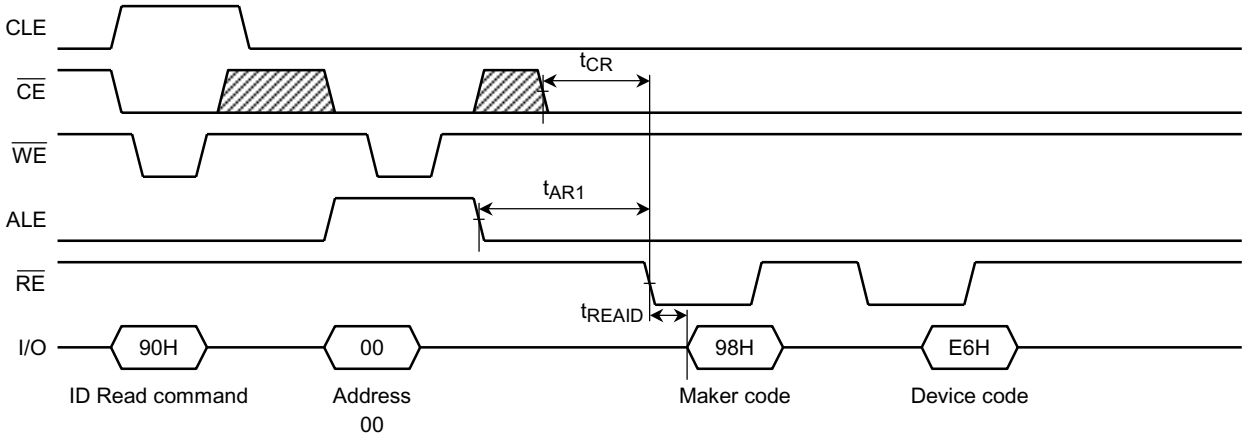
Figure 12.



The second FF command is invalid, but the third FF command is valid.

ID Read

The TC58V64A contains ID codes which identify the device type and the manufacturer. The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAID}, t_{CR} and t_{AR1} refer to the AC Characteristics.

Figure13. ID Read timing

Table 6. Code table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	1	1	1	0	0	1	1	0	E6H

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(3) Pointer control for 00H, 01H and 50H

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 7. Pointer Destination

Read Mode	Command	Pointer
(1)	00H	0~255
(2)	01H	256~511
(3)	50H	512~527

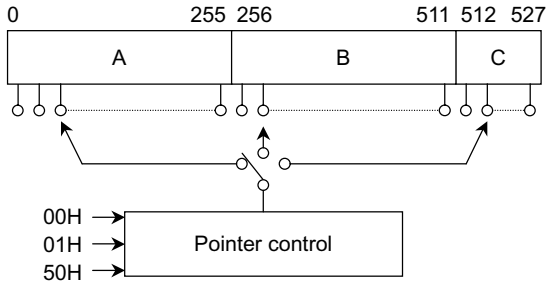
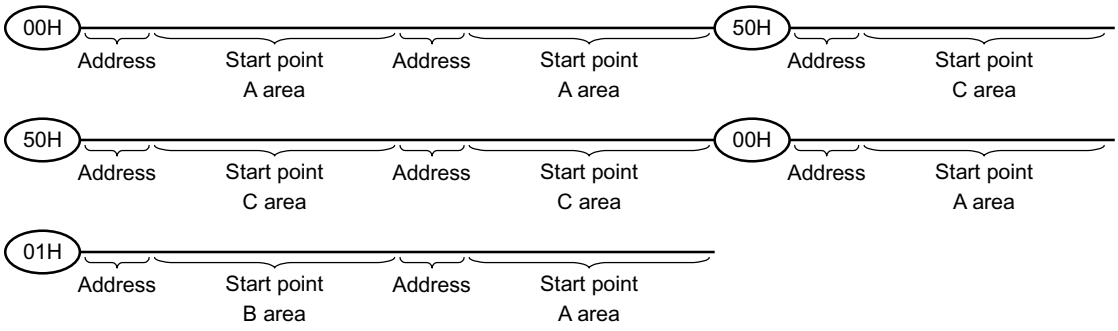


Figure 14. Pointer control

The pointer is set to region A by the 00H command, to region B by the 01H command, and to region C by the 50H command.

(Example)

The 00H command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50H command.

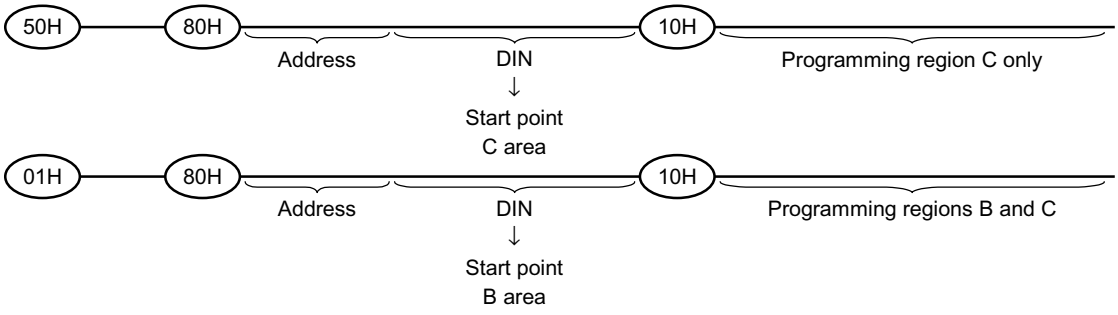


Figure 15. Example of How to Set the Pointer

(4) Acceptable commands after Serial Input command 80H

Once the Serial Input command 80H has been input, do not input any command other than the Program Execution command 10H or the Reset command FFH.

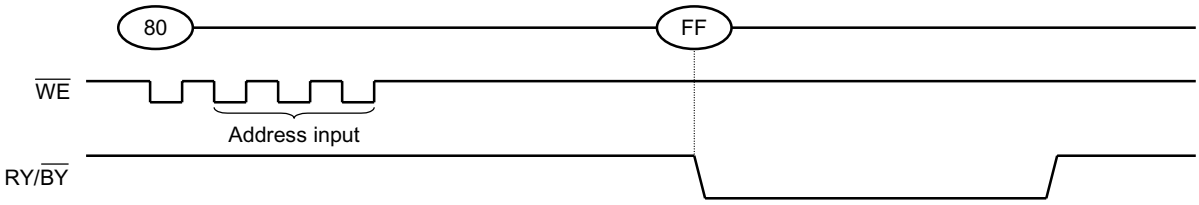
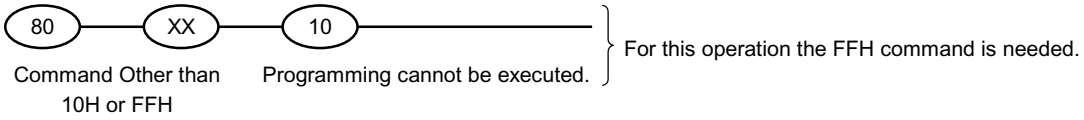


Figure 16.

If a command other than 10H or FFH is input, the Program operation is not performed.



(5) Status Read during a Read operation

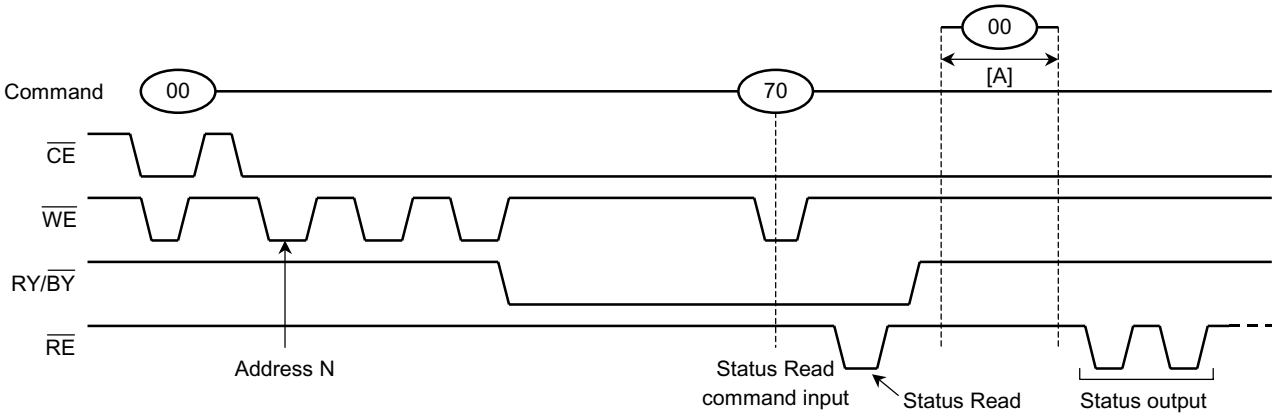


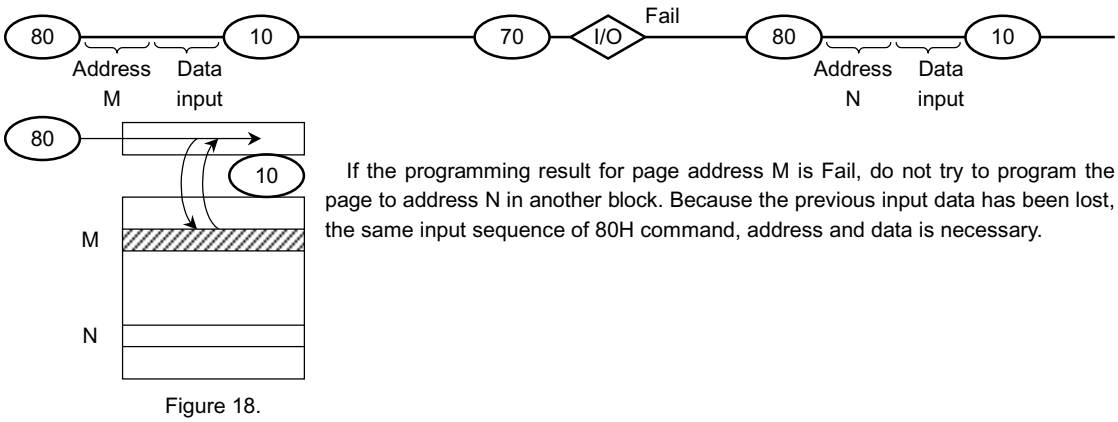
Figure 17.

The device status can be read out by inputting the Status Read command 70H in Read mode. Once the device has been set to Status Read mode by a 70H command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command 00H is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(6) Auto programming failure



If the programming result for page address M is Fail, do not try to program the page to address N in another block. Because the previous input data has been lost, the same input sequence of 80H command, address and data is necessary.

Figure 18.

(7) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.

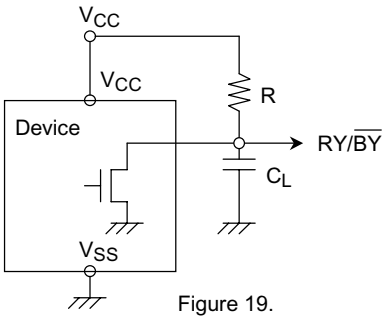
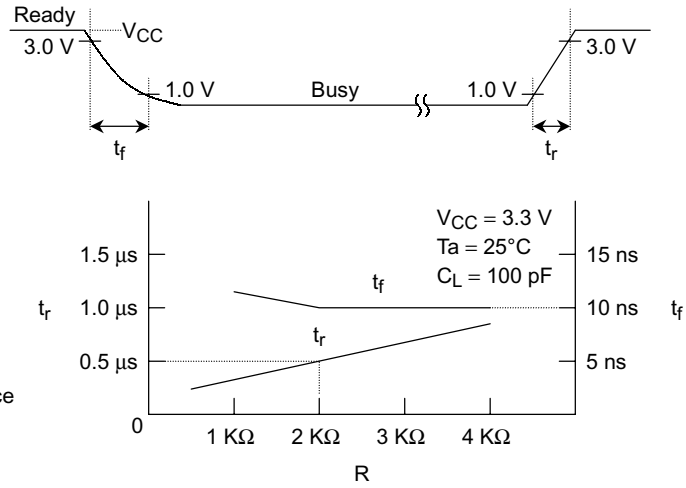


Figure 19.



This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

(8) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

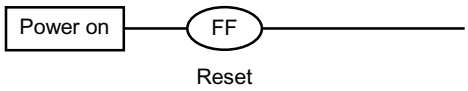


Figure 20.

(9) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary:

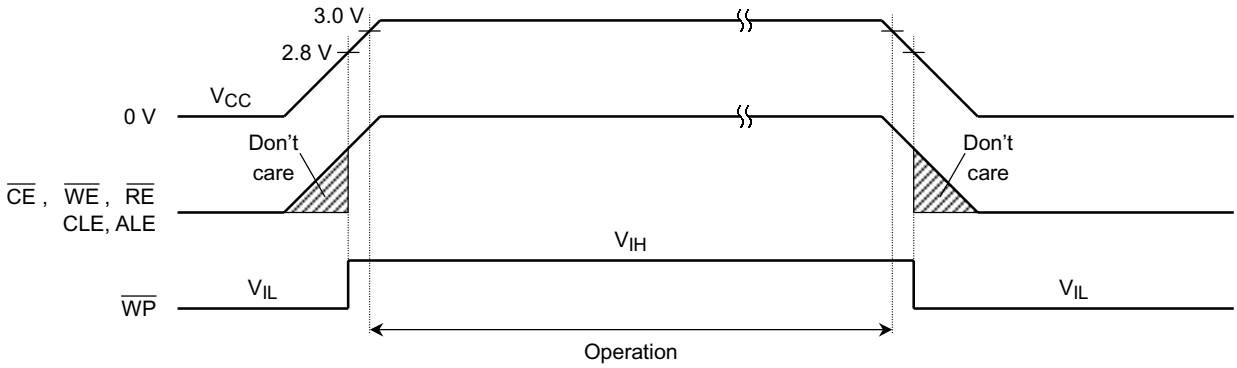
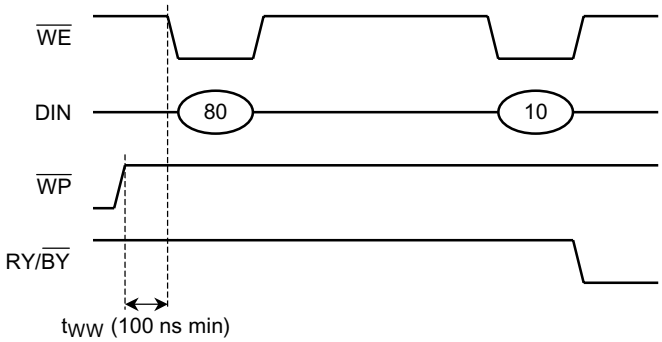


Figure 21. Power-on/off Sequence

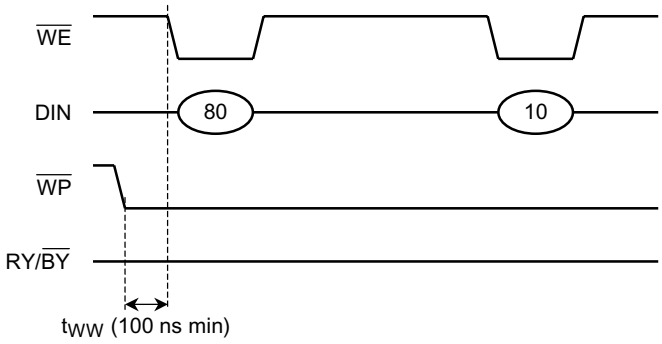
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

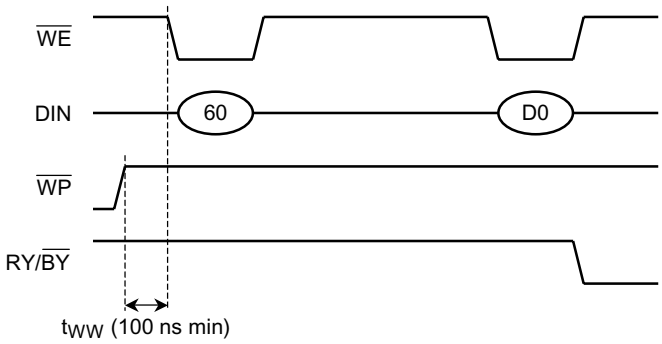
Enable Programming



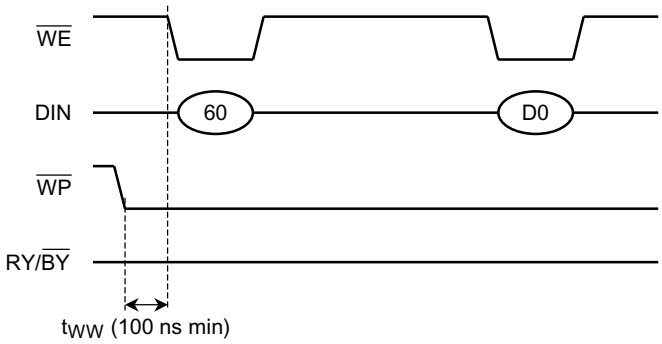
Disable Programming



Enable Erasing



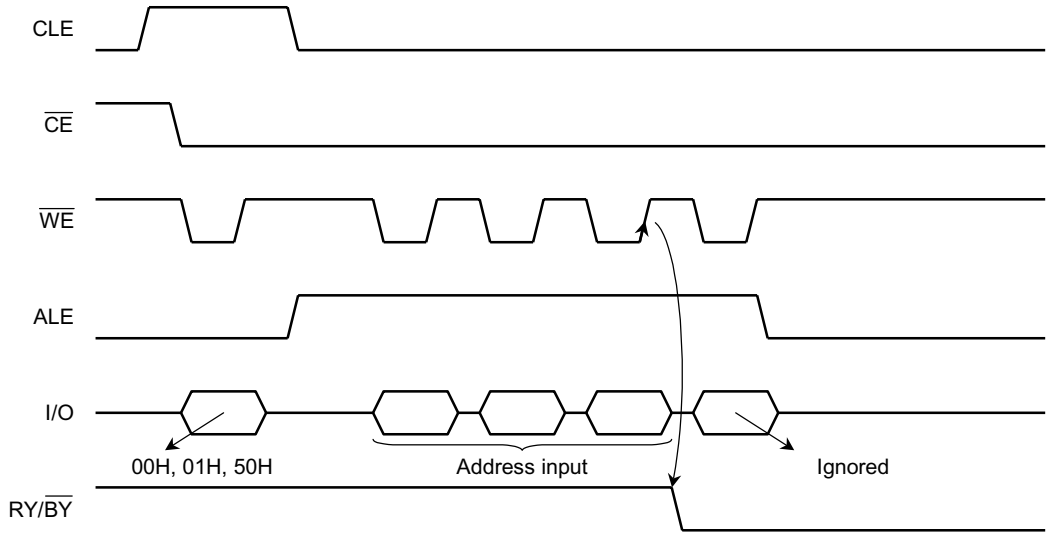
Disable Erasing



(11) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when $\overline{WE}$ goes High in the third cycle.

Figure 22.

Program operation

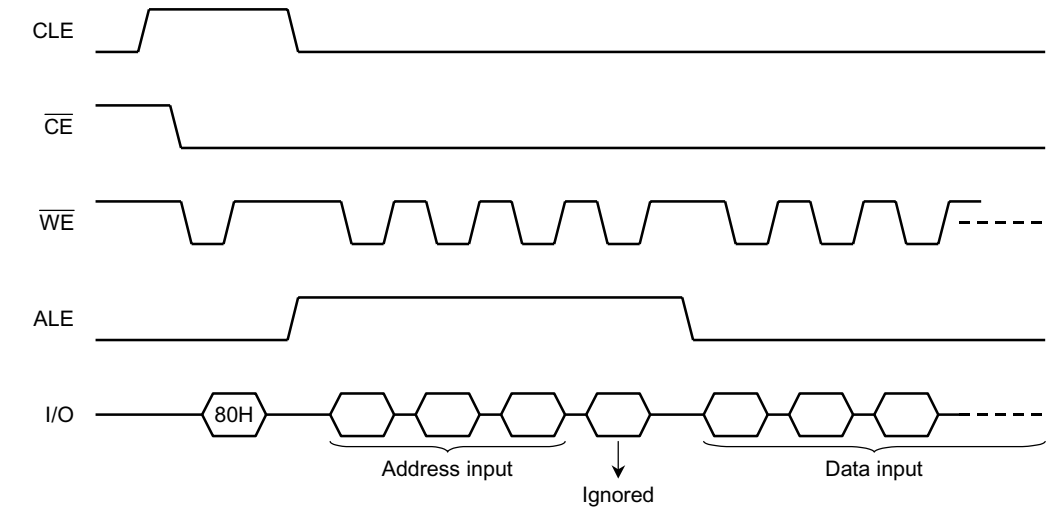


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as follows:

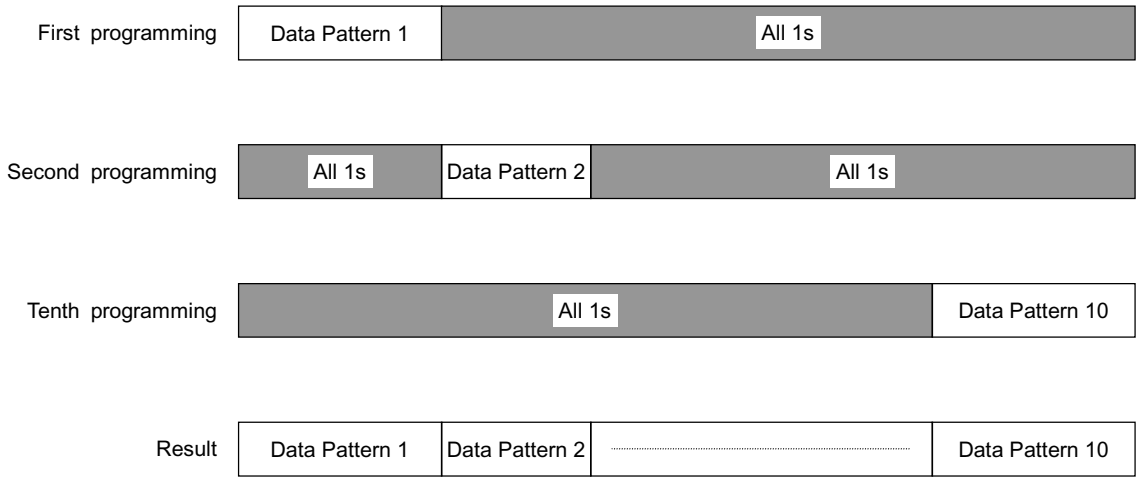


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be 1 (i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all 1).

(13) Note regarding the $\overline{RE}$ signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a 00H, 01H or 50H command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing. If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array → register) will occur and the device will enter Busy state. (Refer to Figure 25.)

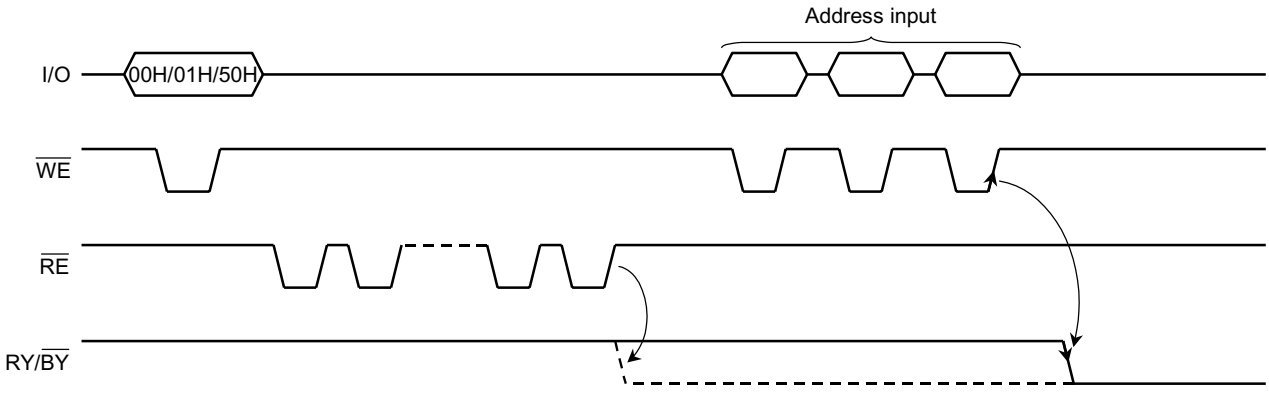


Figure 25.

Hence the $\overline{RE}$ clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, the following issues must be recognized:

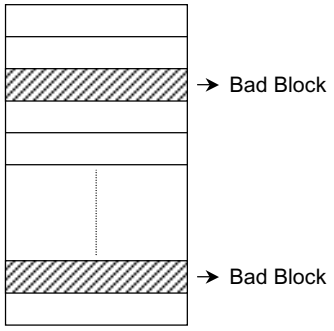


Figure 26.

Referring to the Block status area in the redundant area allows the system to detect bad blocks in the accordance with the physical data format issued by the SSFDC Forum. Detect the bad blocks by checking the Block Status Area at the system power-on, and do not access the bad blocks in the following routine.

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1014	—	1024	Block

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	(1) Block Verify after Program → Retry
		(2) ECC

- ECC: Error Correction Code
- Block Replacement

Program

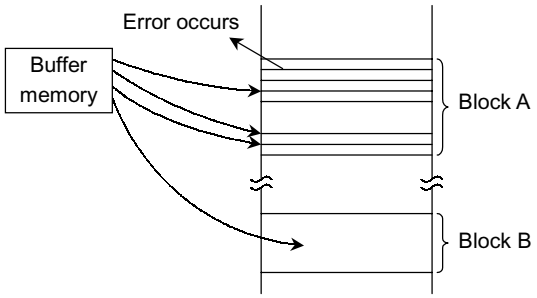


Figure 27.

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Erase

When an error occurs for an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) Chattering of Connector

There may be contact chattering when the TC58V64ADC is inserted or removed from a connector.
This chattering may cause damage to the data in the TC58V64ADC. Therefore, sufficient time must be allowed for contact bouncing to subside when a system is designed with SmartMedia™.

(17) The TC58V64ADC is formatted to comply with the Physical and Logical Data Format of the SSFDC Forum at the time of shipping.

Handling Precaution

(1) Avoid bending or subjecting the card to sudden impact.

(2) Avoid touching the connectors so as to avoid damage from static electricity.
This card should be kept in the antistatic film case when not in use.

(3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data corruption that may occur because of mishandling.

SSFDC Forum

The SSFDC Forum is a voluntary organization intended to promote the SmartMedia™, a small removable NAND flash memory card. The SSFDC Forum standardized the following specifications in order to keep the compatibility of SmartMedia™ in systems. The latest specifications issued by the Forum must be referenced when a system is designed with SmartMedia™, especially with large capacity SmartMedia™.

SmartMedia™ Electrical Specifications
SmartMedia™ Physical Format Specification
SmartMedia™ Logical Format Specification

Some electrical specifications in this data sheet show differences from the Forum's electrical specification. Complying with the Forum's electrical specification maintains compatibility with other SmartMedias.

Please refer folloing SSFDC Forum's URL to get the detailed information of each specification.

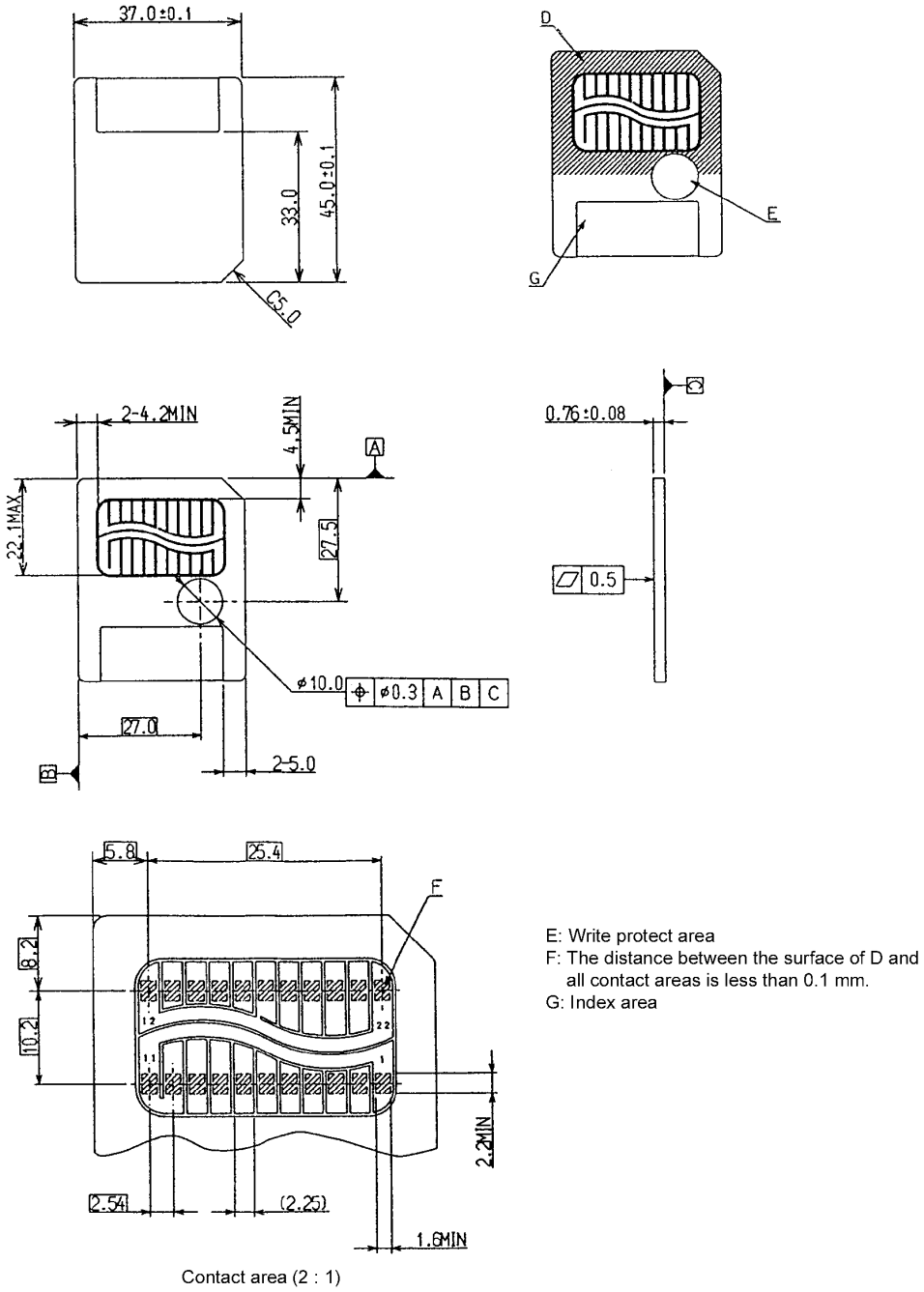
URL http://www.ssfdc.or.jp

PACKAGE DIMENSIONS

- FDC-22A

Unit: mm

FDC-22A



E: Write protect area
F: The distance between the surface of D and all contact areas is less than 0.1 mm.
G: Index area

Contact area (2 : 1)