

## HIGH VOLTAGE HALF BRIDGE

### Features

- Output Power IGBT's in half-bridge configuration
- 600V rated breakdown voltage
- High side gate drive designed for bootstrap operation
- Matched propagation delay for both channels
- Independent high and low side output channels (IR062HD4C10U-P2) or cross-conduction prevention logic (IR082HD4C10U-P2)
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Metal heatsink back for improved  $P_D$

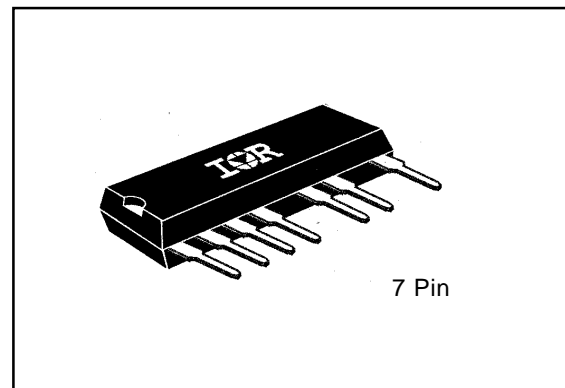
### Description

The IR062HD4C10U-P2 / IR082HD4C10U-P2 are high voltage, high speed half bridges. Proprietary HVIC and latch immune CMOS technologies, along with the power IGBT technology, enable ruggedized single package construction. The logic inputs are compatible with standard CMOS or LSTTL outputs. The front-end features an independent high and low side driver in phase with the logic compatible input signals. The output features two IGBT's in a half-bridge configuration. Propagation delays for the high and low side power IGBT's are matched to simplify use. The device can operate up to 600 volts.

### Product Summary

<b>V<sub>IN</sub> (max)</b>	<b>600V</b>
<b>P<sub>D</sub> (T<sub>A</sub> = 25°C)</b>	<b>3.0W</b>
<b>V<sub>CE(ON)</sub> typ</b>	<b>3.0V</b>

### Package

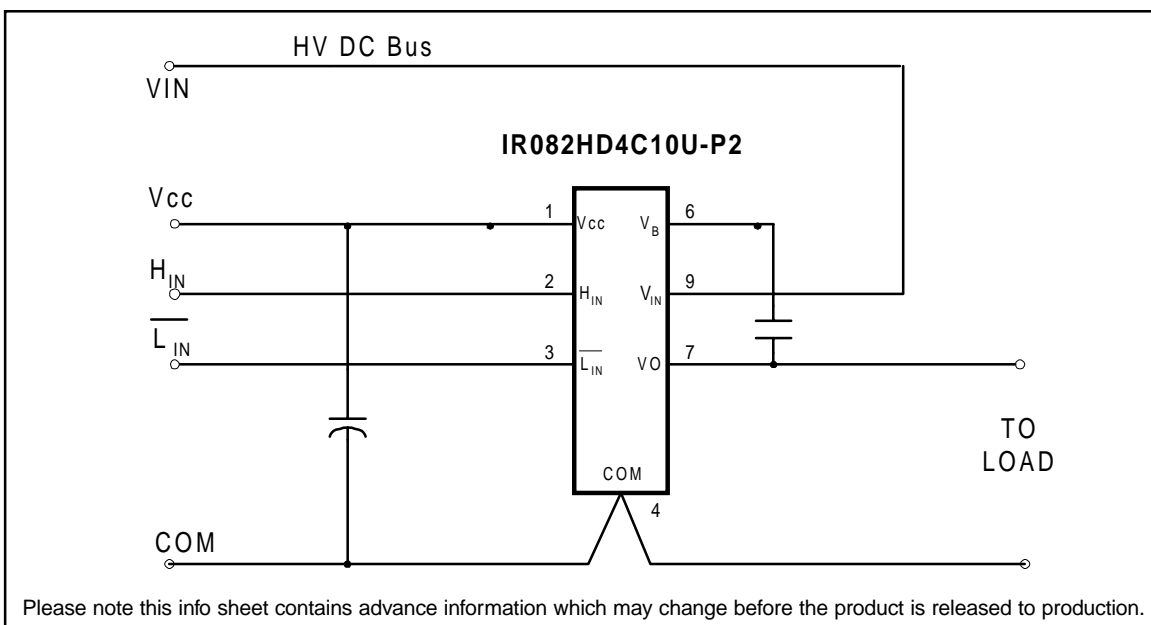
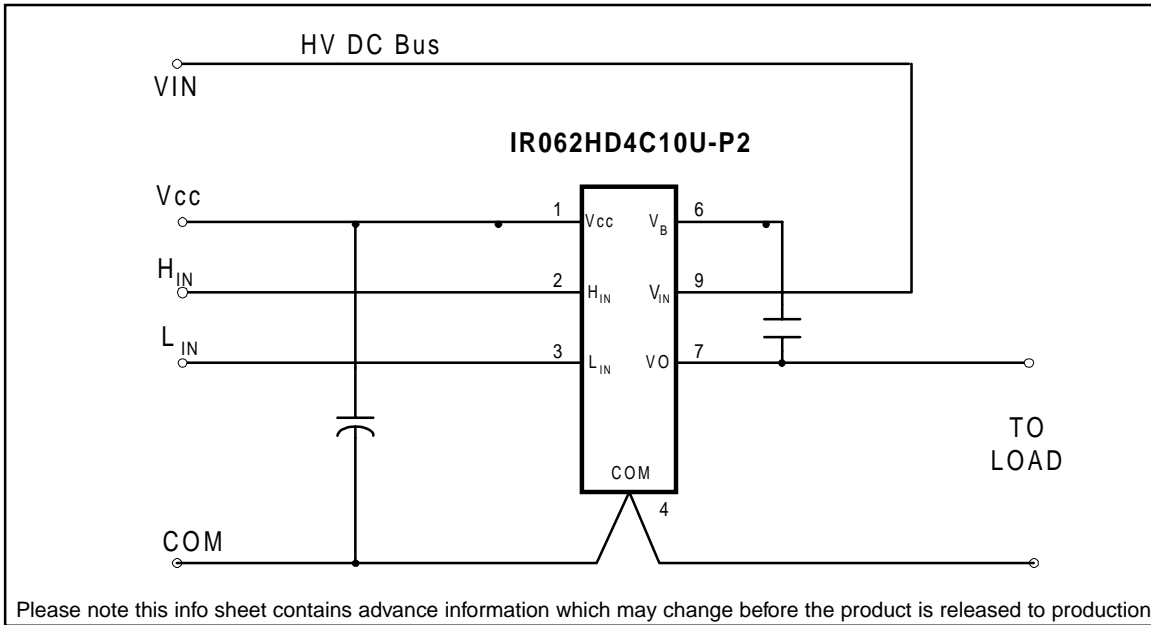


# IR062HD4C10U-P2

# IR082HD4C10U-P2

International  
**IR** Rectifier

## Typical Connections



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>IN</sub>	High voltage supply	- 0.3	600	V
V <sub>B</sub>	High side floating supply absolute voltage	VO -0.3	VO+ 25	
V <sub>O</sub>	Half-bridge output voltage	-0.3	V <sub>IN</sub> + 0.3	
V <sub>IH</sub> /V <sub>IL</sub>	Logic input voltage (HIN & LIN)	- 0.3	V <sub>CC</sub> + 0.3	
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25	
dV/dt	Peak diode recovery dv/dt	—	3.50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	—	3.00	W
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	50	°C/W
R <sub>thJC</sub>	Thermal resistance, junction to case (metal)	—	20	
T <sub>J</sub>	Junction temperature	-55	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>O</sub> + 10	V <sub>O</sub> + 20	V
V <sub>IN</sub>	High voltage supply	—	600	
V <sub>O</sub>	Half-bridge output voltage	(note 1)	V <sub>IN</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>IH</sub> /V <sub>IL</sub>	Logic input voltage (HIN & LIN)	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	A
I <sub>C</sub>	Continuous collector current (TC = 25 °C)	—	2.0	
	(TC = 85 °C)	—	1.1	

**Note 1:** Logic operational for V<sub>O</sub> of -5 to 600V. Logic state held for V<sub>O</sub> of -5 to -V<sub>BO</sub>

# IR062HD4C10U-P2

# IR082HD4C10U-P2

International  
 Rectifier

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A = 25^\circ\text{C}$  unless otherwise specified. Switching time waveform definitions are shown in figure 2. Refer to IC data sheets (IR2106 and IR2108) for further characteristics.

Symbol	Definition	$T_A = 25^\circ\text{C}$			Units	Test Conditions	
		Min.	Typ.	Max.			
$t_{on}$	Turn-on propagation delay (see note 2)	-IR062	—	220	310	ns	$V_o = 0V$
		-IR082	—	680	900		
$t_{off}$	Turn-off propagation delay (see note 2)	-IR062	—	257	380	ns	$V_o = 600V$
		-IR082	—	220	400		
$t_{rr}$	Reverse recovery time (FRED Diode)	—	28	—	nC	$I_F = 400mA$	
$Q_{rr}$	Reverse recovery charge (FRED Diode)	—	40	—		$di/dt = 100 A/us$	

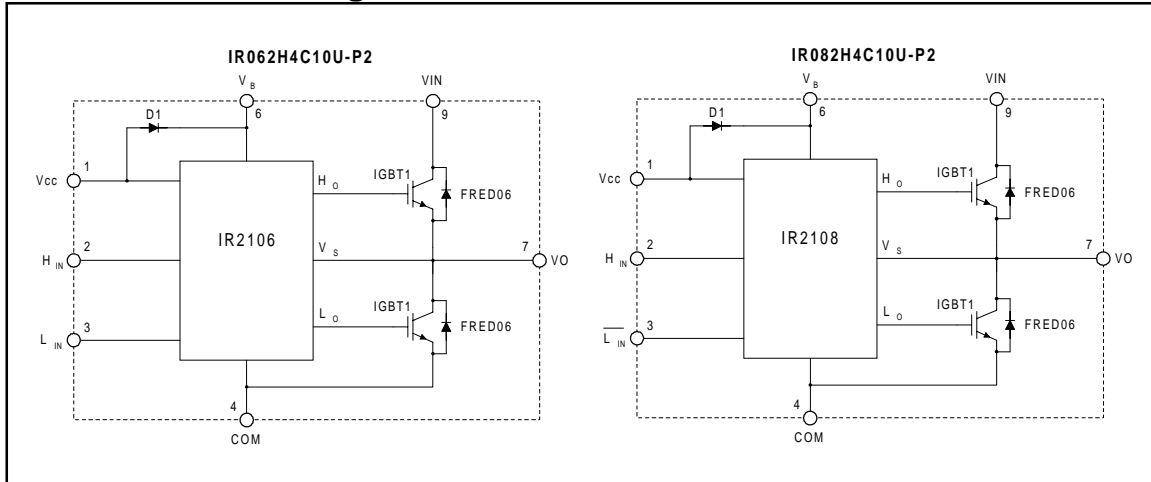
**Note 2:** Switching times as specified and illustrated in figure 2 are referenced to the  $V_O$  output voltage. This is shown as  $V_O$  in figure 2.

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM.

Symbol	Definition	$T_A = 25^\circ\text{C}$			Units	Test Conditions
		Min.	Typ.	Max.		
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$I_{QCC}$	Quiescent $V_{CC}$ supply current	0.4	1.0	1.6	mA	
$I_{QBO}$	Quiescent $V_{BO}$ supply current	20	60	150	$\mu A$	
$I_{LK}$	Offset supply leakage current @25°C	—	—	100		$V_B = 600V$
$I_{INLK}$	$V_{in}$ to $V_O$ leakage current @25°C	—	—	250		$V_{IN} = 600V$ , $V_O = 0V$
		@150°C	—	1000		
$I_{OLK}$	$V_O$ leakage current @25°C	—	—	250		$V_O = 600V$
		@150°C	—	1000		
$V_{IH}$	Logic "1" input voltage	2.7	—	—	V	$V_{CC} = 10V$ to $20V$
$V_{IL}$	Logic "0" input voltage	—	—	0.8		
$I_{IN+}$	Logic "1" input bias current	—	20	40	$\mu A$	$V_{IN} = 5V$
$I_{IN-}$	Logic "0" input bias current	—	—	1		
$V_{CE(on)}$	Collector-to-Emitter saturation voltage	—	3.0	—	V	$I_C = 400mA$
$V_{EC}$	Diode forward voltage	—	1.2	—		$I_E = 400mA$
$V_F$	Bootstrap Diode forward voltage (D1)	—	1.5	—		$I_F = 400mA$

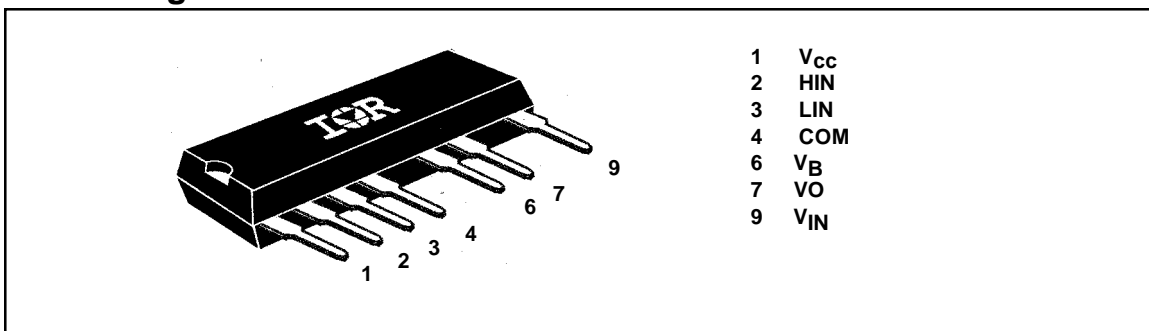
### Functional Block Diagram



### Lead Definitions

Lead	
Symbol	Definition
$V_{CC}$	Logic and internal gate drive supply voltage.
HIN	Logic input for high side half bridge output, in phase
LIN	Logic input for low side half bridge output, in phase (IR062xxx) or out of phase (IR082xxx)
$V_B$	High side gate drive floating supply
$V_{IN}$	High voltage supply
VO	Half bridge output
COM	Logic return and half bridge return

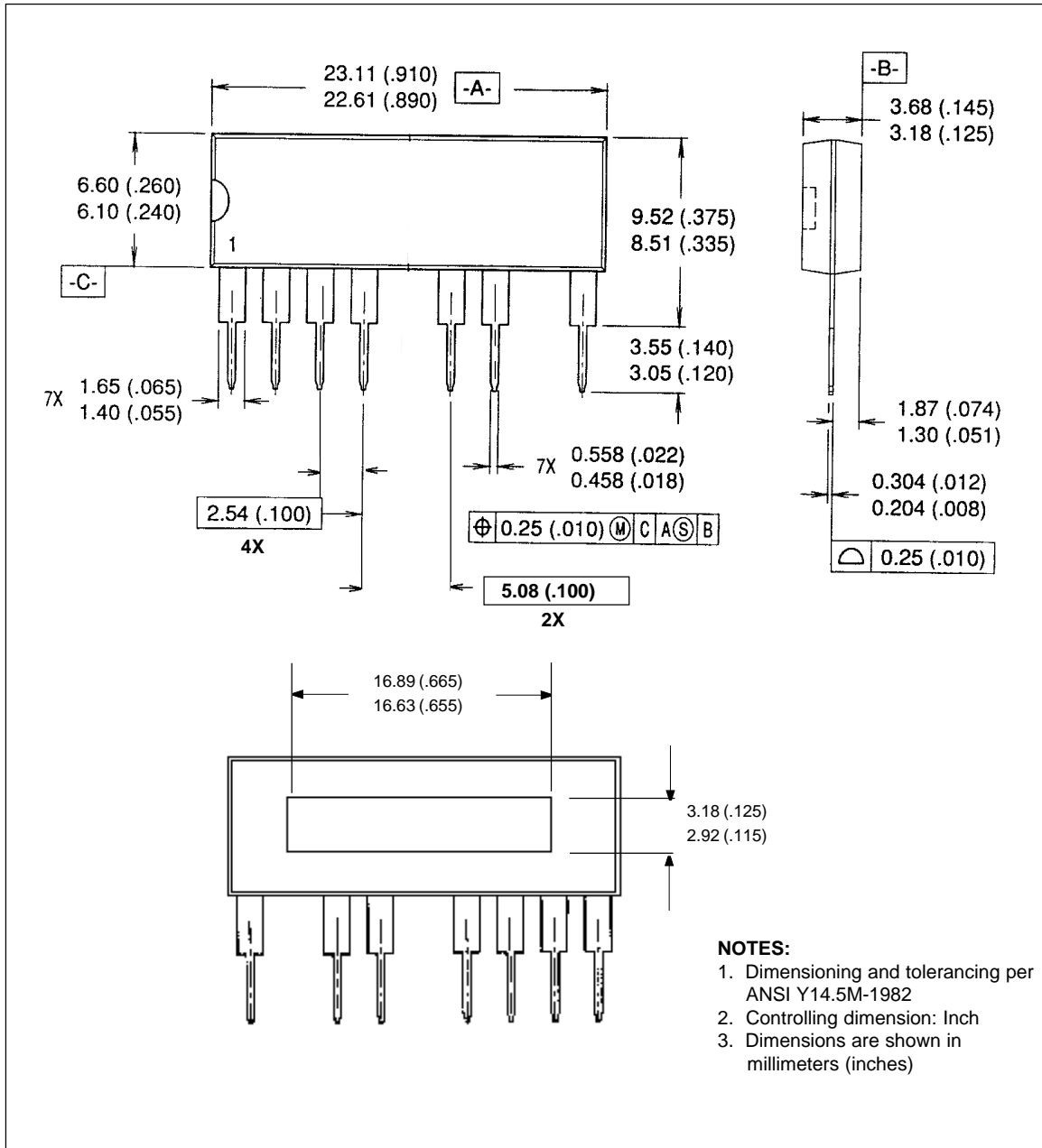
### Lead Assignments

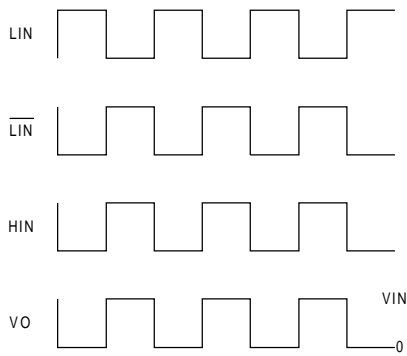


**IR062HD4C10U-P2**  
**IR082HD4C10U-P2**

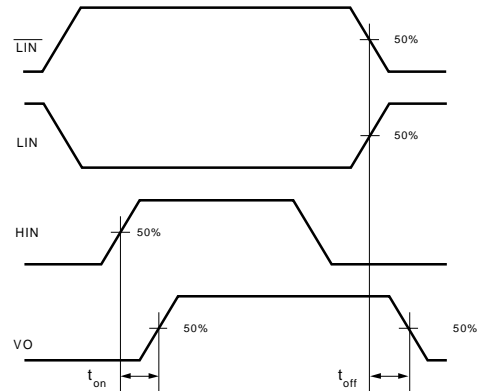
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**Figure 1. Input/Output Timing Diagram**



**Figure 2. Switching Time Waveform Definitions**