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Type	Silicon Monolithic Bipolar IC
Package	36-USO Pin Plastic Package (USONF-36D)
Application	IC for Color TV
Function	4-Input AV Switch IC

A Absolute Maximum Ratings					
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	° C	1
2	Operating Ambient Temperature	Topr	-20 ~ +70	° C	1
3	Operating Ambient Pressure	Popr	$1.013 \times 10^5 \pm 0.61 \times 10^5$	Pa	
4	Operating Constant Acceleration	Gopr	9810	m/s <sup>2</sup>	
5	Operating Shock	Sopr	4900	m/s <sup>2</sup>	
6	Power Supply Voltage	Vcc	14	V	
7	Power Supply Current	Icc	60	mA	
8	Power Dissipation	Pd	840	mW	

Operating Supply Voltage Range	Vcc	8.1V ~ 9.9V
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Note 1) The temperature of all items shall be Ta = 25° C except storage temperature and operating ambient temperature



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**B** Electrical Characteristics  
(VCC=9V, unless otherwise specified, the ambient temperature is 25° C ± 2° C)

No	Item	Symbol	Test cct	Conditions	Limit			Unit	Note
					Min	Typ	Max		
1	Quiescent Current [VIDEO BLOCK]	I <sub>CO</sub>	1	No Input	20	28	40	mA	
2	Video Gain (OUT1)	G <sub>V</sub>	1	f= 15kHz, V <sub>in</sub> = 0.5Vp-p	5.3	6.0	6.7	dB	
	Video Gain Y/Cin (OUT1)	G <sub>VYC</sub>	1	f= 15kHz, V <sub>in</sub> = 0.5Vp-p	-0.5	0	0.5	dB	
3	Video Frequency Characteristics	f	1	f= 100kHz, V <sub>in</sub> = 0.5Vp-p As reference 0dB, measure the frequency at output -3dB point.	20	30	-	MHz	
	Video Frequency Characteristics YCMix ( Vout )	f <sub>Mix</sub>	1	f= 100kHz, V <sub>in</sub> = 0.5Vp-p As reference 0dB, measure the frequency at output -3dB point.	20	30	-	MHz	
4	Input Dynamic Range	V <sub>D</sub>	1	f= 20kHz, maximum input when output at THD < 2.0%.	2.0	2.4	-	Vp-p	
5	Video Crosstalk	C <sub>M</sub>	1	f= 5MHz, V <sub>in</sub> = 1Vp-p	50	60	-	dB	
	V and Y Crosstalk	C <sub>VY</sub>			35	40	-		
	V and C Crosstalk	C <sub>VC</sub>			35	40	-		
	Y and C Crosstalk	C <sub>YC</sub>			35	40	-		
6	Mute Ratio	MR <sub>V</sub>	1	V <sub>in</sub> = 0.5Vp-p, f=15kHz	40	50	-	dB	

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**B Electrical Characteristics**  
(VCC=9V, unless otherwise specified, the ambient temperature is 25° C ± 2° C)

No	Item	Symbol	Test cct	Condition	Limit			Unit	Note
					Min	Typ	Max		
	[AUDIO BLOCK]								
7	Audio Gain	$G_{A0}$	1	f= 1kHz, Vin = 1Vp-p	-0.5	0	0.5	dB	
		$G_{A6}$	1	f= 1kHz, Vin = 1Vp-p	5.5	6.0	6.5	dB	
8	Audio Frequency Characteristics	$f_A$	1	f= 1kHz, Vin = 1Vp-p as reference 0dB, measure the frequency at output -3dB point.	35	40	-	kHz	
9	Input Dynamic Range	$V_{DVA}$	1	Gain setting = 0dB f=1kHz, maximum input when output at THD < 1.5%, at 0dB Mode.	2.8	2.9	-	Vrms	
10	Source Crosstalk	$C_A$	1	f= 1kHz, Vin = 1Vp-p	80	85	-	dB	
	Channel Crosstalk	$C_{LR}$		Din Audio	80	85	-		
11	Mute Ratio	$MR_A$	1	f= 1kHz, Vin = 1Vp-p Din Audio	80	-	-	dB	
	[IIC Interface]								
11	Suction current during ACK	$I_{ACK}$	1	Max. suction current value of Pin 36 at 0.4V	3.0	10	-	mA	
12	SCL, SDA signal input high level	$V_{IHI}$	1		3.0	-	5.5	V	
13	SCL, SDA signal input low level	$V_{ILO}$	1		0	-	1.5	V	
14	Max. frequency allowable to input	$f_{imax}$	1		-	-	100	kbit/s	

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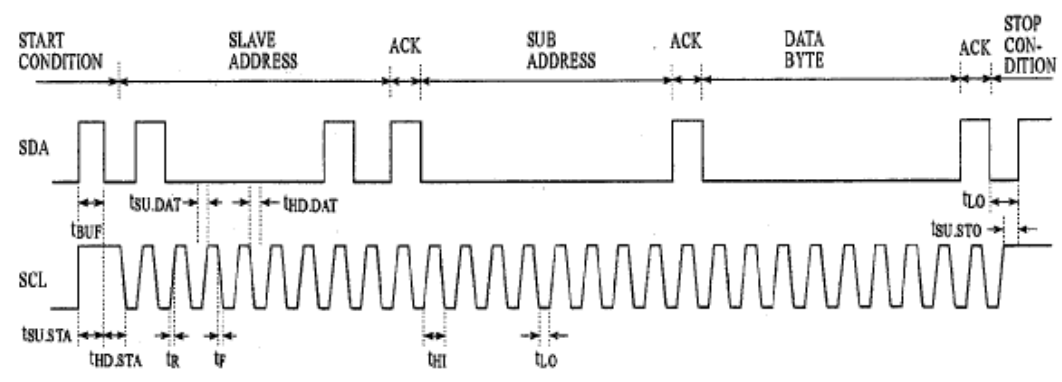
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No	Item	Symbol	Test cct	Condition	Limit			Unit	Note
					Min	Typ	Max		
[IIC Interface]									
1	Bus free before start	$t_{BUF}$			4.0	-	-	$\mu s$	
2	Start condition set-up time	$t_{SU, STA}$			4.0	-	-	$\mu s$	
3	Start condition hold time	$t_{HD, STA}$			4.0	-	-	$\mu s$	
4	Low period SCL, SDA	$t_{LO}$			4.0	-	-	$\mu s$	
5	High period SCL	$t_{HI}$			4.0	-	-	$\mu s$	
6	Rise time SCL, SDA	$t_R$			-	-	1.0	$\mu s$	
7	Fall time SCL, SDA	$t_F$			-	-	0.35	$\mu s$	
8	Data set-up time (write)	$t_{SU, DAT}$			0.25	-	-	$\mu s$	
9	Data hold time (write)	$t_{HD, DAT}$			0	-	-	$\mu s$	
10	Acknowledge set-up time	$t_{SU, ACK}$			-	-	3.5	$\mu s$	
11	Acknowledge hold time	$t_{HD, ACK}$			0	-	-	$\mu s$	
12	Stop condition set-up time	$t_{SU, STO}$			4.0	-	-	$\mu s$	



Note) The above characteristics are reference values on IC designing and not guaranteed by shipping inspection.

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B Electrical Characteristics (VCC=9V, unless otherwise specified, the ambient temperature is 25° C ± 2° C)									
No	Item	Symbol	Test cct	Condition	Limit			Unit	Note
					Min	Typ	Max		
	[Video Block]								
13	Total Harmonic Distortion 1	THD <sub>V</sub>	1	V <sub>in</sub> = 0.5V <sub>p-p</sub> , f = 20kHz	-	0.4	1.0	%	
	[Audio Block]								
14	Total Harmonic Distortion 2	THD <sub>A</sub>	1	Gain Setting = 0dB V <sub>in</sub> = 1V <sub>rms</sub> , f = 1kHz Din Audio	-	0.02	0.3	%	

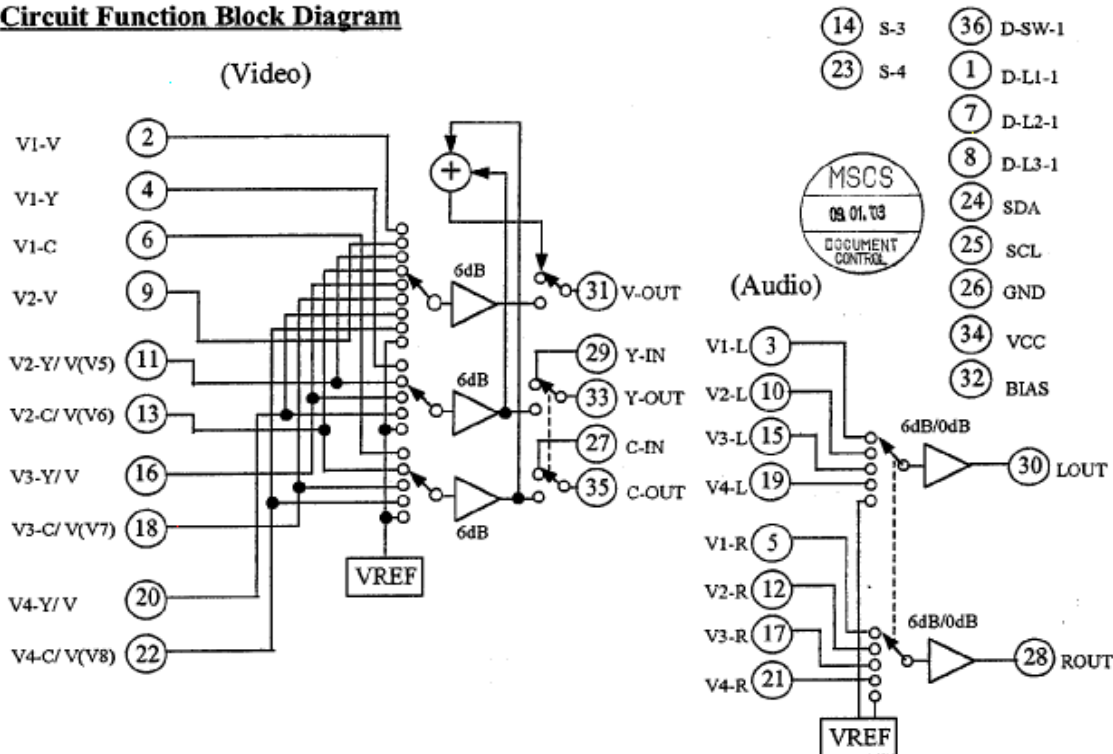
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**Circuit Function Block Diagram**



**Pin Descriptions**

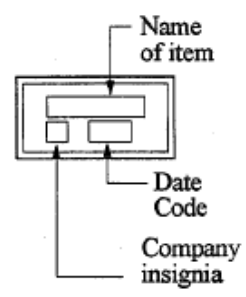
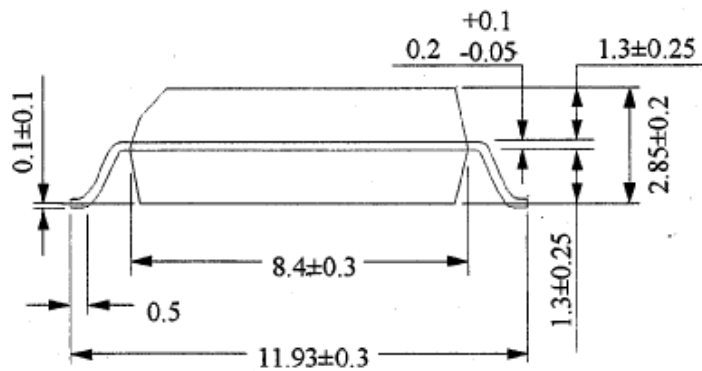
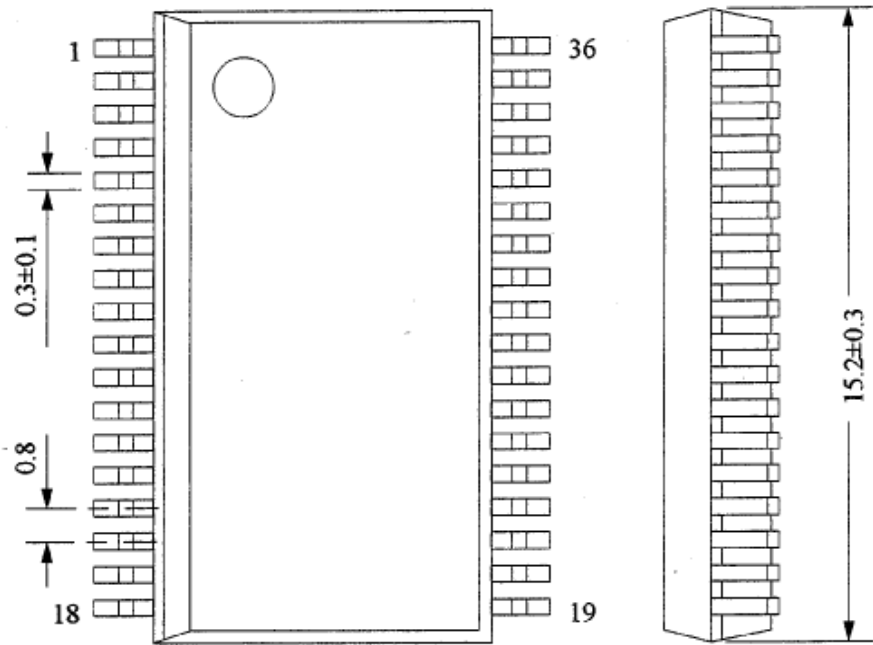
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	D-L1-1	13	V2-C/ V(V6) Input	25	SCL
2	V1-V Input	14	S-3 Input	26	GND
3	V1-L Input	15	V3-L Input	27	CIN
4	V1-Y Input	16	V3-Y/ V Input	28	ROUT
5	V1-R Input	17	V3-R Input	29	YIN
6	V1-C Input	18	V3-C/ V(V7) Input	30	LOUT
7	D-L2-1	19	V4-L Input	31	VOUT
8	D-L3-1	20	V4-Y/ V Input	32	BIAS
9	V2-V Input	21	V4-R Input	33	YOUT
10	V2-L Input	22	V4-C/ V(V8) Input	34	VCC
11	V2-Y/ V(V5) Input	23	S-4	35	COUT
12	V2-R Input	24	SDA	36	D-SW-1

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Package Name USONF-36D

Unit : mm



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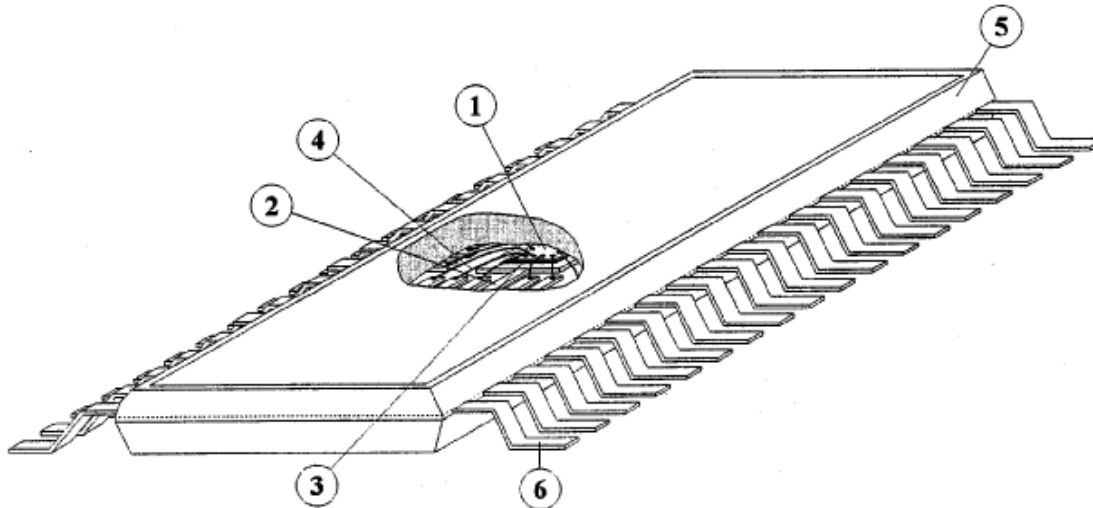
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**(Structure Description)**



Chip surface passivation	SiN,	PSG,	Others ( )	①
Lead frame material	Fe group,	Cu group,	Others ( )	②, ⑥
Inner lead surface process	Ag plating,	Au plating,	Others ( )	②
Outer lead surface process	Solder plating,	Solder dip,	Others ( )	⑥
Chip mounting method	Ag paste,	Au-Si alloy, Solder,	Others ( )	③
Wire bonding method	Ultrasonic heat bonding,		Others ( )	④
Wire material	Au,	Diameter 24 μm	Others ( )	④
Mold material	Epoxy,		Others ( )	⑤
Molding method	Transfer mold,	Multiplunger mold,	Others ( )	⑤

**Package USONF-36D**



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Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
1 7 8	D-L1-1 D-L2-1 D-L3-1	0V	•Aspect Detection Pins	
2 4 6 9 11 13 16 18 20 22	V1-V V1-Y V1-C V2-V V2-Y V2-C V3-Y V3-C V4-Y V4-C	4.5V	•Video Signal Input Pins  •V : Video •Y : Luminance •C : Chrominance	
3 5 10 12 15 17 19 21	V1-L V1-R V2-L V2-R V3-L V3-R V4-L V4-R	4.5V	•Audio Signal Input Pins  •L : Left Channel •R : Right Channel	

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Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
14 23	S3 S4	- -	•S2 protocol compatible pins	
24	SDA	-	•IIC Bus Data Input Pin	
25	SCL	-	•IIC Bus Clock Input Pin	

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Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
26	GND	0V	•Ground Pin	
27 29	C-IN Y-IN	4.5V	•Video Signal Input Pins	
28 30	ROUT LOUT	4.5V	•Audio Signal Output Pins	

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Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
31	VOUT	4.5V	•Video Signal Output Pin	
32	Bias	4.5V	•Audio System Reference Bias Pin	
33 35	YOUT COUT	4.5V	•Video Signal Output Pins	

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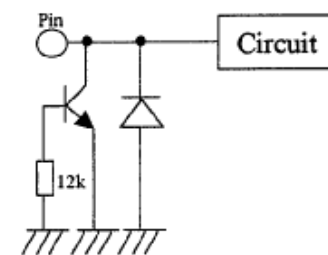
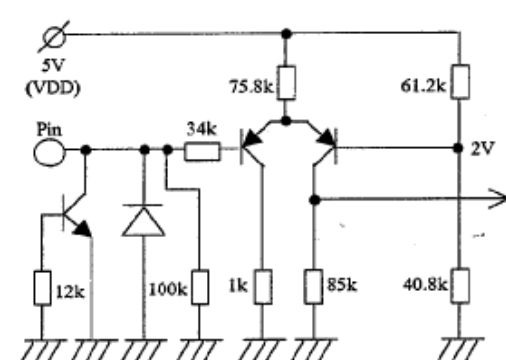
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Pin No.	Pin Name	Pin Voltage	Description	Equivalent Circuit
34	VCC	9V	•Power Supply Pin	
36	D-SW-1	-	•Pin Status Detection Pin	

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**[I<sup>2</sup>C BUS]**

**Write mode:** Master transmitter write data to slave receiver

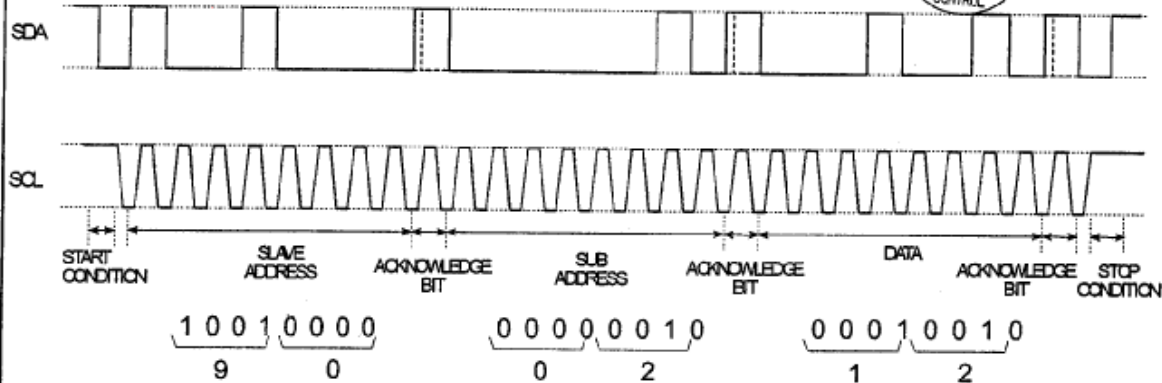


Fig.1 Example of transmission message

For transmission messages, both SCL and SDA are transferred in the form of synchronized serial transmission. SCL is a clock of a specific frequency, and SDA indicates address data for controlling the receiving side and is transferred in parallel, being synchronized with SCL. Data is transferred in principle in 3 octets (bytes), and each one octet (one octet = 8bits) includes one acknowledge bit. Frame structure is described below.

- (a) Start Condition     The receiver becomes possible to receive data when SDA changes from HI to LO while SCL is HI.
- (b) Stop Condition     The receiver halts receiving when SDA changes from LO to HI while SCL is HI.
- (c) Slave Address     This is an address which is determined for each device. If other device address is sent, receiving will be halted.
- (d) Sub Address        This is an address which is determined for each function.
- (e) Data                This is control data.
- (f) Acknowledge Bit    This is a bit by which the master acknowledges that data was successfully received in each octet. Master sends the HI signal and the receiver sends back the LO signal as shown in Figure1 with dotted line, causing the master to acknowledge the reception by the receiver. If the LO signal is not returned, communication will be halted.

Except Start and Stop conditions, SDA does not change while SCL is HI.

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**[I<sup>2</sup>C BUS]**

**Read mode:** Master read data from slave.

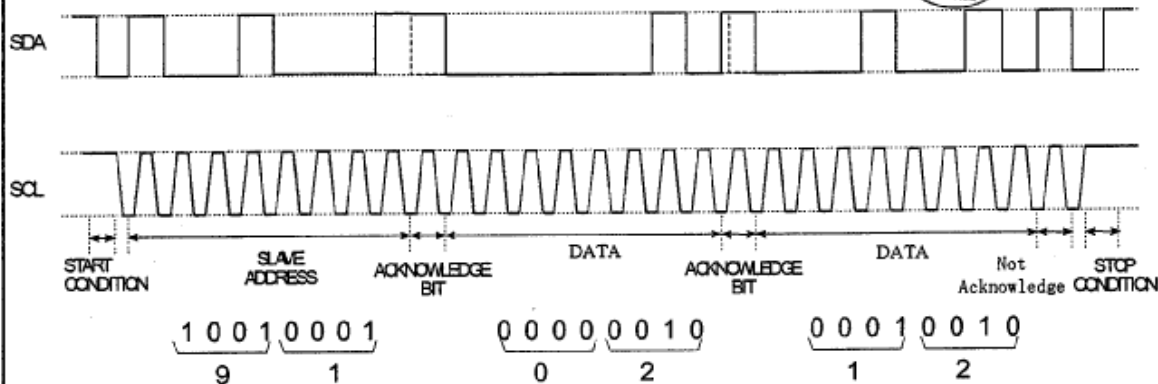


Fig 2. Example of Receiving message

- (a) Start Condition     The receiver becomes possible to receive data when SDA changes from HI to LO while SCL is HI.
- (b) Stop Condition     The receiver halts receiving when SDA changes from LO to HI while SCL is HI.
- (c) Slave Address     This is an address which is determined for each device. If other device address is sent, receiving will be halted.
- (d) Data                 This is control data.
- (f) Acknowledge bit     The first acknowledge (after the slave address) is generate by the slave, the rest of acknowledge (after the data byte) is generate by the master.

Except Start and Stop conditions, SDA does not change while SCL is HI.

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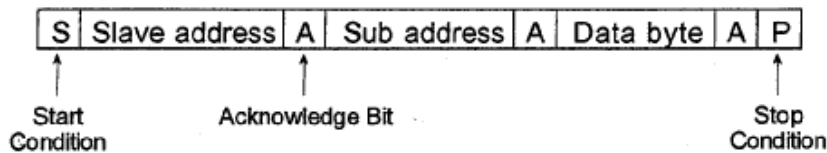
[I<sup>2</sup>C BUS ADDRESSING]

(1) Auto-increment function present :

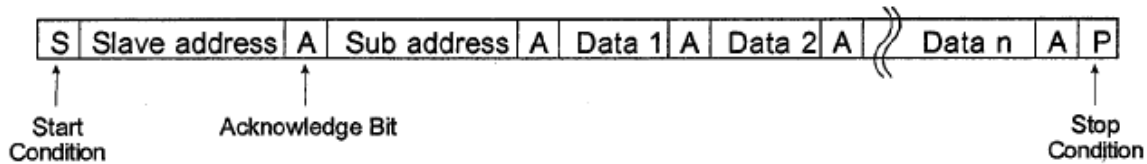
- Sub address 0 \* \* \* \* \* : Auto-Increment Mode  
(When the data is sent in consecutive order, the Sub-address will be changed in consecutive order, as data is input )
- Sub address 1 \* \* \* \* \* : Data Update Mode  
(When the data is sent consecutively, it is sent to the same Sub-address)

(2) I<sup>2</sup>C BUS PROTOCOL (Write mode)

- Slave address : 10010000 (90H)
- Format (Usual)

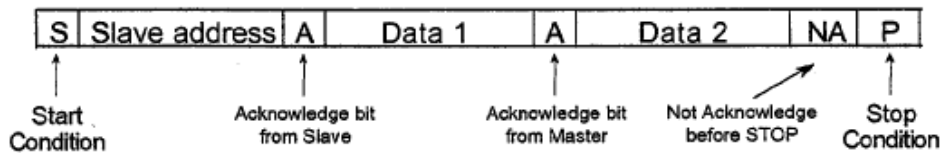


- Auto-Increment Mode/Data Update Mode



(3) I<sup>2</sup>C BUS PROTOCOL (Read mode)

- Slave address : 10010001 (91H)
- Format



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**I2C Bus Specification:**

**Control Register**

Sub address	D7	D6	D5	D4	D3	D2	D1	D0
Slave	1	0	0	1	0	0	0	R/W
00	Audio Mute	Video C Mute	Video Y Mute	Video V Mute	Y/C Mix	Video V-OUT select		
01	Video Y/C-IN	Audio Gain	Audio OUT select		Video C-OUT select		Video Y-OUT select	

**Video V-OUT select**

00/D2	00/D1	00/D0	00/D4	00/D3	Video V-OUT
0	0	0	0	0	V1-V
0	0	1	0	0	V2-V
0	1	0	0	0	V2-Y
0	1	1	0	0	V2-C
1	0	0	0	0	V3-Y
1	0	1	0	0	V3-C
1	1	0	0	0	V4-Y
1	1	1	0	0	V4-C
X	X	X	0	1	YC MIX
X	X	X	1	0	MUTE (DC)

**Video Y-OUT select**

01/D1	01/D0	00/D5	01/D7	Video Y-OUT
0	0	0	0	V1-Y
0	1	0	0	V2-Y
1	0	0	0	V3-Y
1	1	0	0	V4-Y
X	X	0	1	Y-IN
X	X	1	0	MUTE (DC)

**Video C-OUT select**

01/D3	01/D2	00/D6	01/D7	Video C-OUT
0	0	0	0	V1-C
0	1	0	0	V2-C
1	0	0	0	V3-C
1	1	0	0	V4-C
X	X	0	1	C-IN
X	X	1	0	MUTE (DC)

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**I2C Bus Specification:**

**Control Register**

**Audio OUT select**

01/D5	01/D4	00/D7	L-OUT	R-OUT
0	0	0	V1-L	V1-L
0	1	0	V2-L	V2-L
1	0	0	V3-L	V3-L
1	1	0	V4-L	V4-L
X	X	1	MUTE (DC)	MUTE (DC)

**Audio Gain select**

01/D6	L-OUT	R-OUT
1	6 dB	6 dB
0	0 dB	0 dB



**Status Register**

Sub address	D7	D6	D5	D4	D3	D2	D1	D0
00	S3 OPEN	S3 SEL	S4 OPEN	S4 SEL	-	D-pin	L1 scanning lines	
01	L2 i/p input		L3 Aspect Ratio		-	-	-	-

S Pins	Min	Typ	Max	Unit
S3/ S4 OPEN	4.5	-	-	V
S3/ S4 SEL	-	-	0.8	V

**S Pin**

S3/ S4 Voltage	S3/ S4 OPEN	S3/ S4 SEL
Less 0.8V	0	1
1.3 ~ 3.5	0	0
Up 4.5V	1	0

D Pins				
D-pin detection H	2.5			V
D-pin detection L			1.5	V
Line 1~3 detect level H	3.5	-	-	V
Line 1~3 detect level M	1.4	-	2.4	V
Line 1~3 detect level L	-	-	1.0	V

**D1 Pin**

00/ D2	Pin Description
0	Yes
1	No

**L3 Aspect Ratio**

01/ D5	01/ D4	DC Level	Aspect
0	0	L	4:3
0	1	M	Letter Box
1	0	H	16:9
1	1		Don't Care

**L2 I/p input**

01/ D7	01/ D6	DC Level	I/p input
0	0	L	60i
0	1	M	Don't Care
1	0	H	60p
1	1		Don't Care

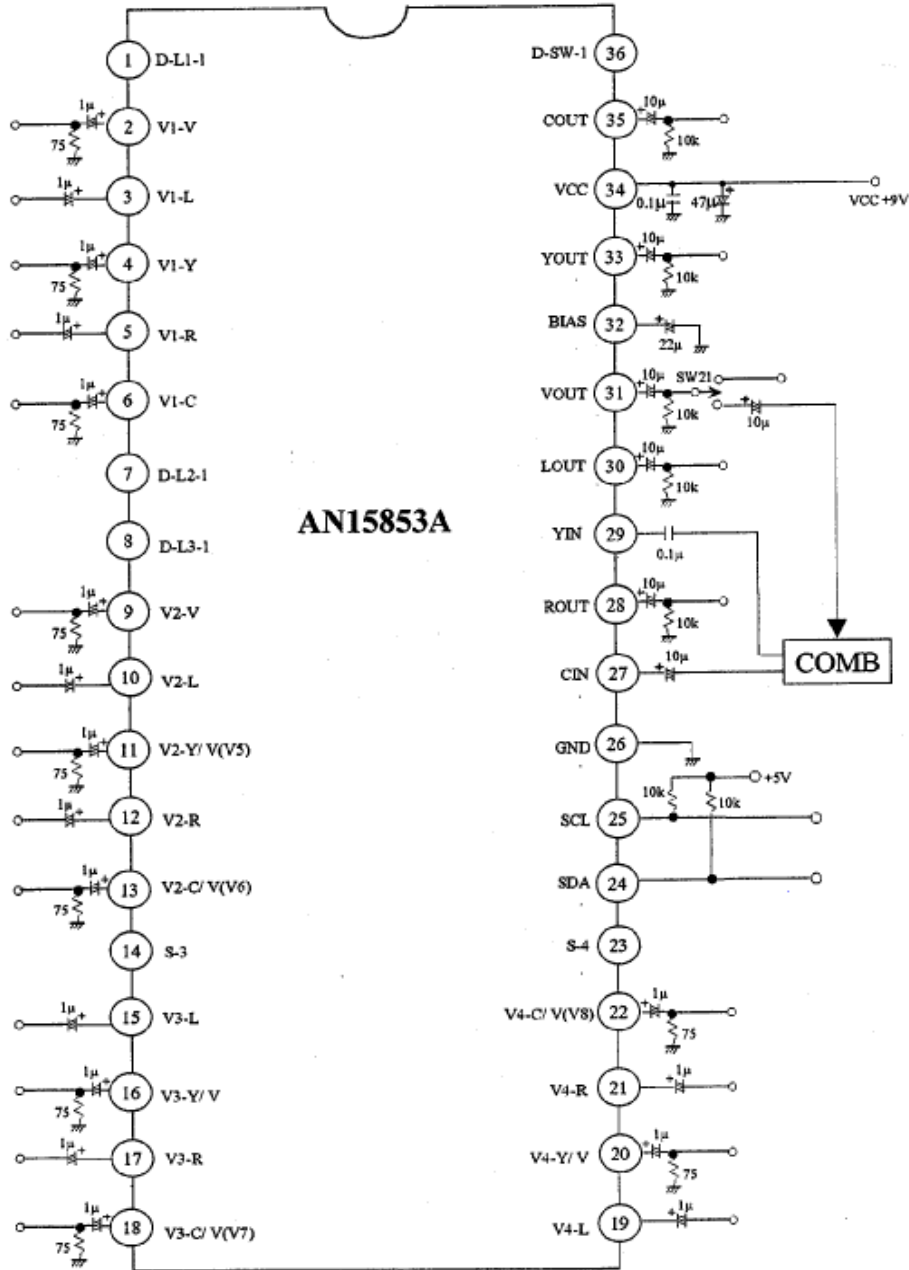
**L1 Scanning Lines**

00/ D1	07/ D0	DC Level	Scanning Lines
0	0	L	480
0	1	M	720
1	0	H	1080
1	1		Don't Care

Eff. Date	Eff. Date	Eff. Date	Eff. Date
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Application Circuit 1



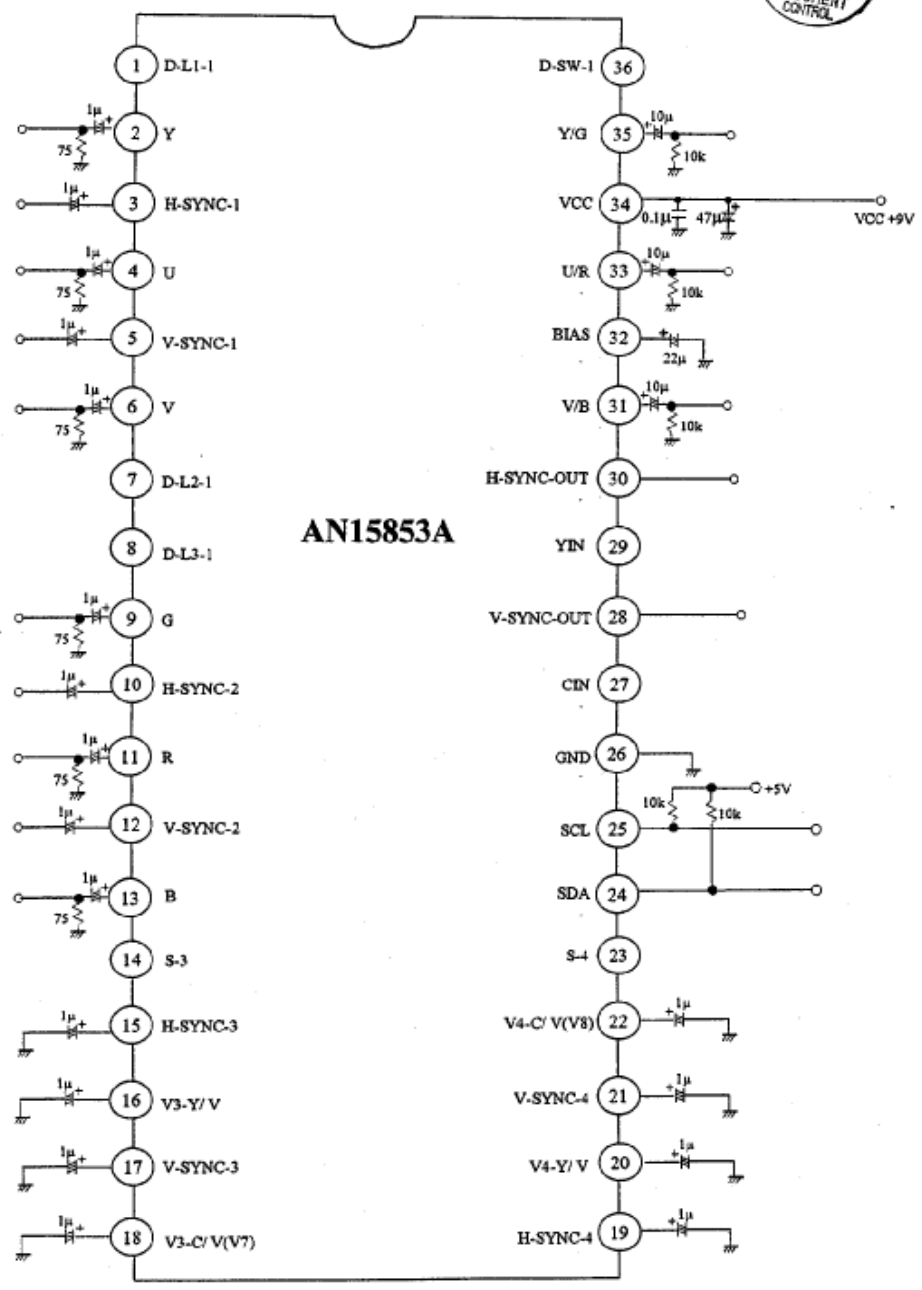
Eff. Date	Eff. Date	Eff. Date	Eff. Date
9 Jan 2003			

APPROVED  
EXTERNAL ISSUE

Doc No. SDSC-PSE-AN15853A REV 1.0

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**Application Circuit 2**  
(For H/V SYNC Input Select)



Eff. Date	Eff. Date	Eff. Date	Eff. Date
9 Jan 2003			

FMSC-PSDA-002-01 Rev.1

Semiconductor Company, Matsushita Electric Industrial Co., Ltd.