



Description

The 89TSF5xx is a complete switch fabric, consisting of two chips:

89TSF552 (queuing engine, 10 Gbps).

89TSF500 (crossbar and scheduler).

The 89TSF5xx switch fabric is a system of one or more queuing engines and one or more crossbar/schedulers. The main function of the 89TSF5xx is to route traffic from the source to the destination in a fair and efficient way. It can be configured in many ways that achieve fairness, balance loads, minimize traffic congestion, and protect against failure. These devices interconnect using sets of high-speed SerDes links. They are scalable, and bandwidth increases linearly when you add multiple 89TSF500s. A functional block diagram of the 89TSF500 is shown in Figure 1.

The 89TSF552 is the interface of a system port (usually equivalent to a line card¹) to the 89TSF5xx switch fabric. The 89TSF500 is the "switch" of the 89TSF5xx switch fabric. Combined, they provide up to 10 Gbps switching bandwidth per system port and up to 32 system ports or 64 system subports² per system.

The 89TSF5xx switch fabric devices interconnect using high speed, serial links. The 89TSF5xx system can be implemented on a single shelf or on multiple shelves. Figure 2 is an example of a single-shelf system, while Figures 3 and 4 illustrate multiple-shelf systems.

The 89TSF5xx switch fabric has a modular and scalable architecture that gives system designers maximum flexibility and performance. This architecture allows a switch to be implemented either on a single shelf using an electrical backplane or on multiple shelves connected by optical transceivers, thus helping system vendors overcome physical space constraints.

The 89TSF500 consists of an integrated crossbar and a scheduler. It has a non-blocking architecture and supports up to 8 classes of service and spatial multicasting. It performs data switching and circuit switching concurrently, providing guaranteed bandwidth and fixed jitter for the circuit paths.

A single 89TSF500 has an aggregate bandwidth of 64 Gbps, full duplex, providing the benefits of high density, low cost, and low power. Multiple 89TSF500s can be combined to support system configurations up to 32 line cards at 10 Gbps, full duplex.

89TSF5xx Features

- ◆ Up to 32 switch ports, with 24 Gbps available per switch port.

¹ A 10 Gbps line card would have a single 89TSF552 and therefore that line card would be equivalent to a system port. However, a 20 Gbps line card would have two 89TSF552s and therefore that line card is equivalent to 2 system ports.

² One 89TSF552 can support up to 4 system subports.

- ◆ Variable length CSIX payload (up to 132 bytes) that supports any type of traffic.
- ◆ Virtual output queues (VOQs) in the ingress direction that eliminate head-of-line blocking. The 256 unicast VOQs provide:
 - A maximum of 32 ports with 8 CoS, or
 - A maximum of 16 ports with 4 subports and 4 CoS.
- ◆ Spatial multicast support with up to 4K global multicast labels. Each multicast label can specify from 1 to 32 ports.
- ◆ Efficient backpressure mechanism that eliminates cell loss caused by congestion.
- ◆ In-service scalable architecture.
- ◆ "Stackable" architecture. Total aggregate bandwidth is linearly proportional to the number of 89TSF500s. Port rate is configurable up to OC-192.
- ◆ Always non-blocking architecture across destination, traffic type (cell, packet), and class of service (CoS).
- ◆ Supports up to 4 egress subports per switch port.
- ◆ Carrier class reliability features:
 - Flexible architecture that allows the 89TSF switch fabric to be employed in a single switch shelf or in multiple switch shelves.
 - Automatic link diagnostics that detect faulty link connections.
 - Both *n+m* (load-sharing mode) and 1:1 protection (active/standby mode) on serial links.
 - Patented error correction scheme to reduce the system bit error rate by 10⁵.
 - Line cord redundancy via Redundant Destination Mapping (RDM) and Queue-Mapped Redundancy (QMR).
 - Dynamic 89TSF500 rerouting that avoids congested or faulty 89TSF500s.
 - Zero cell loss during controlled switchover to standby 89TSF500s.
- ◆ Advanced diagnostic features including multiple loopback paths.
- ◆ Unicast and multicast traffic with up to 8 classes of service.
- ◆ Industry-standard CSIX-over-LVDS interface.
- ◆ Backward compatibility with IDT's ZSF200 switch fabric.

89TSF500 Features

- ◆ 32 embedded SerDes links per device at 2.5 Gbps per link.
- ◆ Linear scalability for higher aggregate port density.
- ◆ Combined unicast and multicast scheduling.
- ◆ Clock synchronization and cell alignment across the fabric.
- ◆ External processor interface for register config. and status.

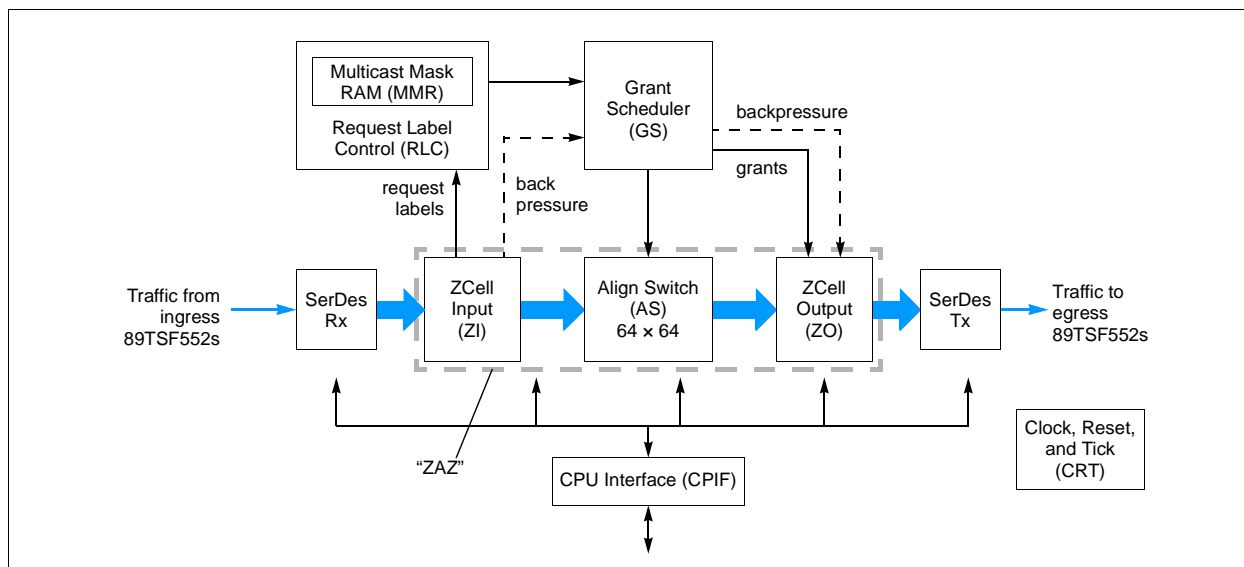


Figure 1 89TSF500 Functional Block Diagram

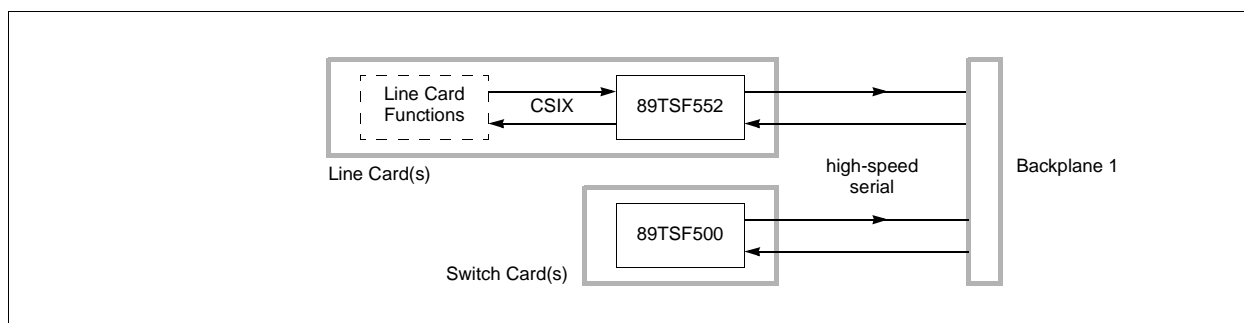


Figure 2 Single-Shelf System

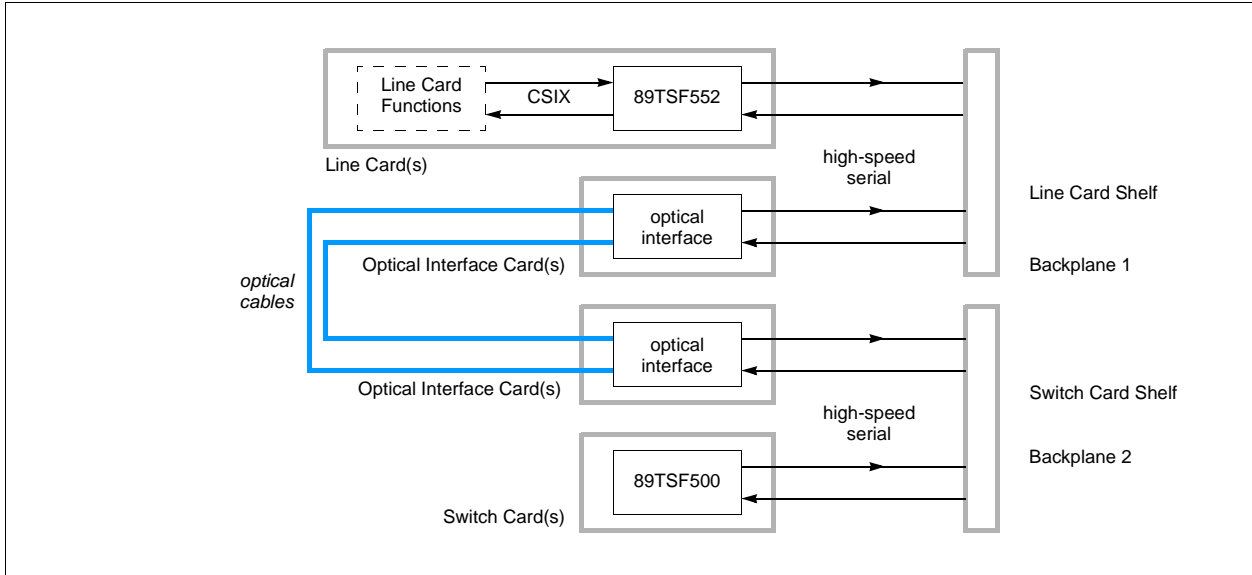


Figure 3 Multiple-Shelf System with Single Switch Shelf

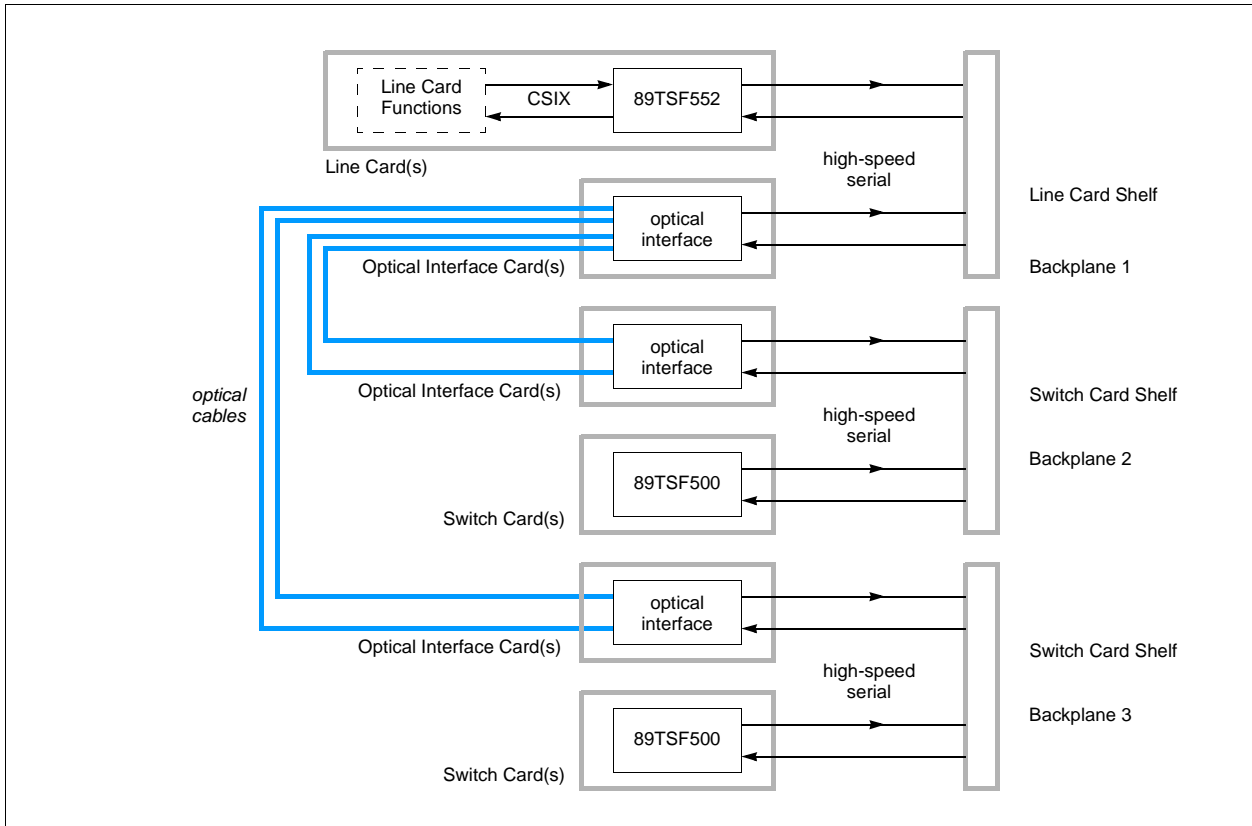


Figure 4 Multiple-Shelf System with Multiple Switch Shelves

89TTSF500 Pin Description

Note: Information in this section is subject to change. Contact your IDT FAE before making design decisions.

In this data sheet, direction is indicated as follows: I for In, O for Out, B for Bidirectional, and P for power.

Signal Name	I/O Type	Dir.	Freq.	Remarks
SYS_CLK (pin AA1)	3.3V LVTTTL	I	125 MHz	N/A
PLL_CORE_LCK (pin AA3)	3.3V LVTTTL	O	—	N/A
PLL_SYS_LCK (pin W3)	3.3V LVTTTL	O	—	N/A
PLL_DIV_RST_N (pin U2)	3.3V LVTTTL	I	—	33K Ω internal pullup
PLL_RST (pin AB3)	3.3V LVTTTL	I	—	33K Ω internal pullup
PLL_CORE_VDDA (pin AB8)	1.8V AVDD	P	—	Supply
PLL_CORE_VSSA (pin AA8)	AVSS	P	—	Supply
PLL_CORE_VDD (pin AB6)	1.8V AVDD	P	—	Supply
PLL_CORE_VSS (pin AA6)	VSS	P	—	Supply
PLL_SYS_VDDA (pin V6)	3.3V AVDD	P	—	Supply
PLL_SYS_VSSA (pin W6)	AVSS	P	—	Supply
PLL_SYS_VDD (pin V8)	1.8V AVDD	P	—	Supply
PLL_SYS_VSS (pin W8)	VSS	P	—	Supply

Table 1 89TSF500 PLL Control and Power Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
SD[2:0]_REFCLKN (pins A24, Y39, AW25)	Serdes diff input	I	250MHz	Reference clocks for both Rx and Tx. The reference clock (SD[n]_REFCLKN and SD[n]_REFCLKP) must be synchronous to twice the system clock (SYS_CLK) input. If an entire SerDes group is not used, the reference clock pins for that group should be pulled down to VSS using a 300 Ω to 1k Ω resistor.
SD[2:0]_REFCLKP (pins A25, AA39, AW24)	Serdes diff input	I	250MHz	
SD[2:0]_REF_RES (pins D25, AA36, AT24)	Serdes Bidi	O	—	Reference resistor pins used to generate bias currents for both Rx and Tx. To ensure proper biasing, connect each of these to VSS through a 3.09 k Ω 1% resistor. If an entire SerDes group is not used, the reference resistor pins for that group should be connected to VDD_SD (1.8V).
VDD_SD[2:0]_PLL (pins J23, Y31, AL23)	VAA18	P	—	SerDes common VDD = 1.8V. These are PLL analog power pins and must be well filtered.
VSS_SD[2:0]_PLL (pins K22, W30, AK24)	VSS	P	—	SerDes PLL ground
VDD_REFCLK[2:0] (pins J24, AA31, AL22)	VAA33	P	—	SerDes common VDD = 3.3V

Table 2 89TSF500 SerDes Pins (Part 1 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
RXN[31:0]	Serdes diff input	I	—	SerDes Rx pairs. Unused pins may be left unconnected.
RXP[31:0]	Serdes diff input	I	—	
TXN[31:0]	Serdes diff input	O	—	SerDes Tx pairs. Unused pins may be left unconnected.
TXP[31:0]	Serdes diff input	O	—	
VDD_SD	VAA18	P	—	SerDes VDD = 1.8V
VDD_TX	VAA25	P	—	SerDes Tx VDD (2.5V)

Table 2 89TSF500 SerDes Pins (Part 2 of 2)

Signal Name	Type	Dir.	Freq.	Remarks
ZBUS_AVALID_N (pin AT5)	3.3V LVTTTL	I	33MHz	33K Ω internal pullup
ZBUS_CLK (pin AV3)	3.3V LVTTTL	I	33MHz	N/A
ZBUS_AD[15:0]	3.3V LVTTTL	B	33MHz	33K Ω internal pullup
ZBUS_DEVID[4:0]	3.3V LVTTTL	I	—	33K Ω internal pullup
ZBUS_DVALID_N (pin AV10)	3.3V LVTTTL	B	33MHz	33K Ω internal pullup
ZBUS_INT_N[2:0] (pins AW11, AU11, AW9)	3.3V LVTTTL	O	—	33K Ω internal pullup
ZBUS_PRTY (pin AV9)	3.3V LVTTTL	B	33MHz	33K Ω internal pullup

Table 3 89TSF500 ZBus Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
TCK (pin A11)	3.3V LVTTTL	I	—	33K internal pullup
TDI (pin A10)	3.3V LVTTTL	I	—	33K internal pullup
TDO (pin B11)	3.3V LVTTTL	O	—	33K internal pullup
TMS (pin C11)	3.3V LVTTTL	I	—	33K internal pullup
TRST_N (pin B10)	3.3V LVTTTL	I	—	33K internal pullup

Table 4 89TSF500 Test and Debugging Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
ZTICK (pin V4)	3.3V LVTTTL	I	—	External reference ZTick input to which the internal ZTick logic will synchronize. If ZTICK_MODE is 0, ZTICK can be left open.
ZTICK_MODE (pin V2)	3.3V LVTTTL	I	—	External ZTick select. 1 = Device uses externally generated ZTicks 0 = Device uses internally generated ZTicks. Pin(s) must be stable at least 16 ns before the deassertion of the RESET_N input. Any change in pin(s) after 16 ns before the deassertion of the RESET_N input must be concurrent with, or followed by, an assertion of the RESET_N input.

Table 5 89TSF500 ZTick Management Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
RESET_N (pin AR3)	3.3V LVTTTL	I	Async	100K internal pullup
CHN_DET_MODE (pin AU2)	3.3V LVTTTL	I	N/A	33K pullup
VDD	VDD18	P	—	1.8V
VDD_IO	VDD33	P	—	3.3V
VSS	VSS	P	—	Ground

Table 6 89TSF500 Misc. Pins

89TSF500 Electrical Specifications

Some data are TBD and will be published as they become available.

The specifications are subject to change without notice.

89TSF500 Absolute Maximum Ratings

The absolute maximum ratings are the maximum conditions that the device can withstand without sustaining permanent damage. Exceeding any of these conditions could result in permanent damage to the device. Normal operation should not be expected at these conditions. In addition, exposure to absolute maximum rated conditions (or near absolute maximum rated conditions) for extended periods may affect device reliability.

Operation of the device is not guaranteed at the absolute maximum ratings, but rather at the operating conditions outlined in Table 8.

Symbol	Parameter	Min	Max	Units	Conditions
T_{JMAX}	Junction temperature under bias	—	105	°C	
$T_{STORAGE}$	Storage temperature	—	150	°C	
	Storage temperature range	-40	85	°C	Long term storage
T_{SOLDER}	Soldering temperature	—	215	°C	
T_{REWORK}	Rework temperature	—	204	°C	

Table 7 89TSF500 Absolute Maximum Ratings (Part 1 of 2)

Symbol	Parameter	Min	Max	Units	Conditions
T_{GP_SOLDER}	Soldering temperature for green package	—	245	°C	
T_{GP_REWORK}	Rework temperature for green package	—	245	°C	
V_{IO}	I/O terminal voltage	-0.6	VDD+0.6	V	longer than 1 ns
		-1.0	VDD+1.0	V	pulse \leq 1 ns

Table 7 89TSF500 Absolute Maximum Ratings (Part 2 of 2)

89TSF500 Operating Ranges

Symbol	Parameter	Min	Typical	Max	Units	Conditions
T_J	Operating junction temperature range	0	—	85	°C	
V_{VDD}	Core digital 1.8V power supply	1.71	1.8	1.89	V	$\pm 5\%$
$V_{PLL_SYS_VDD}$, $V_{PLL_CORE_VDD}$	PLL digital 1.8V power supply	1.71	1.8	1.89	V	$\pm 5\%$
$V_{PLL_SYS_VDDA}$, $V_{PLL_CORE_VDDA}$	PLL analog 3.3V power supply	3.135	3.3	3.465	V	$\pm 5\%$
V_{VDD_IO}	LVTTTL 3.3V I/O 3.3V power supply	3.135	3.3	3.465	V	$\pm 5\%$
V_{VDD_SD}	SerDes Core 1.8V power supply	1.71	1.8	1.89	V	$\pm 5\%$
$V_{VDD_SD_PLL}$	SerDes PLL 1.8V power supply	1.71	1.8	1.89	V	$\pm 5\%$
V_{VDD_TX}	SerDes transmit 2.5V power supply	2.375	2.5	2.625	V	$\pm 5\%$
V_{VDD_REFCLK}	SerDes reference clock 3.3V power supply	3.135	3.3	3.465	V	$\pm 5\%$
—	SerDes power supply voltage noise (all power supplies)	—	—	TBD	mV	Peak-to-peak (50 kHz to 100 MHz)
Power Dissipation		—	17.39	21.06	W	Max. values use the maximum voltages and current listed in this table and typical values use the typical voltages and current.

Table 8 89TSF500 Operating Ranges

89TSF500 DC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 8.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
I_{VDD}	Input current for core digital 1.8V power supply	—	4250	4930	mA	"Typical" here means max. load, nominal voltage
$I_{PLL_SYS_VDD}$ $I_{PLL_CORE_VDD}$	Input current for PLL digital 1.8V power supply	—	1.7	1.9	mA	"Typical" here means max. load, nominal voltage
$I_{PLL_SYS_VDDA}$ $I_{PLL_CORE_VDDA}$	Input current for PLL analog 3.3V power supply	—	0.35	0.4	mA	"Typical" here means max. load, nominal voltage
I_{VDD_IO}	Input current for LVTTTL 3.3V I/O power supply	—	160	187	mA	"Typical" here means max. load, nominal voltage
I_{VDD_SD}	Input current for SerDes core 1.8V power supply	—	3300	3764	mA	"Typical" here means max. load, nominal voltage
$I_{VDD_SD_PLL}$	Input current for SerDes PLL 1.8V power supply	—	210	270	mA	"Typical" here means max. load, nominal voltage
I_{VDD_TX}	Input current for SerDes transmitters 2.5V power supply	—	1150	1317	mA	"Typical" here means max. load, nominal voltage
I_{VDD_REFCLK}	Input current for SerDes reference clock buffer 3.3V power supply	—	3	3	mA	"Typical" here means max. load, nominal voltage
I_{IL33}	Input leakage low current for 3.3V I/O	-5	—	5	μ A	
I_{IH33}	Input leakage high current for 3.3V I/O	-5	—	5	μ A	
I_{IL33PU}	Input leakage low current for 3.3V I/O with internal pullup	-80	—	5	μ A	
I_{IH33PU}	Input leakage high current for 3.3V I/O with internal pullup	-5	—	5	μ A	
I_{IL33PD}	Input leakage low current for 3.3V I/O with internal pulldown	-5	—	5	μ A	
I_{IH33PD}	Input leakage high current for 3.3V I/O with internal pulldown	+5	—	+200	μ A	
V_{IL33}	Input low voltage for 3.3V I/O	-0.3	—	0.8	V	
V_{IH33}	Input high voltage for 3.3V I/O	2.0	—	$V_{DDLVTTL33}+0.5$	V	
V_{OL33}	Output low voltage for 3.3V I/O	—	—	0.4	V	$I = 12$ mA for 12 mA drivers and 16 mA for 16 mA drivers
V_{OH33}	Output high voltage for 3.3V I/O	2.4	—	—	V	$I = -12$ mA for 12 mA drivers and -16 mA for 16 mA drivers

Table 9 89TSF500 DC Characteristics

89TSF500 AC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 8.

Symbol	Parameter	Min	Typical	Max	Units
f_{SYS}	System clock frequency (125 MHz \pm 0.1 MHz)	124.9	125	125.1	MHz
T_{JSYS}	Jitter requirements (peak to peak) for system clock. Peak to peak jitter requirements apply to entire range of allowed system clock frequencies.	—	—	100	ps
D_{SYS}	Percentage duty cycle for system clock	45	50	55	%
T_{RSYSCI}	System clock input rise time (10% to 90%)	—	—	TBD	ns
T_{FSYSCI}	System clock input fall time (90% to 10%)	—	—	TBD	ns

Table 10 89TSF500 System Clock Timing

Symbol	Parameter	Min	Typical	Max	Units
f_{ZB}	ZBus clock frequency	30	$f_{SYS} / 4$	33.1	MHz
D_{ZB}	Percentage duty cycle for ZBus clock	45	50	55	%
T_{RZBCI}	ZBus clock input rise time (10% to 90%)	—	—	TBD	ns
T_{FZBCI}	ZBus clock input fall time (90% to 10%)	—	—	TBD	ns

Table 11 89TSF500 ZBus Clock Timing

Symbol	Parameter	Min	Typical	Max	Units
T_{KQVZB}	ZBus clock rising edge to output valid	—	—	10.0	ns
T_{KOXZB}	ZBus clock rising edge to output invalid	1.0	—		ns
T_{KQLZB}	ZBus clock rising edge to output low Z	1.0	—	10.0	ns
T_{KOHZB}	ZBus clock rising edge to output high Z	1.0	—	10.0	ns
T_{SZB}	Input setup time from ZBus clock rising edge	5.0	—		ns
T_{HZB}	Input hold time from ZBus clock rising edge	1.0	—		ns
T_{RZBI}	Input rise time (10% to 90%)	—	—	TBD	ns
T_{FZBI}	Input fall time (90% to 10%)	—	—	TBD	ns

Table 12 89TSF500 ZBus Interface Timing

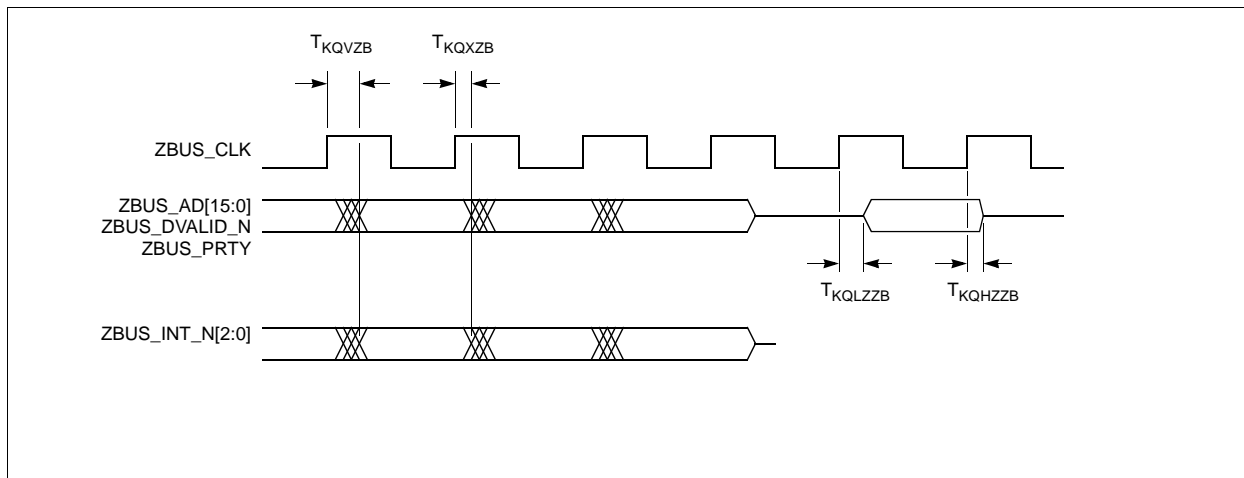


Figure 5 89TSF500 ZBus Interface Output Timing

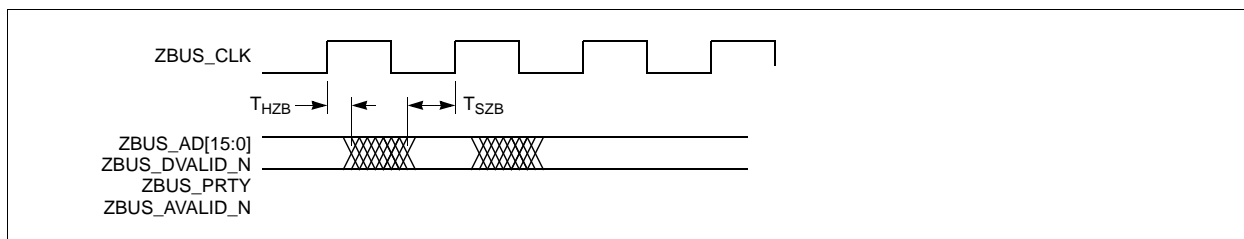


Figure 6 89TSF500 ZBus Interface Input Timing

Symbol	Parameter	Min	Typical	Max	Units
T_{SZT}	Input setup time from system clock (SYS_CLK pin) rising edge	3.0	—	—	ns
T_{HZT}	Input hold time from system clock rising edge	1.0	—	—	ns
T_{RZTI}	Input rise time (10% to 90%)	—	—	TBD	ns
T_{FZTI}	Input fall time (90% to 10%)	—	—	TBD	ns

Table 13 89TSF500 ZTick Interface Timing

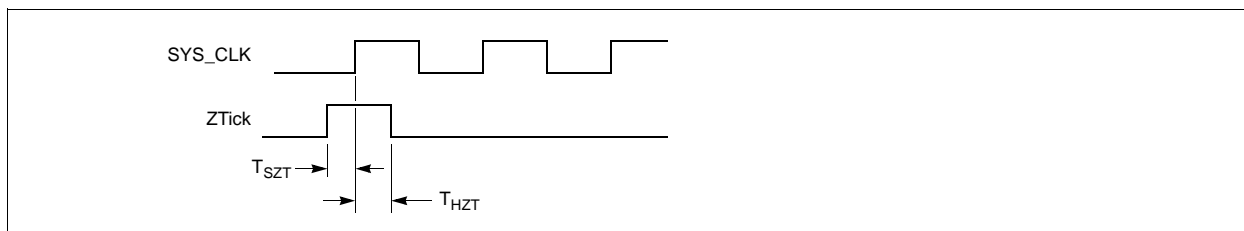


Figure 7 89TSF500 ZTick Interface Input Timing

Symbol	Parameter	Min	Typical	Max	Units	Conditions
	Common mode range	1.5	2	3	V	
V _{PP} (differential)	"Eye" opening	300	400	—	mV	Common mode should be VDD_REFCLK – 1/2 eye opening
f _{SDREF}	SerDes reference clock frequency	2 × f _{SYS}			MHz	The expected frequency is 250 MHz (2 × 125 MHz)
D _{SDREF}	Percentage duty cycle for SerDes reference clock	40	—	60	%	
J _{SDREF}	Random jitter for SerDes reference clock		—	5	ps	RMS
f _{oSDREF}	Frequency offset between source and destination SerDes reference clocks	-100	—	+100	ppm	
T _{RSDREFCI}	SerDes reference clock input rise time (10% to 90%)	—	—	TBD	ns	T _{RZBCI}
T _{FSDREFCI}	SerDes reference clock input fall time (90% to 10%)	—	—	TBD	ns	T _{FZBCI}

Table 14 89TSF500 SerDes Reference Clock Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
J _{DR}	Deterministic Jitter at receiver	—	—	0.41	UI	
J _{TR}	Total jitter at receiver	—	—	0.65	UI	at 10 ⁻¹² BER
Z _{RTERM}	Single-ended termination of differential inputs	45	—	55	Ohm	
LDR	Rx return loss	TBD	—	—	dB	100 MHz to 1.875 GHz
—	Rx common mode return loss	TBD	—	—	dB	100 MHz to 1.875 GHz
V _{RSense}	Input sensitivity	200	—	—	mV	Differential peak-peak
V _{MAX}	Maximum input voltage	—	—	2000	mV	Differential peak-peak
T _{reyc}	"Eye" opening	140	—	—	ps	
I _{roff}	Off current	-50	—	50	mA	Maximum current into a pin with power off

Table 15 89TSF500 SerDes Interface Receiver Characteristics

Symbol	Parameter	Min	Typical ¹	Max	Units	Notes
V _{DIFF1}	Differential output (without pre-emphasis) (amplitude setting 1)	TBD	625	TBD	mV	Refer to Table 17.
V _{DIFF2}	Differential output (without pre-emphasis) (amplitude setting 2)	TBD	1100	TBD	mV	Refer to Table 18.
V _{DIFF3}	Differential output (without pre-emphasis) (amplitude setting 3)	TBD	1200	TBD	mV	Refer to Table 19.
t _{dfr}	Driver rise/fall time	TBD	TBD	TBD	ps	Measured at 20–80%

Table 16 89TSF500 SerDes Interface Transmitter Characteristics (Part 1 of 2)

Symbol	Parameter	Min	Typical ¹	Max	Units	Notes
Z _D	Differential output impedance	—	100	—	Ohm	100 MHz to 1.875 GHz
Z _{SE}	Single-ended output impedance	—	50	—	Ohm	100 MHz to 1.875 GHz
Z _{MSE}	Single-ended output impedance matching	3	—	8	%	100 MHz to 1.875 GHz
J _D	Deterministic jitter	—	—	0.15	UI	Without pre-emphasis
J _T	Total jitter	—	—	0.21	UI	At ±7 sigma

Table 16 89TSF500 SerDes Interface Transmitter Characteristics (Part 2 of 2)

¹: The typical amplitude values are obtained when V_{DD_TX}=2.5V, and V_{DD_SD}=1.8V

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.31	15.5%
2	0.46	23%
3	0.77	38.5%
4	0.61	30.5%
5	0.90	45%
6	1.04	52%
7	1.25	62.5%

Table 17 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 1 (625mV typical)

¹: Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

²: Amount "a" in Figure 8.

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.17	8.5%
2	0.26	13%
3	0.44	22%
4	0.34	17%
5	0.52	26%
6	0.59	29.5%
7	0.72	36%

Table 18 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 2 (1100mV typical)

¹: Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

²: Amount "a" in Figure 8.

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.16	8.0%
2	0.23	11.5%
3	0.39	19.5%
4	0.31	15.5%
5	0.46	23%
6	0.53	26.5%
7	0.64	32%

Table 19 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 3 (1200mV typical)

¹ Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

² Amount "a" in Figure 8.

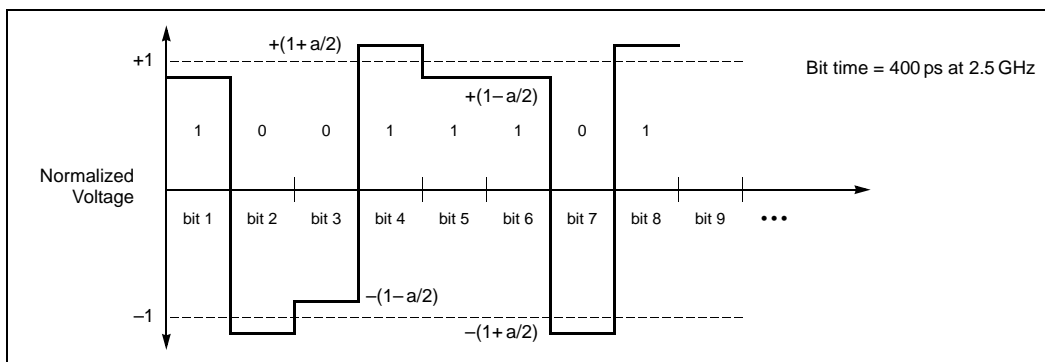


Figure 8 Output with Pre-Emphasis

89TSF500 AC Test Conditions

Input Rise/Fall Time	1 V / ns (20% / 80%)
Output timing measurement reference level (V_{REF}) for 3.3V interfaces.	1.65V
Output load	As shown in Figure 9

Table 20 89TSF500 AC Test Conditions

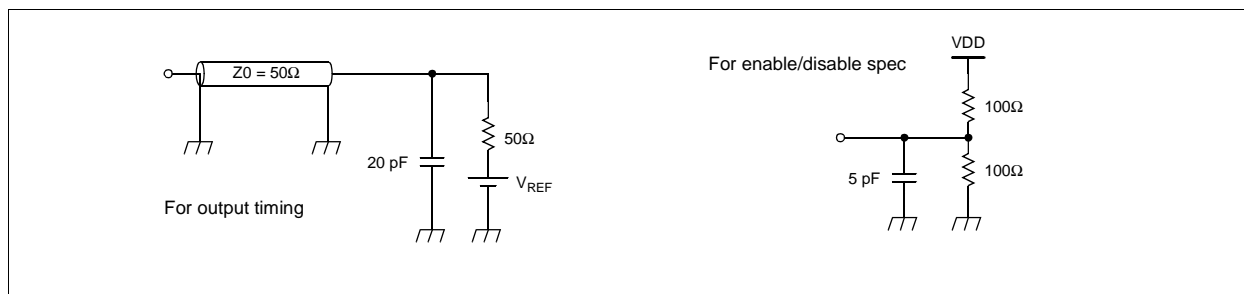


Figure 9 89TSF500 AC Test Load

89TSF500 Thermal Considerations

This section describes the temperature and heat sink calculations for flip-chip BGA devices.

Symbol	Parameter	Value	Units	Conditions
θ_{JA}	Thermal resistance, junction to ambient (no heat sink)	9.0	°C / W	Still air
		5.5	°C / W	200 FPM
		4.5	°C / W	500 FPM
θ_{JB}	Estimated thermal resistance, junction to board	2.2	°C / W	
θ_{JC}	Thermal resistance, junction to case	0.19	°C / W	

Table 21 89TSF500 Thermal Characteristics

The thermal circuit is as shown below.

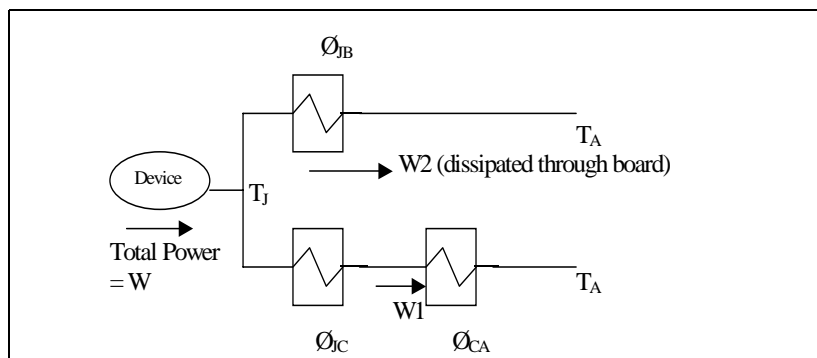


Figure 10 89TSF500 Thermal Circuit

For flip-chip BGA devices, there are two paths for heat dissipation: one through the package balls to the board and other through the package case to air. The device specifications provide θ_{JB} and θ_{JC} numbers. The θ_{CA} number comes from the heat sink manufacturer and depends on type of heat sink (area, height, fin type, etc.) and the airflow across the heat sink. The device specifications also provide the maximum operating junction temperature (T_J) that will not degrade the device reliability. The system designer should ensure that the device maximum junction temperature is not exceeded under any operating condition. One method of accomplishing this is to calculate the maximum ambient temperature (T_A) that can be tolerated based on the above device parameters. The formula is shown below.

$$T_A = T_J - W \times \frac{\theta_{JB} \times (\theta_{JC} + \theta_{CA})}{\theta_{JB} + \theta_{JC} + \theta_{CA}}$$

The following graph depicts the ambient temperature (T_A) versus θ_{CA} .

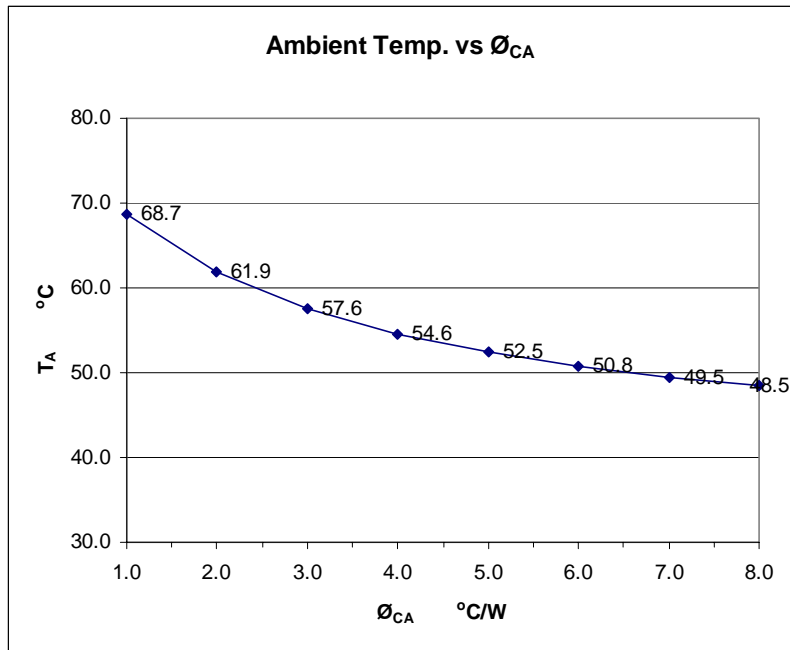


Figure 11 89TSF500 Ambient Temperature Curve

For system designers, specification of the maximum device junction temperature (operating) is critical, since it allows them to select a heat sink that meets the maximum ambient temperature requirements of their system.

The other parameter that is device package-specific is θ_{JA} , without a heat sink, and is specified for various air-flow conditions. This is the intrinsic thermal resistance of the package (junction to case + case to ambient) and is mainly specified as a reference parameter. (This is when a heat sink is not present and the top surface of the package is essentially acting as the heat sink). However, in devices that have high power dissipation, heat sink usage is highly desirable. Consequently, system designers may have limited use for this parameter.

89TSF500 Power, Reset, and Initialization Sequencing Requirements

Power Supply Power-Up Sequence

There is a power supply power-up sequence requirement that addresses potential latchup issues with some I/O buffers. All 3.3V I/O power must ramp up before all other power supply pins:

- 3.3V I/O (VDD_{IO} , $VDDP33$, $VDD_{REFCLKn}$)
- All other power supply pins

Further, IDT recommends that the designer use current limiting resistors on the bidirectional ZBus pins to limit potential high transient current from short-circuit current or bus contention during the power-up period. Such events can occur because of an unknown state of output enable of the bidirectional buffers. After core power ramps up (with RESET_N asserted), the bidirectional I/O lines enter normal operating mode.

Power Supply Power-Down Sequence

Because the power supply power-off state clears any latchup condition, the power-down sequence is not dictated by latchup. However, potential high transient current from short-circuit current or bus contention can also occur during the power-down period. We recommend appropriate sequencing. All 3.3V I/O power should ramp down before the 1.8V core (VDD) power:

- 3.3V I/O (VDD_{IO})
- 1.8V core (VDD)

However, if appropriate current limiting techniques (e.g., series resistors) are employed and the 2.5V and 1.5V power supplies ramp down soon after the 1.8V core power supply (within about 50 ms), the system designer can safely ignore this recommendation.

PLL Power-Up Initialization

PLL inputs into the 89TSF500, from an external device such as the ZBus bridge in IDT's reference system, require a special initialization sequence. Figure 12 shows the initialization sequence.

PLL initialization is necessary only at power-up. If the PLLs fail to lock, repeatedly assert PLL_RST until they do.

Note: The 89TSF500 must be reset *after* PLL initialization. Hold RESET_N low for at least 16 clocks (SYS_CLK) after PLL initialization completes.

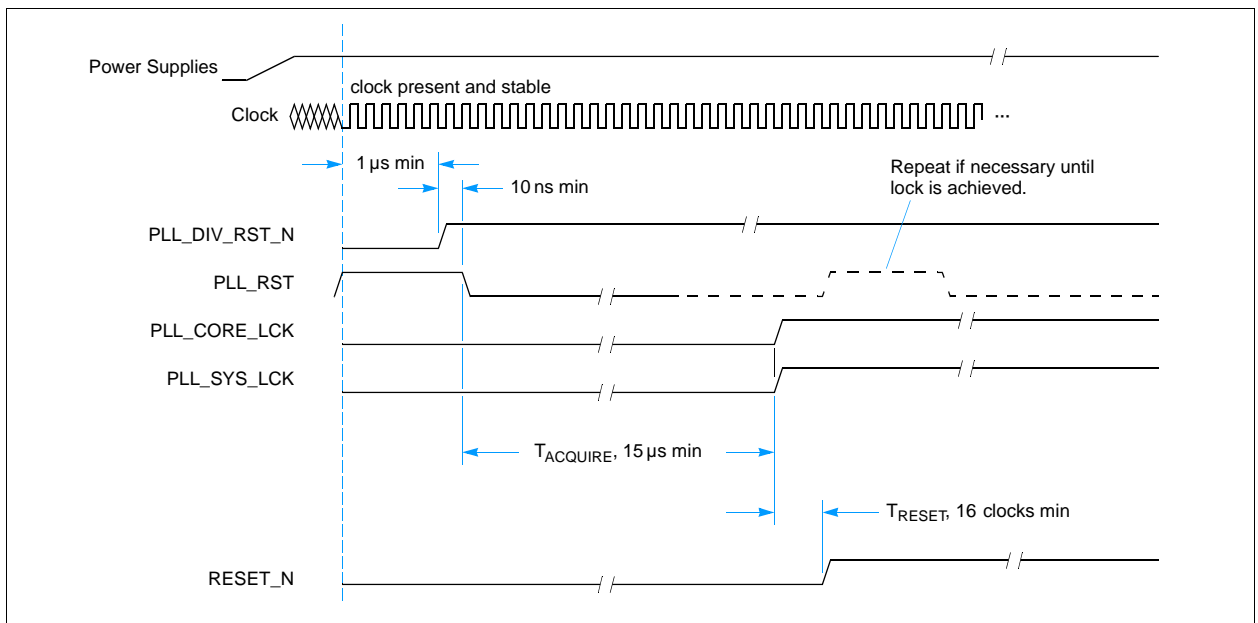


Figure 12 PLL Power-Up Initialization for the 89TSF500

Device Reset

It is possible to reset the entire 89TSF500 except for the PLL. To reset the device without being required to re-initialize the PLL, assert the RESET_N pin (low) for at least 16 clocks (SYS_CLK) and then deassert it.

Pin List I/O Description

The 89TSF500 Pin List on page 18 uses the following I/O notations:

I	Input
O	Output
B	Bidirectional
P	Power
DNC	Do not connect
RPD	Reserved, pulldwn. Pin must be connected to VSS through a 300 - 1K Ω resistor.
RPU	Reserved, pullup. Pin is connected to VDD_IO (3.3V) through a 1K - 10K Ω resistor.

89TSF500 Pin List

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
A2	DNC	DNC	do not connect	B6	DNC	DNC	do not connect
A3	DNC	DNC	do not connect	B7	DNC	DNC	do not connect
A4	VDD_IO	P	VDD33	B8	DNC	DNC	do not connect
A5	DNC	DNC	do not connect	B9	RPD	I	RPD
A6	VSS	P	VSS	B10	TRST_N	I	3.3V LVTTTL
A7	DNC	DNC	do not connect	B11	TDO	I	3.3V LVTTTL
A8	VDD_IO	P	VDD33	B12	VSS	P	VSS
A9	DNC	DNC	do not connect	B13	DNC	DNC	do not connect
A10	TDI	I	3.3V LVTTTL	B14	VSS	P	VSS
A11	TCK	I	3.3V LVTTTL	B15	VSS	P	VSS
A12	VSS	P	VSS	B16	VSS	P	VSS
A13	DNC	DNC	do not connect	B17	VSS	P	VSS
A14	VSS	P	VSS	B18	VSS	P	VSS
A15	RXN[31]	I	Serdes diff input	B19	VSS	P	VSS
A16	RXP[31]	I	Serdes diff input	B20	VSS	P	VSS
A17	RXN[30]	I	Serdes diff input	B21	VSS	P	VSS
A18	RXP[30]	I	Serdes diff input	B22	VSS	P	VSS
A19	RXN[29]	I	Serdes diff input	B23	VSS	P	VSS
A20	RXP[29]	I	Serdes diff input	B24	VSS	P	VSS
A21	RXN[28]	I	Serdes diff input	B25	VSS	P	VSS
A22	RXP[28]	I	Serdes diff input	B26	VSS	P	VSS
A23	VSS	P	VSS	B27	VSS	P	VSS
A24	SD2_REFCLKN	I	Serdes diff clock	B28	VSS	P	VSS
A25	SD2_REFCLKP	I	Serdes diff clock	B29	VSS	P	VSS
A26	VSS	P	VSS	B30	VSS	P	VSS
A27	RXN[27]	I	Serdes diff input	B31	VSS	P	VSS
A28	RXP[27]	I	Serdes diff input	B32	VSS	P	VSS
A29	RXN[26]	I	Serdes diff input	B33	VSS	P	VSS
A30	RXP[26]	I	Serdes diff input	B34	VSS	P	VSS
A31	RXN[25]	I	Serdes diff input	B35	VSS	P	VSS
A32	RXP[25]	I	Serdes diff input	B36	VSS	P	VSS
A33	RXN[24]	I	Serdes diff input	B37	VSS	P	VSS
A34	RXP[24]	I	Serdes diff input	B38	VSS	P	VSS
A35	VSS	P	VSS	B39	VSS	P	VSS
A36	VSS	P	VSS	C1	VSS	P	VSS
A37	VSS	P	VSS	C2	DNC	DNC	do not connect
A38	VSS	P	VSS	C3	DNC	DNC	do not connect
B1	VDD_IO	P	VDD33	C4	DNC	DNC	do not connect
B2	DNC	DNC	do not connect	C5	DNC	DNC	do not connect
B3	DNC	DNC	do not connect	C6	DNC	DNC	do not connect
B4	DNC	DNC	do not connect	C7	DNC	DNC	do not connect
B5	DNC	DNC	do not connect	C8	DNC	DNC	do not connect
				C9	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
C10	RPU	I	RPU	D14	VSS	P	VSS
C11	TMS	I	3.3V LVTTTL	D15	VSS	P	VSS
C12	VSS	P	VSS	D16	VSS	P	VSS
C13	DNC	DNC	do not connect	D17	VSS	P	VSS
C14	VSS	P	VSS	D18	VSS	P	VSS
C15	TXN[31]	O	Serdes diff output	D19	VSS	P	VSS
C16	TXP[31]	O	Serdes diff output	D20	VSS	P	VSS
C17	TXN[30]	O	Serdes diff output	D21	VSS	P	VSS
C18	TXP[30]	O	Serdes diff output	D22	VSS	P	VSS
C19	TXN[29]	O	Serdes diff output	D23	VSS	P	VSS
C20	TXP[29]	O	Serdes diff output	D24	DNC	DNC	do not connect
C21	TXN[28]	O	Serdes diff output	D25	SD2_REF_RES	B	Serdes Bidi
C22	TXP[28]	O	Serdes diff output	D26	VSS	P	VSS
C23	VSS	P	VSS	D27	VSS	P	VSS
C24	DNC	DNC	do not connect	D28	VSS	P	VSS
C25	RPD	I	RPD	D29	VSS	P	VSS
C26	VSS	P	VSS	D30	VSS	P	VSS
C27	TXN[27]	O	Serdes diff output	D31	VSS	P	VSS
C28	TXP[27]	O	Serdes diff output	D32	VSS	P	VSS
C29	TXN[26]	O	Serdes diff output	D33	VSS	P	VSS
C30	TXP[26]	O	Serdes diff output	D34	VSS	P	VSS
C31	TXN[25]	O	Serdes diff output	D35	VSS	P	VSS
C32	TXP[25]	O	Serdes diff output	D36	VSS	P	VSS
C33	TXN[24]	O	Serdes diff output	D37	TXP[23]	O	Serdes diff output
C34	TXP[24]	O	Serdes diff output	D38	VSS	P	VSS
C35	VSS	P	VSS	D39	RXP[23]	I	Serdes diff input
C36	VSS	P	VSS	E1	DNC	DNC	do not connect
C37	TXN[23]	O	Serdes diff output	E2	DNC	DNC	do not connect
C38	VSS	P	VSS	E3	DNC	DNC	do not connect
C39	RXN[23]	I	Serdes diff input	E4	DNC	DNC	do not connect
D1	DNC	DNC	do not connect	E5	DNC	DNC	do not connect
D2	DNC	DNC	do not connect	E6	DNC	DNC	do not connect
D3	DNC	DNC	do not connect	E7	DNC	DNC	do not connect
D4	VSS	P	VSS	E8	DNC	DNC	do not connect
D5	DNC	DNC	do not connect	E9	DNC	DNC	do not connect
D6	VDD_IO	P	VDD33	E10	DNC	DNC	do not connect
D7	DNC	DNC	do not connect	E11	DNC	DNC	do not connect
D8	VSS	P	VSS	E12	DNC	DNC	do not connect
D9	DNC	DNC	do not connect	E13	DNC	DNC	do not connect
D10	RPU	I	RPU	E14	DNC	DNC	do not connect
D11	RPU	I	RPU	E15	DNC	DNC	do not connect
D12	VSS	P	VSS	E16	DNC	DNC	do not connect
D13	DNC	DNC	do not connect	E17	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
E18	DNC	DNC	do not connect	F22	DNC	DNC	do not connect
E19	DNC	DNC	do not connect	F23	DNC	DNC	do not connect
E20	DNC	DNC	do not connect	F24	DNC	DNC	do not connect
E21	DNC	DNC	do not connect	F25	VSS	P	VSS
E22	DNC	DNC	do not connect	F26	DNC	DNC	do not connect
E23	DNC	DNC	do not connect	F27	DNC	DNC	do not connect
E24	DNC	DNC	do not connect	F28	DNC	DNC	do not connect
E25	VSS	P	VSS	F29	DNC	DNC	do not connect
E26	DNC	DNC	do not connect	F30	DNC	DNC	do not connect
E27	DNC	DNC	do not connect	F31	DNC	DNC	do not connect
E28	DNC	DNC	do not connect	F32	DNC	DNC	do not connect
E29	DNC	DNC	do not connect	F33	DNC	DNC	do not connect
E30	DNC	DNC	do not connect	F34	DNC	DNC	do not connect
E31	DNC	DNC	do not connect	F35	DNC	DNC	do not connect
E32	DNC	DNC	do not connect	F36	VSS	P	VSS
E33	DNC	DNC	do not connect	F37	TXP[22]	O	Serdes diff output
E34	DNC	DNC	do not connect	F38	VSS	P	VSS
E35	DNC	DNC	do not connect	F39	RXP[22]	I	Serdes diff input
E36	VSS	P	VSS	G1	DNC	DNC	do not connect
E37	TXN[22]	O	Serdes diff output	G2	DNC	DNC	do not connect
E38	VSS	P	VSS	G3	DNC	DNC	do not connect
E39	RXN[22]	I	Serdes diff input	G4	DNC	DNC	do not connect
F1	VSS	P	VSS	G5	DNC	DNC	do not connect
F2	DNC	DNC	do not connect	G6	DNC	DNC	do not connect
F3	DNC	DNC	do not connect	G7	DNC	DNC	do not connect
F4	VDD_IO	P	VDD33	G8	DNC	DNC	do not connect
F5	DNC	DNC	do not connect	G9	DNC	DNC	do not connect
F6	DNC	DNC	do not connect	G10	DNC	DNC	do not connect
F7	DNC	DNC	do not connect	G11	DNC	DNC	do not connect
F8	DNC	DNC	do not connect	G12	DNC	DNC	do not connect
F9	DNC	DNC	do not connect	G13	DNC	DNC	do not connect
F10	DNC	DNC	do not connect	G14	DNC	DNC	do not connect
F11	DNC	DNC	do not connect	G15	DNC	DNC	do not connect
F12	DNC	DNC	do not connect	G16	DNC	DNC	do not connect
F13	DNC	DNC	do not connect	G17	DNC	DNC	do not connect
F14	DNC	DNC	do not connect	G18	DNC	DNC	do not connect
F15	DNC	DNC	do not connect	G19	DNC	DNC	do not connect
F16	DNC	DNC	do not connect	G20	DNC	DNC	do not connect
F17	DNC	DNC	do not connect	G21	DNC	DNC	do not connect
F18	DNC	DNC	do not connect	G22	DNC	DNC	do not connect
F19	DNC	DNC	do not connect	G23	DNC	DNC	do not connect
F20	DNC	DNC	do not connect	G24	DNC	DNC	do not connect
F21	DNC	DNC	do not connect	G25	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
G26	DNC	DNC	do not connect	H30	DNC	DNC	do not connect
G27	DNC	DNC	do not connect	H31	DNC	DNC	do not connect
G28	DNC	DNC	do not connect	H32	DNC	DNC	do not connect
G29	DNC	DNC	do not connect	H33	DNC	DNC	do not connect
G30	DNC	DNC	do not connect	H34	DNC	DNC	do not connect
G31	DNC	DNC	do not connect	H35	DNC	DNC	do not connect
G32	DNC	DNC	do not connect	H36	VSS	P	VSS
G33	DNC	DNC	do not connect	H37	TXP[21]	O	Serdes diff output
G34	DNC	DNC	do not connect	H38	VSS	P	VSS
G35	DNC	DNC	do not connect	H39	RXP[21]	I	Serdes diff input
G36	VSS	P	VSS	J1	DNC	DNC	do not connect
G37	TXN[21]	O	Serdes diff output	J2	DNC	DNC	do not connect
G38	VSS	P	VSS	J3	DNC	DNC	do not connect
G39	RXN[21]	I	Serdes diff input	J4	DNC	DNC	do not connect
H1	VDD_IO	P	VDD33	J5	DNC	DNC	do not connect
H2	DNC	DNC	do not connect	J6	DNC	DNC	do not connect
H3	DNC	DNC	do not connect	J7	DNC	DNC	do not connect
H4	VSS	P	VSS	J8	DNC	DNC	do not connect
H5	DNC	DNC	do not connect	J9	DNC	DNC	do not connect
H6	DNC	DNC	do not connect	J10	DNC	DNC	do not connect
H7	DNC	DNC	do not connect	J11	DNC	DNC	do not connect
H8	DNC	DNC	do not connect	J12	DNC	DNC	do not connect
H9	DNC	DNC	do not connect	J13	DNC	DNC	do not connect
H10	DNC	DNC	do not connect	J14	DNC	DNC	do not connect
H11	DNC	DNC	do not connect	J15	DNC	DNC	do not connect
H12	DNC	DNC	do not connect	J16	DNC	DNC	do not connect
H13	DNC	DNC	do not connect	J17	DNC	DNC	do not connect
H14	DNC	DNC	do not connect	J18	DNC	DNC	do not connect
H15	DNC	DNC	do not connect	J19	DNC	DNC	do not connect
H16	DNC	DNC	do not connect	J20	DNC	DNC	do not connect
H17	DNC	DNC	do not connect	J21	DNC	DNC	do not connect
H18	DNC	DNC	do not connect	J22	DNC	DNC	do not connect
H19	DNC	DNC	do not connect	J23	VDD_SD2_PLL	P	VAA18
H20	DNC	DNC	do not connect	J24	VDD_REFCLK2	P	VAA33
H21	DNC	DNC	do not connect	J25	DNC	DNC	do not connect
H22	DNC	DNC	do not connect	J26	DNC	DNC	do not connect
H23	DNC	DNC	do not connect	J27	VSS	P	VSS
H24	DNC	DNC	do not connect	J28	DNC	DNC	do not connect
H25	DNC	DNC	do not connect	J29	DNC	DNC	do not connect
H26	DNC	DNC	do not connect	J30	DNC	DNC	do not connect
H27	DNC	DNC	do not connect	J31	DNC	DNC	do not connect
H28	DNC	DNC	do not connect	J32	DNC	DNC	do not connect
H29	DNC	DNC	do not connect	J33	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
J34	DNC	DNC	do not connect	K38	VSS	P	VSS
J35	DNC	DNC	do not connect	K39	RXP[20]	I	Serdes diff input
J36	VSS	P	VSS	L1	DNC	DNC	do not connect
J37	TXN[20]	O	Serdes diff output	L2	DNC	DNC	do not connect
J38	VSS	P	VSS	L3	DNC	DNC	do not connect
J39	RXN[20]	I	Serdes diff input	L4	DNC	DNC	do not connect
K1	VSS	P	VSS	L5	DNC	DNC	do not connect
K2	DNC	DNC	do not connect	L6	DNC	DNC	do not connect
K3	DNC	DNC	do not connect	L7	DNC	DNC	do not connect
K4	VDD_IO	P	VDD33	L8	DNC	DNC	do not connect
K5	DNC	DNC	do not connect	L9	DNC	DNC	do not connect
K6	DNC	DNC	do not connect	L10	VSS	P	VSS
K7	DNC	DNC	do not connect	L11	VSS	P	VSS
K8	DNC	DNC	do not connect	L12	VSS	P	VSS
K9	DNC	DNC	do not connect	L13	VSS	P	VSS
K10	VSS	P	VSS	L14	VSS	P	VSS
K11	VSS	P	VSS	L15	VSS	P	VSS
K12	VSS	P	VSS	L16	VSS	P	VSS
K13	VSS	P	VSS	L17	VSS	P	VSS
K14	VSS	P	VSS	L18	DNC	DNC	do not connect
K15	VSS	P	VSS	L19	VSS	P	VSS
K16	VSS	P	VSS	L20	VSS	P	VSS
K17	VSS	P	VSS	L21	VSS	P	VSS
K18	DNC	DNC	do not connect	L22	VSS	P	VSS
K19	VSS	P	VSS	L23	VSS	P	VSS
K20	VSS	P	VSS	L24	VSS	P	VSS
K21	VSS	P	VSS	L25	VSS	P	VSS
K22	VSS_SD2_PLL	P	VSS	L26	VSS	P	VSS
K23	VSS	P	VSS	L27	VSS	P	VSS
K24	VSS	P	VSS	L28	VSS	P	VSS
K25	VSS	P	VSS	L29	VSS	P	VSS
K26	VSS	P	VSS	L30	VSS	P	VSS
K27	VSS	P	VSS	L31	DNC	DNC	do not connect
K28	VSS	P	VSS	L32	DNC	DNC	do not connect
K29	VSS	P	VSS	L33	DNC	DNC	do not connect
K30	VSS	P	VSS	L34	DNC	DNC	do not connect
K31	DNC	DNC	do not connect	L35	DNC	DNC	do not connect
K32	DNC	DNC	do not connect	L36	VSS	P	VSS
K33	DNC	DNC	do not connect	L37	TXN[19]	O	Serdes diff output
K34	DNC	DNC	do not connect	L38	VSS	P	VSS
K35	DNC	DNC	do not connect	L39	RXN[19]	I	Serdes diff input
K36	VSS	P	VSS	M1	VDD_IO	P	VDD33
K37	TXP[20]	O	Serdes diff output	M2	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
M3	DNC	DNC	do not connect	N7	DNC	DNC	do not connect
M4	VSS	P	VSS	N8	DNC	DNC	do not connect
M5	DNC	DNC	do not connect	N9	DNC	DNC	do not connect
M6	DNC	DNC	do not connect	N10	VSS	P	VSS
M7	DNC	DNC	do not connect	N11	VSS	P	VSS
M8	DNC	DNC	do not connect	N12	VDD_IO	P	VDD33
M9	DNC	DNC	do not connect	N13	VDD	P	VDD18
M10	VSS	P	VSS	N14	VDD	P	VDD18
M11	VSS	P	VSS	N15	VDD	P	VDD18
M12	VDD_IO	P	VDD33	N16	VDD	P	VDD18
M13	VDD_IO	P	VDD33	N17	VDD	P	VDD18
M14	VDD_IO	P	VDD33	N18	DNC	DNC	do not connect
M15	VDD_IO	P	VDD33	N19	VDD_SD	P	VAA18
M16	VDD_IO	P	VDD33	N20	VDD_SD	P	VAA18
M17	VDD_IO	P	VDD33	N21	VDD_SD	P	VAA18
M18	DNC	DNC	do not connect	N22	VDD_SD	P	VAA18
M19	VDD_TX	P	VAA25	N23	VDD_SD	P	VAA18
M20	VDD_TX	P	VAA25	N24	VDD_SD	P	VAA18
M21	VDD_TX	P	VAA25	N25	VDD_SD	P	VAA18
M22	VDD_TX	P	VAA25	N26	VDD_SD	P	VAA18
M23	VDD_TX	P	VAA25	N27	VDD_SD	P	VAA18
M24	VDD_TX	P	VAA25	N28	VDD_TX	P	VAA25
M25	VDD_TX	P	VAA25	N29	VSS	P	VSS
M26	VDD_TX	P	VAA25	N30	VSS	P	VSS
M27	VDD_TX	P	VAA25	N31	DNC	DNC	do not connect
M28	VDD_TX	P	VAA25	N32	DNC	DNC	do not connect
M29	VSS	P	VSS	N33	DNC	DNC	do not connect
M30	VSS	P	VSS	N34	DNC	DNC	do not connect
M31	DNC	DNC	do not connect	N35	DNC	DNC	do not connect
M32	DNC	DNC	do not connect	N36	VSS	P	VSS
M33	DNC	DNC	do not connect	N37	TXN[18]	O	Serdes diff output
M34	DNC	DNC	do not connect	N38	VSS	P	VSS
M35	DNC	DNC	do not connect	N39	RXN[18]	I	Serdes diff input
M36	VSS	P	VSS	P1	VSS	P	VSS
M37	TXP[19]	O	Serdes diff output	P2	DNC	DNC	do not connect
M38	VSS	P	VSS	P3	DNC	DNC	do not connect
M39	RXP[19]	I	Serdes diff input	P4	VDD_IO	P	VDD33
N1	DNC	DNC	do not connect	P5	RPD	I	RPD
N2	DNC	DNC	do not connect	P6	DNC	DNC	do not connect
N3	DNC	DNC	do not connect	P7	DNC	DNC	do not connect
N4	DNC	DNC	do not connect	P8	DNC	DNC	do not connect
N5	DNC	DNC	do not connect	P9	DNC	DNC	do not connect
N6	DNC	DNC	do not connect	P10	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
P11	VSS	P	VSS	R15	VSS	P	VSS
P12	VDD_IO	P	VDD33	R16	VSS	P	VSS
P13	VDD	P	VDD18	R17	VSS	P	VSS
P14	VSS	P	VSS	R18	VSS	P	VSS
P15	VSS	P	VSS	R19	VSS	P	VSS
P16	VSS	P	VSS	R20	VSS	P	VSS
P17	VSS	P	VSS	R21	VSS	P	VSS
P18	VSS	P	VSS	R22	VSS	P	VSS
P19	VSS	P	VSS	R23	VSS	P	VSS
P20	VSS	P	VSS	R24	VSS	P	VSS
P21	VSS	P	VSS	R25	VSS	P	VSS
P22	VSS	P	VSS	R26	VSS	P	VSS
P23	VSS	P	VSS	R27	VDD_SD	P	VAA18
P24	VSS	P	VSS	R28	VDD_TX	P	VAA25
P25	VSS	P	VSS	R29	VSS	P	VSS
P26	VSS	P	VSS	R30	VSS	P	VSS
P27	VDD_SD	P	VAA18	R31	DNC	DNC	do not connect
P28	VDD_TX	P	VAA25	R32	DNC	DNC	do not connect
P29	VSS	P	VSS	R33	DNC	DNC	do not connect
P30	VSS	P	VSS	R34	DNC	DNC	do not connect
P31	DNC	DNC	do not connect	R35	DNC	DNC	do not connect
P32	DNC	DNC	do not connect	R36	VSS	P	VSS
P33	DNC	DNC	do not connect	R37	TXN[17]	O	Serdes diff output
P34	DNC	DNC	do not connect	R38	VSS	P	VSS
P35	DNC	DNC	do not connect	R39	RXN[17]	I	Serdes diff input
P36	VSS	P	VSS	T1	VDD_IO	P	VDD33
P37	TXP[18]	O	Serdes diff output	T2	DNC	DNC	do not connect
P38	VSS	P	VSS	T3	DNC	DNC	do not connect
P39	RXP[18]	I	Serdes diff input	T4	VSS	P	VSS
R1	DNC	DNC	do not connect	T5	DNC	DNC	do not connect
R2	DNC	DNC	do not connect	T6	DNC	DNC	do not connect
R3	DNC	DNC	do not connect	T7	DNC	DNC	do not connect
R4	DNC	DNC	do not connect	T8	DNC	DNC	do not connect
R5	DNC	DNC	do not connect	T9	DNC	DNC	do not connect
R6	DNC	DNC	do not connect	T10	VSS	P	VSS
R7	DNC	DNC	do not connect	T11	VSS	P	VSS
R8	DNC	DNC	do not connect	T12	VDD_IO	P	VDD33
R9	DNC	DNC	do not connect	T13	VDD	P	VDD18
R10	VSS	P	VSS	T14	VSS	P	VSS
R11	VSS	P	VSS	T15	VSS	P	VSS
R12	VDD_IO	P	VDD33	T16	VDD	P	VDD18
R13	VDD	P	VDD18	T17	VDD	P	VDD18
R14	VSS	P	VSS	T18	VDD	P	VDD18

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
T19	VDD	P	VDD18	U23	VSS	P	VSS
T20	VDD	P	VDD18	U24	VDD	P	VDD18
T21	VDD	P	VDD18	U25	VSS	P	VSS
T22	VDD	P	VDD18	U26	VSS	P	VSS
T23	VDD	P	VDD18	U27	VDD_SD	P	VAA18
T24	VDD	P	VDD18	U28	VDD_TX	P	VAA25
T25	VSS	P	VSS	U29	VSS	P	VSS
T26	VSS	P	VSS	U30	VSS	P	VSS
T27	VDD_SD	P	VAA18	U31	DNC	DNC	do not connect
T28	VDD_TX	P	VAA25	U32	DNC	DNC	do not connect
T29	VSS	P	VSS	U33	DNC	DNC	do not connect
T30	VSS	P	VSS	U34	DNC	DNC	do not connect
T31	DNC	DNC	do not connect	U35	DNC	DNC	do not connect
T32	DNC	DNC	do not connect	U36	VSS	P	VSS
T33	DNC	DNC	do not connect	U37	TXN[16]	O	Serdes diff output
T34	DNC	DNC	do not connect	U38	VSS	P	VSS
T35	DNC	DNC	do not connect	U39	RXN[16]	I	Serdes diff input
T36	VSS	P	VSS	V1	DNC	DNC	do not connect
T37	TXP[17]	O	Serdes diff output	V2	ZTICK_MODE	I	3.3V LVTTTL
T38	VSS	P	VSS	V3	RPU	I	RPU
T39	RXP[17]	I	Serdes diff input	V4	ZTICK	I	3.3V LVTTTL
U1	VSS	P	VSS	V5	DNC	DNC	do not connect
U2	PLL_DIV_RST_N	I	3.3V LVTTTL	V6	PLL_SYS_VDDA	P	3.3V AVDD
U3	DNC	DNC	do not connect	V7	DNC	DNC	do not connect
U4	DNC	DNC	do not connect	V8	PLL_SYS_VDD	P	1.8V AVDD
U5	DNC	DNC	do not connect	V9	DNC	DNC	do not connect
U6	DNC	DNC	do not connect	V10	VSS	P	VSS
U7	DNC	DNC	do not connect	V11	VSS	P	VSS
U8	DNC	DNC	do not connect	V12	VDD_IO	P	VDD33
U9	DNC	DNC	do not connect	V13	VDD	P	VDD18
U10	VSS	P	VSS	V14	VSS	P	VSS
U11	VSS	P	VSS	V15	VSS	P	VSS
U12	VDD_IO	P	VDD33	V16	VDD	P	VDD18
U13	VDD	P	VDD18	V17	VSS	P	VSS
U14	VSS	P	VSS	V18	VSS	P	VSS
U15	VSS	P	VSS	V19	VSS	P	VSS
U16	VDD	P	VDD18	V20	VSS	P	VSS
U17	VSS	P	VSS	V21	VSS	P	VSS
U18	VSS	P	VSS	V22	VSS	P	VSS
U19	VSS	P	VSS	V23	VSS	P	VSS
U20	VSS	P	VSS	V24	VDD	P	VDD18
U21	VSS	P	VSS	V25	VSS	P	VSS
U22	VSS	P	VSS	V26	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
V27	VDD_SD	P	VAA18	W31	DNC	DNC	do not connect
V28	VDD_TX	P	VAA25	W32	DNC	DNC	do not connect
V29	VSS	P	VSS	W33	DNC	DNC	do not connect
V30	VSS	P	VSS	W34	DNC	DNC	do not connect
V31	DNC	DNC	do not connect	W35	DNC	DNC	do not connect
V32	DNC	DNC	do not connect	W36	VSS	P	VSS
V33	DNC	DNC	do not connect	W37	VSS	P	VSS
V34	DNC	DNC	do not connect	W38	VSS	P	VSS
V35	DNC	DNC	do not connect	W39	VSS	P	VSS
V36	VSS	P	VSS	Y1	VSS	P	VSS
V37	TXP[16]	O	Serdes diff output	Y2	VSS	P	VSS
V38	VSS	P	VSS	Y3	VSS	P	VSS
V39	RXP[16]	I	Serdes diff input	Y4	VSS	P	VSS
W1	DNC	DNC	do not connect	Y5	DNC	DNC	do not connect
W2	RPU	I	RPU	Y6	DNC	DNC	do not connect
W3	PLL_SYS_LCK	O	3.3V LVTTTL	Y7	DNC	DNC	do not connect
W4	VSS	P	VSS	Y8	DNC	DNC	do not connect
W5	DNC	DNC	do not connect	Y9	DNC	DNC	do not connect
W6	PLL_SYS_VSSA	P	AVSS	Y10	VSS	P	VSS
W7	DNC	DNC	do not connect	Y11	VSS	P	VSS
W8	PLL_SYS_VSS	P	VSS	Y12	VDD_IO	P	VDD33
W9	DNC	DNC	do not connect	Y13	VDD	P	VDD18
W10	VSS	P	VSS	Y14	VSS	P	VSS
W11	VSS	P	VSS	Y15	VSS	P	VSS
W12	VDD_IO	P	VDD33	Y16	VDD	P	VDD18
W13	VDD	P	VDD18	Y17	VSS	P	VSS
W14	VSS	P	VSS	Y18	VSS	P	VSS
W15	VSS	P	VSS	Y19	VSS	P	VSS
W16	VDD	P	VDD18	Y20	VDD	P	VDD18
W17	VSS	P	VSS	Y21	VDD	P	VDD18
W18	VSS	P	VSS	Y22	VSS	P	VSS
W19	VSS	P	VSS	Y23	VSS	P	VSS
W20	VDD	P	VDD18	Y24	VDD	P	VDD18
W21	VDD	P	VDD18	Y25	VSS	P	VSS
W22	VSS	P	VSS	Y26	VSS	P	VSS
W23	VSS	P	VSS	Y27	VDD_SD	P	VAA18
W24	VDD	P	VDD18	Y28	VDD_TX	P	VAA25
W25	VSS	P	VSS	Y29	VSS	P	VSS
W26	VSS	P	VSS	Y30	VSS	P	VSS
W27	VDD_SD	P	VAA18	Y31	VDD_SD1_PLL	P	VAA18
W28	VDD_TX	P	VAA25	Y32	DNC	DNC	do not connect
W29	VSS	P	VSS	Y33	DNC	DNC	do not connect
W30	VSS_SD1_PLL	P	VSS	Y34	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
Y35	DNC	DNC	do not connect	AA39	SD1_REFCLKP	I	Serdes diff clock
Y36	DNC	DNC	do not connect	AB1	VSS	P	VSS
Y37	DNC	DNC	do not connect	AB2	VSS	P	VSS
Y38	VSS	P	VSS	AB3	PLL_RST	I	3.3V LVTTTL
Y39	SD1_REFCLKN	I	Serdes diff clock	AB4	RPD	I	RPD
AA1	SYS_CLK	I	3.3V LVTTTL	AB5	DNC	DNC	do not connect
AA2	VSS	P	VSS	AB6	PLL_CORE_VDD	P	1.8V AVDD
AA3	PLL_CORE_LCK	O	3.3V LVTTTL	AB7	DNC	DNC	do not connect
AA4	RPU	I	RPU	AB8	PLL_CORE_VDDA	P	3.3V AVDD
AA5	DNC	DNC	do not connect	AB9	DNC	DNC	do not connect
AA6	PLL_CORE_VSS	P	VSS	AB10	VSS	P	VSS
AA7	DNC	DNC	do not connect	AB11	VSS	P	VSS
AA8	PLL_CORE_VSSA	P	AVSS	AB12	VDD_IO	P	VDD33
AA9	DNC	DNC	do not connect	AB13	VDD	P	VDD18
AA10	VSS	P	VSS	AB14	VSS	P	VSS
AA11	VSS	P	VSS	AB15	VSS	P	VSS
AA12	VDD_IO	P	VDD33	AB16	VDD	P	VDD18
AA13	VDD	P	VDD18	AB17	VSS	P	VSS
AA14	VSS	P	VSS	AB18	VSS	P	VSS
AA15	VSS	P	VSS	AB19	VSS	P	VSS
AA16	VDD	P	VDD18	AB20	VSS	P	VSS
AA17	VSS	P	VSS	AB21	VSS	P	VSS
AA18	VSS	P	VSS	AB22	VSS	P	VSS
AA19	VSS	P	VSS	AB23	VSS	P	VSS
AA20	VDD	P	VDD18	AB24	VDD	P	VDD18
AA21	VDD	P	VDD18	AB25	VSS	P	VSS
AA22	VSS	P	VSS	AB26	VSS	P	VSS
AA23	VSS	P	VSS	AB27	VDD_SD	P	VAA18
AA24	VDD	P	VDD18	AB28	VDD_TX	P	VAA25
AA25	VSS	P	VSS	AB29	VSS	P	VSS
AA26	VSS	P	VSS	AB30	VSS	P	VSS
AA27	VDD_SD	P	VAA18	AB31	DNC	DNC	do not connect
AA28	VDD_TX	P	VAA25	AB32	DNC	DNC	do not connect
AA29	VSS	P	VSS	AB33	DNC	DNC	do not connect
AA30	VSS	P	VSS	AB34	DNC	DNC	do not connect
AA31	VDD_REFCLK1	P	VAA33	AB35	DNC	DNC	do not connect
AA32	DNC	DNC	do not connect	AB36	VSS	P	VSS
AA33	VSS	P	VSS	AB37	VSS	P	VSS
AA34	VSS	P	VSS	AB38	VSS	P	VSS
AA35	VSS	P	VSS	AB39	VSS	P	VSS
AA36	SD1_REF_RES	B	Serdes Bidi	AC1	DNC	DNC	do not connect
AA37	RPD	I	RPD	AC2	RPD	I	RPD
AA38	VSS	P	VSS	AC3	RPD	I	RPD

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AC4	RPD	I	RPD	AD8	DNC	DNC	do not connect
AC5	DNC	DNC	do not connect	AD9	DNC	DNC	do not connect
AC6	DNC	DNC	do not connect	AD10	VSS	P	VSS
AC7	DNC	DNC	do not connect	AD11	VSS	P	VSS
AC8	DNC	DNC	do not connect	AD12	VDD_IO	P	VDD33
AC9	DNC	DNC	do not connect	AD13	VDD	P	VDD18
AC10	VSS	P	VSS	AD14	VSS	P	VSS
AC11	VSS	P	VSS	AD15	VSS	P	VSS
AC12	VDD_IO	P	VDD33	AD16	VDD	P	VDD18
AC13	VDD	P	VDD18	AD17	VDD	P	VDD18
AC14	VSS	P	VSS	AD18	VDD	P	VDD18
AC15	VSS	P	VSS	AD19	VDD	P	VDD18
AC16	VDD	P	VDD18	AD20	VDD	P	VDD18
AC17	VSS	P	VSS	AD21	VDD	P	VDD18
AC18	VSS	P	VSS	AD22	VDD	P	VDD18
AC19	VSS	P	VSS	AD23	VDD	P	VDD18
AC20	VSS	P	VSS	AD24	VDD	P	VDD18
AC21	VSS	P	VSS	AD25	VSS	P	VSS
AC22	VSS	P	VSS	AD26	VSS	P	VSS
AC23	VSS	P	VSS	AD27	VDD_SD	P	VAA18
AC24	VDD	P	VDD18	AD28	VDD_TX	P	VAA25
AC25	VSS	P	VSS	AD29	VSS	P	VSS
AC26	VSS	P	VSS	AD30	VSS	P	VSS
AC27	VDD_SD	P	VAA18	AD31	DNC	DNC	do not connect
AC28	VDD_TX	P	VAA25	AD32	DNC	DNC	do not connect
AC29	VSS	P	VSS	AD33	DNC	DNC	do not connect
AC30	VSS	P	VSS	AD34	DNC	DNC	do not connect
AC31	DNC	DNC	do not connect	AD35	DNC	DNC	do not connect
AC32	DNC	DNC	do not connect	AD36	VSS	P	VSS
AC33	DNC	DNC	do not connect	AD37	TXP[15]	O	Serdes diff output
AC34	DNC	DNC	do not connect	AD38	VSS	P	VSS
AC35	DNC	DNC	do not connect	AD39	RXP[15]	I	Serdes diff input
AC36	VSS	P	VSS	AE1	DNC	DNC	do not connect
AC37	TXN[15]	O	Serdes diff output	AE2	DNC	DNC	do not connect
AC38	VSS	P	VSS	AE3	DNC	DNC	do not connect
AC39	RXN[15]	I	Serdes diff input	AE4	DNC	DNC	do not connect
AD1	VDD_IO	P	VDD33	AE5	DNC	DNC	do not connect
AD2	DNC	DNC	do not connect	AE6	DNC	DNC	do not connect
AD3	DNC	DNC	do not connect	AE7	DNC	DNC	do not connect
AD4	DNC	DNC	do not connect	AE8	DNC	DNC	do not connect
AD5	DNC	DNC	do not connect	AE9	DNC	DNC	do not connect
AD6	DNC	DNC	do not connect	AE10	VSS	P	VSS
AD7	DNC	DNC	do not connect	AE11	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AE12	VDD_IO	P	VDD33	AF16	VSS	P	VSS
AE13	VDD	P	VDD18	AF17	VSS	P	VSS
AE14	VSS	P	VSS	AF18	VSS	P	VSS
AE15	VSS	P	VSS	AF19	VSS	P	VSS
AE16	VSS	P	VSS	AF20	VSS	P	VSS
AE17	VSS	P	VSS	AF21	VSS	P	VSS
AE18	VSS	P	VSS	AF22	VSS	P	VSS
AE19	VSS	P	VSS	AF23	VSS	P	VSS
AE20	VSS	P	VSS	AF24	VSS	P	VSS
AE21	VSS	P	VSS	AF25	VSS	P	VSS
AE22	VSS	P	VSS	AF26	VSS	P	VSS
AE23	VSS	P	VSS	AF27	VDD_SD	P	VAA18
AE24	VSS	P	VSS	AF28	VDD_TX	P	VAA25
AE25	VSS	P	VSS	AF29	VSS	P	VSS
AE26	VSS	P	VSS	AF30	VSS	P	VSS
AE27	VDD_SD	P	VAA18	AF31	DNC	DNC	do not connect
AE28	VDD_TX	P	VAA25	AF32	DNC	DNC	do not connect
AE29	VSS	P	VSS	AF33	DNC	DNC	do not connect
AE30	VSS	P	VSS	AF34	DNC	DNC	do not connect
AE31	DNC	DNC	do not connect	AF35	DNC	DNC	do not connect
AE32	DNC	DNC	do not connect	AF36	VSS	P	VSS
AE33	DNC	DNC	do not connect	AF37	TXP[14]	O	Serdes diff output
AE34	DNC	DNC	do not connect	AF38	VSS	P	VSS
AE35	DNC	DNC	do not connect	AF39	RXP[14]	I	Serdes diff input
AE36	VSS	P	VSS	AG1	DNC	DNC	do not connect
AE37	TXN[14]	O	Serdes diff output	AG2	DNC	DNC	do not connect
AE38	VSS	P	VSS	AG3	DNC	DNC	do not connect
AE39	RXN[14]	I	Serdes diff input	AG4	DNC	DNC	do not connect
AF1	VSS	P	VSS	AG5	DNC	DNC	do not connect
AF2	DNC	DNC	do not connect	AG6	DNC	DNC	do not connect
AF3	DNC	DNC	do not connect	AG7	DNC	DNC	do not connect
AF4	VDD_IO	P	VDD33	AG8	DNC	DNC	do not connect
AF5	DNC	DNC	do not connect	AG9	DNC	DNC	do not connect
AF6	DNC	DNC	do not connect	AG10	VSS	P	VSS
AF7	DNC	DNC	do not connect	AG11	VSS	P	VSS
AF8	DNC	DNC	do not connect	AG12	VDD_IO	P	VDD33
AF9	DNC	DNC	do not connect	AG13	VDD	P	VDD18
AF10	VSS	P	VSS	AG14	VDD	P	VDD18
AF11	VSS	P	VSS	AG15	VDD	P	VDD18
AF12	VDD_IO	P	VDD33	AG16	VDD	P	VDD18
AF13	VDD	P	VDD18	AG17	VDD	P	VDD18
AF14	VSS	P	VSS	AG18	DNC	DNC	do not connect
AF15	VSS	P	VSS	AG19	VDD_SD	P	VAA18

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AG20	VDD_SD	P	VAA18	AH24	VDD_TX	P	VAA25
AG21	VDD_SD	P	VAA18	AH25	VDD_TX	P	VAA25
AG22	VDD_SD	P	VAA18	AH26	VDD_TX	P	VAA25
AG23	VDD_SD	P	VAA18	AH27	VDD_TX	P	VAA25
AG24	VDD_SD	P	VAA18	AH28	VDD_TX	P	VAA25
AG25	VDD_SD	P	VAA18	AH29	VSS	P	VSS
AG26	VDD_SD	P	VAA18	AH30	VSS	P	VSS
AG27	VDD_SD	P	VAA18	AH31	DNC	DNC	do not connect
AG28	VDD_TX	P	VAA25	AH32	DNC	DNC	do not connect
AG29	VSS	P	VSS	AH33	DNC	DNC	do not connect
AG30	VSS	P	VSS	AH34	DNC	DNC	do not connect
AG31	DNC	DNC	do not connect	AH35	DNC	DNC	do not connect
AG32	DNC	DNC	do not connect	AH36	VSS	P	VSS
AG33	DNC	DNC	do not connect	AH37	TXP[13]	O	Serdes diff output
AG34	DNC	DNC	do not connect	AH38	VSS	P	VSS
AG35	DNC	DNC	do not connect	AH39	RXP[13]	I	Serdes diff input
AG36	VSS	P	VSS	AJ1	DNC	DNC	do not connect
AG37	TXN[13]	O	Serdes diff output	AJ2	DNC	DNC	do not connect
AG38	VSS	P	VSS	AJ3	DNC	DNC	do not connect
AG39	RXN[13]	I	Serdes diff input	AJ4	DNC	DNC	do not connect
AH1	DNC	DNC	do not connect	AJ5	DNC	DNC	do not connect
AH2	DNC	DNC	do not connect	AJ6	DNC	DNC	do not connect
AH3	DNC	DNC	do not connect	AJ7	DNC	DNC	do not connect
AH4	DNC	DNC	do not connect	AJ8	DNC	DNC	do not connect
AH5	DNC	DNC	do not connect	AJ9	DNC	DNC	do not connect
AH6	DNC	DNC	do not connect	AJ10	VSS	P	VSS
AH7	DNC	DNC	do not connect	AJ11	VSS	P	VSS
AH8	DNC	DNC	do not connect	AJ12	VSS	P	VSS
AH9	DNC	DNC	do not connect	AJ13	VSS	P	VSS
AH10	VSS	P	VSS	AJ14	VSS	P	VSS
AH11	VSS	P	VSS	AJ15	VSS	P	VSS
AH12	VDD_IO	P	VDD33	AJ16	VSS	P	VSS
AH13	VDD_IO	P	VDD33	AJ17	VSS	P	VSS
AH14	VDD_IO	P	VDD33	AJ18	DNC	DNC	do not connect
AH15	VDD_IO	P	VDD33	AJ19	VSS	P	VSS
AH16	VDD_IO	P	VDD33	AJ20	VSS	P	VSS
AH17	VDD_IO	P	VDD33	AJ21	VSS	P	VSS
AH18	DNC	DNC	do not connect	AJ22	VSS	P	VSS
AH19	VDD_TX	P	VAA25	AJ23	VSS	P	VSS
AH20	VDD_TX	P	VAA25	AJ24	VSS	P	VSS
AH21	VDD_TX	P	VAA25	AJ25	VSS	P	VSS
AH22	VDD_TX	P	VAA25	AJ26	VSS	P	VSS
AH23	VDD_TX	P	VAA25	AJ27	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AJ28	VSS	P	VSS	AK32	DNC	DNC	do not connect
AJ29	VSS	P	VSS	AK33	DNC	DNC	do not connect
AJ30	VSS	P	VSS	AK34	DNC	DNC	do not connect
AJ31	DNC	DNC	do not connect	AK35	DNC	DNC	do not connect
AJ32	DNC	DNC	do not connect	AK36	VSS	P	VSS
AJ33	DNC	DNC	do not connect	AK37	TXP[12]	O	Serdes diff output
AJ34	DNC	DNC	do not connect	AK38	VSS	P	VSS
AJ35	DNC	DNC	do not connect	AK39	RXP[12]	I	Serdes diff input
AJ36	VSS	P	VSS	AL1	DNC	DNC	do not connect
AJ37	TXN[12]	O	Serdes diff output	AL2	DNC	DNC	do not connect
AJ38	VSS	P	VSS	AL3	DNC	DNC	do not connect
AJ39	RXN[12]	I	Serdes diff input	AL4	DNC	DNC	do not connect
AK1	VSS	P	VSS	AL5	DNC	DNC	do not connect
AK2	DNC	DNC	do not connect	AL6	DNC	DNC	do not connect
AK3	DNC	DNC	do not connect	AL7	DNC	DNC	do not connect
AK4	VDD_IO	P	VDD33	AL8	DNC	DNC	do not connect
AK5	DNC	DNC	do not connect	AL9	DNC	DNC	do not connect
AK6	DNC	DNC	do not connect	AL10	DNC	DNC	do not connect
AK7	DNC	DNC	do not connect	AL11	DNC	DNC	do not connect
AK8	DNC	DNC	do not connect	AL12	DNC	DNC	do not connect
AK9	DNC	DNC	do not connect	AL13	DNC	DNC	do not connect
AK10	VSS	P	VSS	AL14	DNC	DNC	do not connect
AK11	VSS	P	VSS	AL15	DNC	DNC	do not connect
AK12	VSS	P	VSS	AL16	DNC	DNC	do not connect
AK13	VSS	P	VSS	AL17	DNC	DNC	do not connect
AK14	VSS	P	VSS	AL18	DNC	DNC	do not connect
AK15	VSS	P	VSS	AL19	VSS	P	VSS
AK16	VSS	P	VSS	AL20	DNC	DNC	do not connect
AK17	VSS	P	VSS	AL21	DNC	DNC	do not connect
AK18	DNC	DNC	do not connect	AL22	VDD_REFCLK0	P	VAA33
AK19	VSS	P	VSS	AL23	VDD_SD0_PLL	P	VAA18
AK20	VSS	P	VSS	AL24	DNC	DNC	do not connect
AK21	VSS	P	VSS	AL25	DNC	DNC	do not connect
AK22	VSS	P	VSS	AL26	DNC	DNC	do not connect
AK23	VSS	P	VSS	AL27	DNC	DNC	do not connect
AK24	VSS_SD0_PLL	P	VSS	AL28	DNC	DNC	do not connect
AK25	VSS	P	VSS	AL29	DNC	DNC	do not connect
AK26	VSS	P	VSS	AL30	DNC	DNC	do not connect
AK27	VSS	P	VSS	AL31	DNC	DNC	do not connect
AK28	VSS	P	VSS	AL32	DNC	DNC	do not connect
AK29	VSS	P	VSS	AL33	DNC	DNC	do not connect
AK30	VSS	P	VSS	AL34	DNC	DNC	do not connect
AK31	DNC	DNC	do not connect	AL35	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AL36	VSS	P	VSS	AN1	DNC	DNC	do not connect
AL37	TXN[11]	O	Serdes diff output	AN2	DNC	DNC	do not connect
AL38	VSS	P	VSS	AN3	DNC	DNC	do not connect
AL39	RXN[11]	I	Serdes diff input	AN4	DNC	DNC	do not connect
AM1	DNC	DNC	do not connect	AN5	DNC	DNC	do not connect
AM2	DNC	DNC	do not connect	AN6	DNC	DNC	do not connect
AM3	DNC	DNC	do not connect	AN7	DNC	DNC	do not connect
AM4	DNC	DNC	do not connect	AN8	DNC	DNC	do not connect
AM5	DNC	DNC	do not connect	AN9	DNC	DNC	do not connect
AM6	DNC	DNC	do not connect	AN10	DNC	DNC	do not connect
AM7	DNC	DNC	do not connect	AN11	DNC	DNC	do not connect
AM8	DNC	DNC	do not connect	AN12	DNC	DNC	do not connect
AM9	DNC	DNC	do not connect	AN13	DNC	DNC	do not connect
AM10	DNC	DNC	do not connect	AN14	DNC	DNC	do not connect
AM11	DNC	DNC	do not connect	AN15	DNC	DNC	do not connect
AM12	DNC	DNC	do not connect	AN16	DNC	DNC	do not connect
AM13	DNC	DNC	do not connect	AN17	DNC	DNC	do not connect
AM14	DNC	DNC	do not connect	AN18	DNC	DNC	do not connect
AM15	DNC	DNC	do not connect	AN19	DNC	DNC	do not connect
AM16	DNC	DNC	do not connect	AN20	DNC	DNC	do not connect
AM17	DNC	DNC	do not connect	AN21	DNC	DNC	do not connect
AM18	DNC	DNC	do not connect	AN22	DNC	DNC	do not connect
AM19	DNC	DNC	do not connect	AN23	DNC	DNC	do not connect
AM20	DNC	DNC	do not connect	AN24	DNC	DNC	do not connect
AM21	DNC	DNC	do not connect	AN25	DNC	DNC	do not connect
AM22	DNC	DNC	do not connect	AN26	DNC	DNC	do not connect
AM23	DNC	DNC	do not connect	AN27	DNC	DNC	do not connect
AM24	DNC	DNC	do not connect	AN28	DNC	DNC	do not connect
AM25	DNC	DNC	do not connect	AN29	DNC	DNC	do not connect
AM26	DNC	DNC	do not connect	AN30	DNC	DNC	do not connect
AM27	DNC	DNC	do not connect	AN31	DNC	DNC	do not connect
AM28	DNC	DNC	do not connect	AN32	DNC	DNC	do not connect
AM29	DNC	DNC	do not connect	AN33	DNC	DNC	do not connect
AM30	DNC	DNC	do not connect	AN34	DNC	DNC	do not connect
AM31	DNC	DNC	do not connect	AN35	DNC	DNC	do not connect
AM32	DNC	DNC	do not connect	AN36	VSS	P	VSS
AM33	DNC	DNC	do not connect	AN37	TXN[10]	O	Serdes diff output
AM34	DNC	DNC	do not connect	AN38	VSS	P	VSS
AM35	DNC	DNC	do not connect	AN39	RXN[10]	I	Serdes diff input
AM36	VSS	P	VSS	AP1	DNC	DNC	do not connect
AM37	TXP[11]	O	Serdes diff output	AP2	DNC	DNC	do not connect
AM38	VSS	P	VSS	AP3	DNC	DNC	do not connect
AM39	RXP[11]	I	Serdes diff input	AP4	DNC	DNC	do not connect

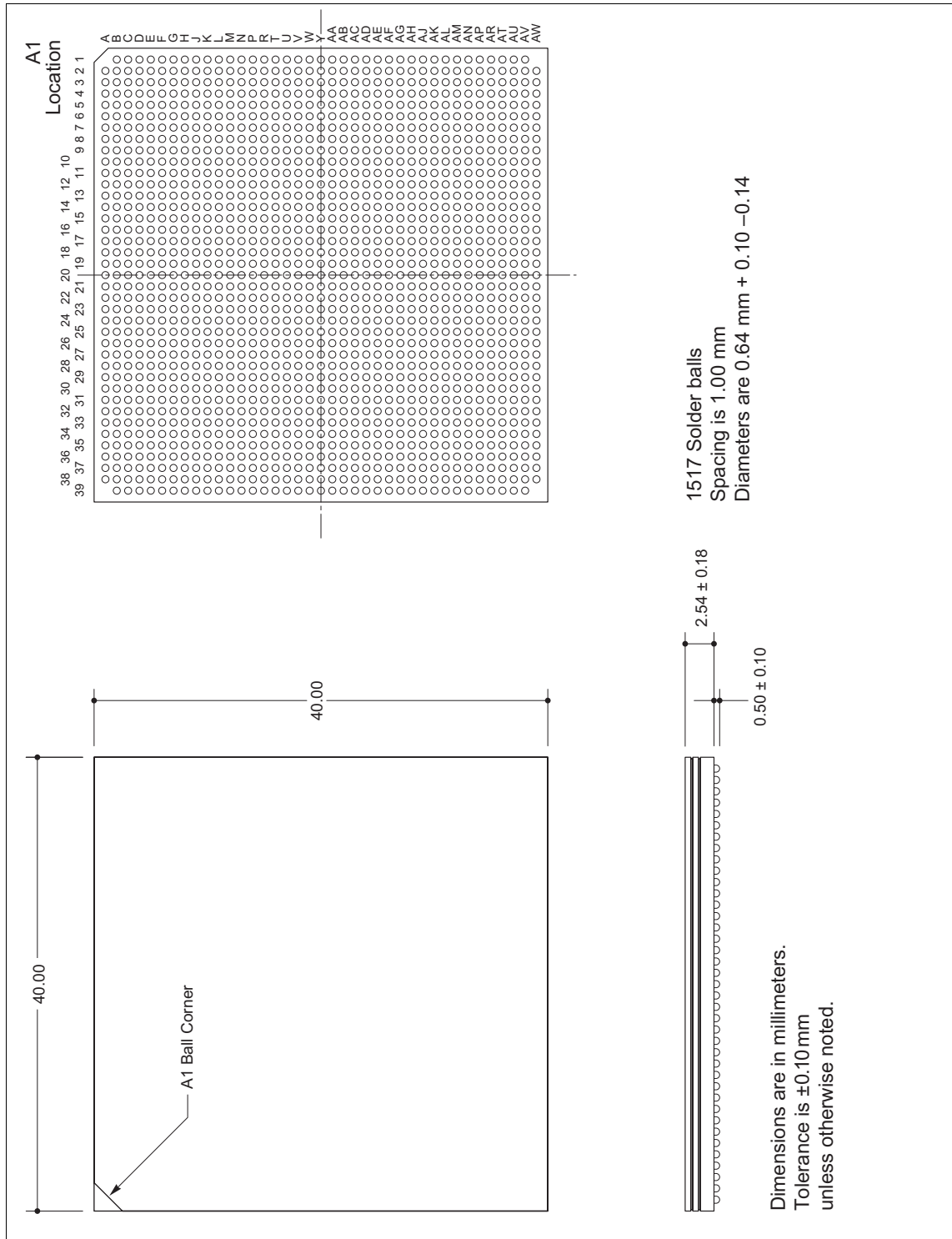
Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AP5	DNC	DNC	do not connect	AR9	DNC	DNC	do not connect
AP6	DNC	DNC	do not connect	AR10	DNC	DNC	do not connect
AP7	DNC	DNC	do not connect	AR11	DNC	DNC	do not connect
AP8	DNC	DNC	do not connect	AR12	DNC	DNC	do not connect
AP9	DNC	DNC	do not connect	AR13	DNC	DNC	do not connect
AP10	DNC	DNC	do not connect	AR14	DNC	DNC	do not connect
AP11	DNC	DNC	do not connect	AR15	DNC	DNC	do not connect
AP12	DNC	DNC	do not connect	AR16	DNC	DNC	do not connect
AP13	DNC	DNC	do not connect	AR17	DNC	DNC	do not connect
AP14	DNC	DNC	do not connect	AR18	DNC	DNC	do not connect
AP15	DNC	DNC	do not connect	AR19	DNC	DNC	do not connect
AP16	DNC	DNC	do not connect	AR20	DNC	DNC	do not connect
AP17	DNC	DNC	do not connect	AR21	DNC	DNC	do not connect
AP18	DNC	DNC	do not connect	AR22	DNC	DNC	do not connect
AP19	DNC	DNC	do not connect	AR23	DNC	DNC	do not connect
AP20	DNC	DNC	do not connect	AR24	VSS	P	VSS
AP21	DNC	DNC	do not connect	AR25	DNC	DNC	do not connect
AP22	DNC	DNC	do not connect	AR26	DNC	DNC	do not connect
AP23	DNC	DNC	do not connect	AR27	DNC	DNC	do not connect
AP24	DNC	DNC	do not connect	AR28	DNC	DNC	do not connect
AP25	DNC	DNC	do not connect	AR29	DNC	DNC	do not connect
AP26	DNC	DNC	do not connect	AR30	DNC	DNC	do not connect
AP27	DNC	DNC	do not connect	AR31	DNC	DNC	do not connect
AP28	DNC	DNC	do not connect	AR32	DNC	DNC	do not connect
AP29	DNC	DNC	do not connect	AR33	DNC	DNC	do not connect
AP30	DNC	DNC	do not connect	AR34	DNC	DNC	do not connect
AP31	DNC	DNC	do not connect	AR35	DNC	DNC	do not connect
AP32	DNC	DNC	do not connect	AR36	VSS	P	VSS
AP33	DNC	DNC	do not connect	AR37	TXN[09]	O	Serdes diff output
AP34	DNC	DNC	do not connect	AR38	VSS	P	VSS
AP35	DNC	DNC	do not connect	AR39	RXN[09]	I	Serdes diff input
AP36	VSS	P	VSS	AT1	DNC	DNC	do not connect
AP37	TXP[10]	O	Serdes diff output	AT2	DNC	DNC	do not connect
AP38	VSS	P	VSS	AT3	ZBUS_DEVID[0]	I	3.3V LVTTTL
AP39	RXP[10]	I	Serdes diff input	AT4	VDD_IO	P	VDD33
AR1	DNC	DNC	do not connect	AT5	ZBUS_AVALID_N	I	3.3V LVTTTL
AR2	DNC	DNC	do not connect	AT6	VSS	P	VSS
AR3	RESET_N	I	3.3V LVTTTL	AT7	ZBUS_AD[04]	B	3.3V LVTTTL
AR4	DNC	DNC	do not connect	AT8	VDD_IO	P	VDD33
AR5	ZBUS_DEVID[2]	I	3.3V LVTTTL	AT9	ZBUS_AD[12]	B	3.3V LVTTTL
AR6	ZBUS_DEVID[4]	I	3.3V LVTTTL	AT10	VSS	P	VSS
AR7	ZBUS_DEVID[3]	I	3.3V LVTTTL	AT11	DNC	DNC	do not connect
AR8	DNC	DNC	do not connect	AT12	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AT13	DNC	DNC	do not connect	AU17	TXP[01]	O	Serdes diff output
AT14	VSS	P	VSS	AU18	TXN[01]	O	Serdes diff output
AT15	VSS	P	VSS	AU19	TXP[02]	O	Serdes diff output
AT16	VSS	P	VSS	AU20	TXN[02]	O	Serdes diff output
AT17	VSS	P	VSS	AU21	TXP[03]	O	Serdes diff output
AT18	VSS	P	VSS	AU22	TXN[03]	O	Serdes diff output
AT19	VSS	P	VSS	AU23	VSS	P	VSS
AT20	VSS	P	VSS	AU24	RPD	I	RPD
AT21	VSS	P	VSS	AU25	DNC	DNC	do not connect
AT22	VSS	P	VSS	AU26	VSS	P	VSS
AT23	VSS	P	VSS	AU27	TXP[04]	O	Serdes diff output
AT24	SD0_REF_RES	B	Serdes Bidi	AU28	TXN[04]	O	Serdes diff output
AT25	DNC	DNC	do not connect	AU29	TXP[05]	O	Serdes diff output
AT26	VSS	P	VSS	AU30	TXN[05]	O	Serdes diff output
AT27	VSS	P	VSS	AU31	TXP[06]	O	Serdes diff output
AT28	VSS	P	VSS	AU32	TXN[06]	O	Serdes diff output
AT29	VSS	P	VSS	AU33	TXP[07]	O	Serdes diff output
AT30	VSS	P	VSS	AU34	TXN[07]	O	Serdes diff output
AT31	VSS	P	VSS	AU35	VSS	P	VSS
AT32	VSS	P	VSS	AU36	VSS	P	VSS
AT33	VSS	P	VSS	AU37	TXN[08]	O	Serdes diff output
AT34	VSS	P	VSS	AU38	VSS	P	VSS
AT35	VSS	P	VSS	AU39	RXN[08]	I	Serdes diff input
AT36	VSS	P	VSS	AV1	VDD_IO	P	VDD33
AT37	TXP[09]	O	Serdes diff output	AV2	ZBUS_DEVID[1]	I	3.3V LVTTTL
AT38	VSS	P	VSS	AV3	ZBUS_CLK	I	3.3V LVTTTL
AT39	RXP[09]	I	Serdes diff input	AV4	ZBUS_AD[02]	B	3.3V LVTTTL
AU1	VSS	P	VSS	AV5	ZBUS_AD[07]	B	3.3V LVTTTL
AU2	CHN_DET_MODE	I	3.3V LVTTTL	AV6	ZBUS_AD[08]	B	3.3V LVTTTL
AU3	DNC	DNC	do not connect	AV7	ZBUS_AD[10]	B	3.3V LVTTTL
AU4	ZBUS_AD[01]	B	3.3V LVTTTL	AV8	ZBUS_AD[13]	B	3.3V LVTTTL
AU5	ZBUS_AD[03]	B	3.3V LVTTTL	AV9	ZBUS_PRTY	B	3.3V LVTTTL
AU6	ZBUS_AD[05]	B	3.3V LVTTTL	AV10	ZBUS_DVALID_N	B	3.3V LVTTTL
AU7	ZBUS_AD[06]	B	3.3V LVTTTL	AV11	RPD	I	RPD
AU8	ZBUS_AD[11]	B	3.3V LVTTTL	AV12	VSS	P	VSS
AU9	ZBUS_AD[14]	B	3.3V LVTTTL	AV13	DNC	DNC	do not connect
AU10	DNC	DNC	do not connect	AV14	VSS	P	VSS
AU11	ZBUS_INT_N[1]	O	3.3V LVTTTL	AV15	VSS	P	VSS
AU12	VSS	P	VSS	AV16	VSS	P	VSS
AU13	DNC	DNC	do not connect	AV17	VSS	P	VSS
AU14	VSS	P	VSS	AV18	VSS	P	VSS
AU15	TXP[00]	O	Serdes diff output	AV19	VSS	P	VSS
AU16	TXN[00]	O	Serdes diff output	AV20	VSS	P	VSS

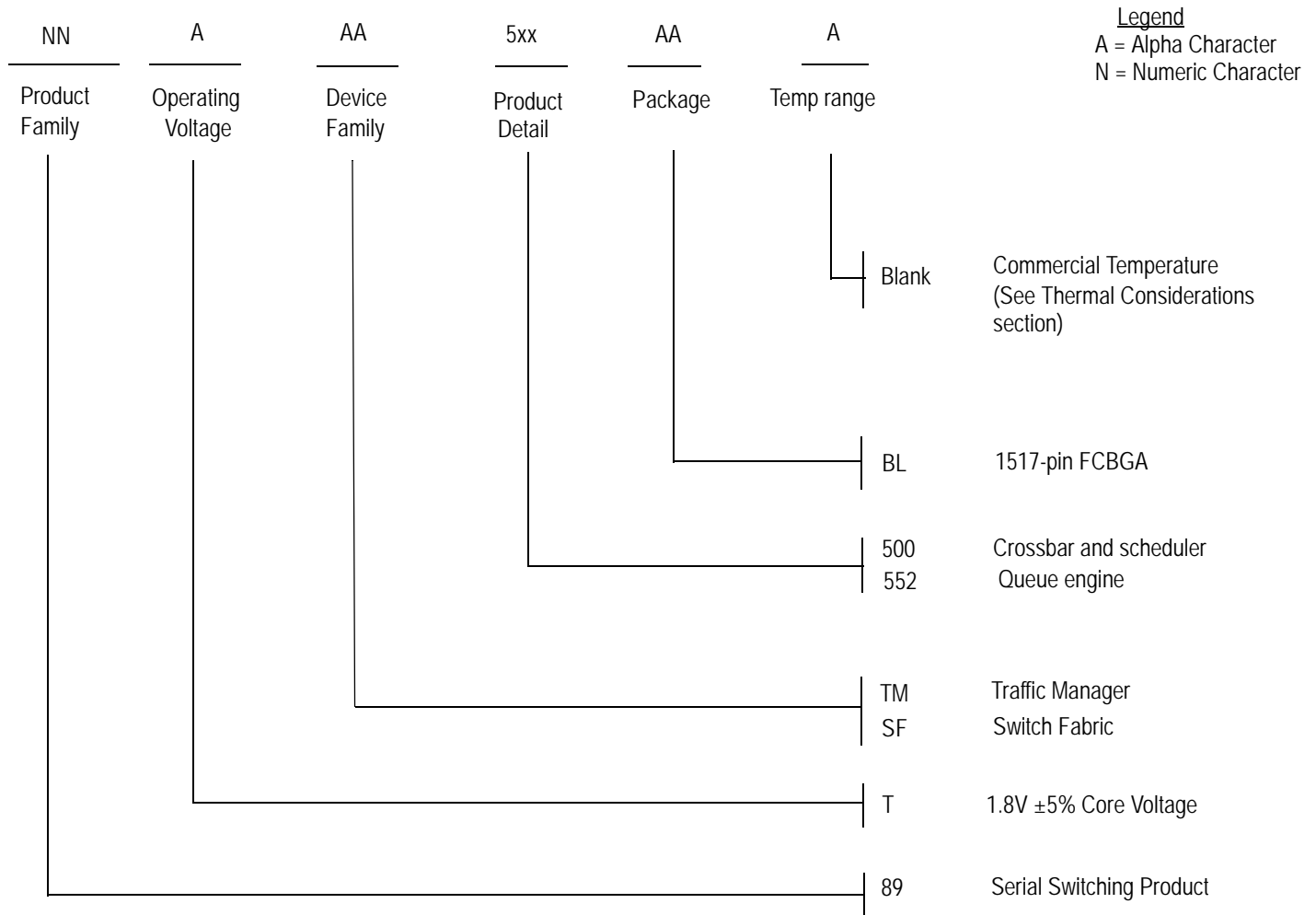
Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AV21	VSS	P	VSS	AW26	VSS	P	VSS
AV22	VSS	P	VSS	AW27	RXP[04]	I	Serdes diff input
AV23	VSS	P	VSS	AW28	RXN[04]	I	Serdes diff input
AV24	VSS	P	VSS	AW29	RXP[05]	I	Serdes diff input
AV25	VSS	P	VSS	AW30	RXN[05]	I	Serdes diff input
AV26	VSS	P	VSS	AW31	RXP[06]	I	Serdes diff input
AV27	VSS	P	VSS	AW32	RXN[06]	I	Serdes diff input
AV28	VSS	P	VSS	AW33	RXP[07]	I	Serdes diff input
AV29	VSS	P	VSS	AW34	RXN[07]	I	Serdes diff input
AV30	VSS	P	VSS	AW35	VSS	P	VSS
AV31	VSS	P	VSS	AW36	VSS	P	VSS
AV32	VSS	P	VSS	AW37	VSS	P	VSS
AV33	VSS	P	VSS	AW38	VSS	P	VSS
AV34	VSS	P	VSS				
AV35	VSS	P	VSS				
AV36	VSS	P	VSS				
AV37	TXP[08]	O	Serdes diff output				
AV38	VSS	P	VSS				
AV39	RXP[08]	I	Serdes diff input				
AW2	ZBUS_AD[00]	B	3.3V LVTTTL				
AW3	VDD_IO	P	VDD33				
AW4	VSS	P	VSS				
AW5	ZBUS_AD[09]	B	3.3V LVTTTL				
AW6	VDD_IO	P	VDD33				
AW7	ZBUS_AD[15]	B	3.3V LVTTTL				
AW8	VSS	P	VSS				
AW9	ZBUS_INT_N[0]	O	3.3V LVTTTL				
AW10	VDD_IO	P	VDD33				
AW11	ZBUS_INT_N[2]	O	3.3V LVTTTL				
AW12	VSS	P	VSS				
AW13	DNC	DNC	do not connect				
AW14	VSS	P	VSS				
AW15	RXP[00]	I	Serdes diff input				
AW16	RXN[00]	I	Serdes diff input				
AW17	RXP[01]	I	Serdes diff input				
AW18	RXN[01]	I	Serdes diff input				
AW19	RXP[02]	I	Serdes diff input				
AW20	RXN[02]	I	Serdes diff input				
AW21	RXP[03]	I	Serdes diff input				
AW22	RXN[03]	I	Serdes diff input				
AW23	VSS	P	VSS				
AW24	SD0_REFCLKP	I	Serdes diff clock				
AW25	SD0_REFCLKN	I	Serdes diff clock				

89TSF500 Package Diagram

The 89TSF500 package is an Amkor FCBGA, having 1517 pins, with 1 mm pitch; a 39x39 pin array; and a 40x40 mm enclosure. The package geometry is shown below.



Ordering Information



Valid Combinations

89TSF500BL

1517-pin FCBGA package, Commercial Temperature

Revision History

November 23, 2004: Initial publication by IDT.



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