12 Lane 3-Port PCI Express® Switch

89PES12N3
Product Brief

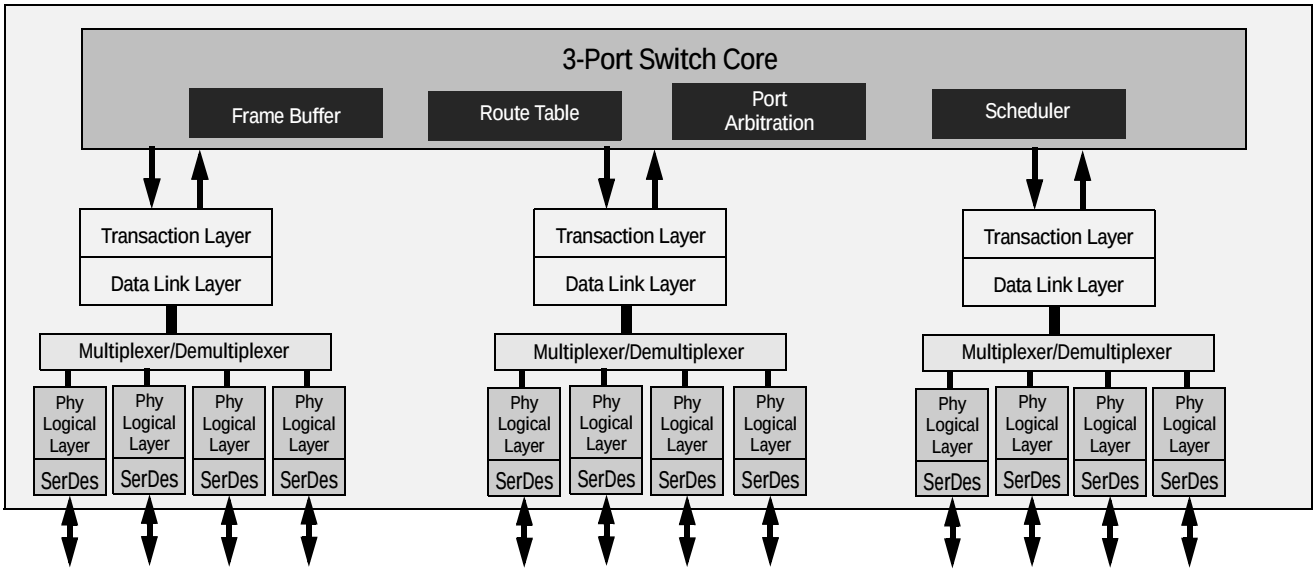
Device Overview

The PES12N3, a 12 lane 3-port PCI Express® switch, is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES12N3 is a peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers and storage. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Three x4 ports with 12 PCI lanes total*
  - *Delivers 6 GBps (48 Gbps) aggregate switching capacity*
  - *Low latency cut-through switch architecture*
  - *Supports 128 to 256 byte maximum payload size*
  - *Supports one virtual channel*
  - *PCI Express Base specification Revision 1.0a compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Port arbitration schemes utilizing round robin or weighted round robin algorithms*
  - *Supports automatic per port link with negotiation (x4, x2, or x1)*
  - *Supports static lane reversal on all ports*
  - *Supports polarity inversion*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates 12 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC passed through*
  - *Supports PCI Express Native Hot-Plug*
    - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- Power Management
  - *Supports PCI Express Power Management Interface Specification, Revision 1.1 (PCI-PM)*
  - *Unused SerDes are disabled*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- Testability and Debug Features
  - *Supports IEEE 1149.6 JTAG*
  - *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*

Block Diagram



- Two SMBus Interfaces
- 8 General Purpose Input/Output pins
- Packaged in 19x19mm 324 ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect the PES12N3 provides the most efficient high-performance I/O connectivity device for applications requiring high throughput, low latency and simple board layout. It provides 6 GBps (48 Gbps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12N3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12N3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes.

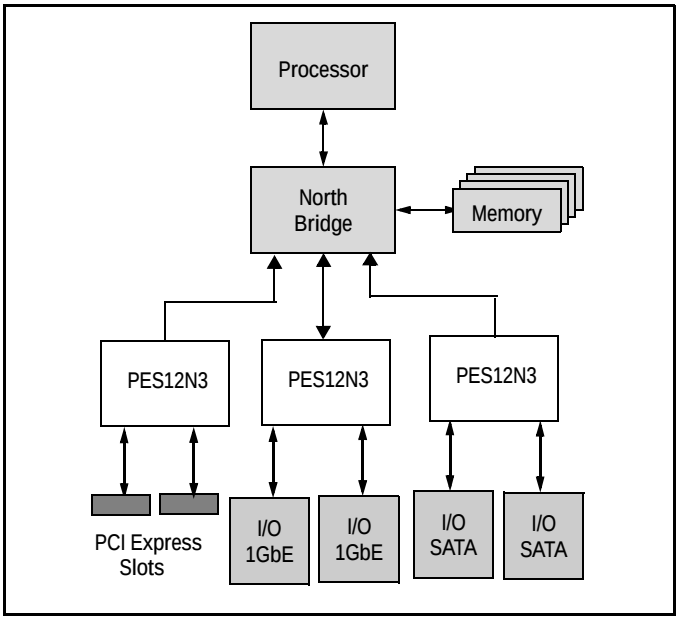


Figure 1 I/O Expansion Application

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