SwitchStar™ Switch Manager

IDT77V550

Features List

- **Interprets switch command cells from external work station and loads the command into the IDT77V500 Switch Controller**
- **Utilizes in-stream (in-band) signalling technique via the cell stream into the Switching Memory**
- **Can generate control cells to be sent back to the external workstation**
- **Executes three types of commands:**
  - *Writing data to Switch Controller*
  - *Reading data from Switch Controller*
  - *Reset operations*
- **Single +3.3V ± 0.3V power supply**
- **Industrial Temperature (-40°C to 85°C) is available.**

Description

The IDT77V550 Switch Manager is a device developed to provide a simple method of communication between an external workstation/ processor and the IDT77V500 Switch Controller. An In-Band signalling technique is utilized to examine incoming ATM cells, determining if the cell is a Command Cell for the Switch Controller, and loads the command if appropriate. In the typical configuration (Figure 1), the IDT77V550 is located on the IDT77V400 port to receive both signalling cells and standard traffic cells. The Switch Manager does not have to be connected to a Switching Memory port if it is only receiving the signalling cells.

The Switch Manager has two cell streams which flow in opposite directions, and can both interpret an incoming cell and generate control cells as necessary. Figure 2 illustrates the basic block configuration of the Switch Manager. The Data Path Interface (DPI) is used on both the cell input and output ports of the IDT77V550. DPI is utilized on the IDT77V400 to provide both reduced pin count per port and to offer configuration flexibility.

The IDT77V550 is capable of executing four basic types of commands in the system:

- Writing data to the Switch Controller
- Reading data from the Switch Controller
- Resetting the switch components
- Reading Switch Manager version information

When writing information to the Switch Controller, the IDT77V550 will store information needed to execute the command (up to 32 bytes) in internal memory and perform the command across the Switch Controller Manager bus. Likewise, for a read operation the information is received from the Switch Controller, stored internally by the IDT77V550, and then

Block Diagram

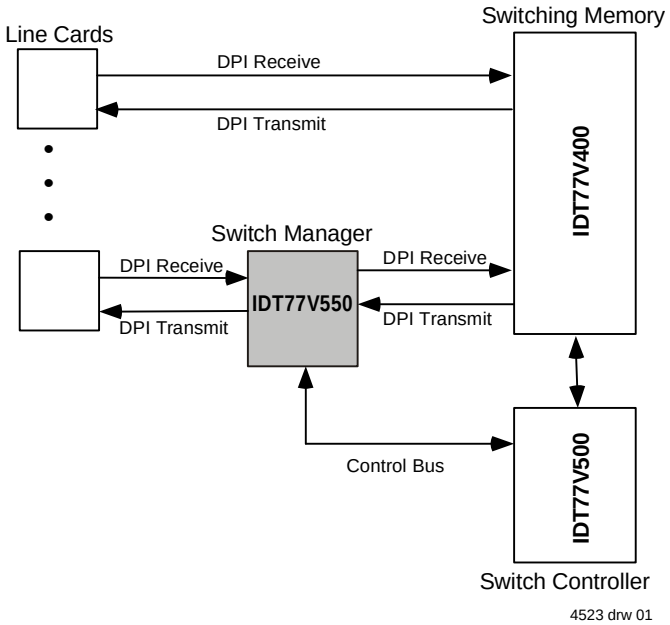


Figure 1 IDT77V550 Application with IDT77V400 Switching Memory and IDT77V500 Switch Controller

transmitted to the external workstation via a generated cell. Please refer to the data sheet of the IDT77V500 Switch Controller and the SwitchStar User Manual for additional information on these commands.

Additional information on DPI is available in Technical Note 34 on the IDT Web Site at:
http://www.idt.com/products/pages/ATM-PL114_Sub227_Dev285.html.

The switch command cell enters the Switch Manager at the Port DPI input interface, and they are interpreted in the cell receiver. If the received cell VPI/VCI address matches the VPI/VCI expected for a command cell the Switch Manager begins executing the command. The switch command cell is filtered out by the Switch Manager.

For a write data switch command to the Switch Controller, the internal cell receiver of the IDT77V550 stores up to 32 data bytes to internal memory. Then the IDT77V550 writes the data to the IDT77V500 Switch Controller using the eight bit Manager bus interface. Finally the Switch Manager will write the switch control instruction to the instruction register in the Switch Controller.

For a read data switch command to the Switch Controller, the Switch Manager reads the appropriate number of the bytes and stores them internally. The data is returned to the external control source on the lower cell stream of the port (see Figure 2). The cell generator will look for a space in the cell stream before stopping the DPI read clock and inserting the Switch Manager generated cell.

The switch manager can only process one command cell at a time. Each command cell received by the switch manager must be processed prior to receiving another command cell.

Once the IDT77V550 is finished processing the command cell, it will drive the Manager Bus based on the command received. It is necessary to wait for an acknowledgment from the IDT77V500 Switch Controller that the command sent by the IDT77V550 has been received and processed by the IDT77V500. Acknowledgment means the IDT77V500 sets MDATA 7 high after a command has been executed. The IDT77V550 can not receive or process another command cell until it receives this acknowledgment from the IDT77V500.

Revision History

February 15, 1999: Initial publication.

September 2, 1999: Added line to paragraph in DPI Receive Path. Changed name of table to Command Field format and added information and note. Changed waveforms to include SCLK.

February 4, 2000: Changed pin in Pin Configuration diagram. Changed pin definitions in Pin definitions table. Changed data in several tables. Made changes to Table 23, AC Electrical Characteristics. Made changes to Order Information section.

March 24, 2000: Made changes to last paragraph in Device Operations section. Made changes in last row of Table 23, AC Electrical Characteristics. Edited timing waveforms and added new waveform.

July 28, 2000: Added paragraph to Device Operation section. Added information in Switch Manager Commands section. Deleted tRESTED row in Table 23. Deleted Command Cell Execution Delay Timing Waveform.

November 2, 2000: Updated QFP80 Package and made several minor edits.

March 26, 2001: Corrected package dimensions (Note 3 for Figure 3) to read 12 mm x 12 mm x 1.4 mm.

June 22, 2001: Added a Note 6 to Figure 9 and another Note 6 to Figure 10. Removed “All resets will be asserted by the Switch Manager for at least 1.5us” from Reset Operations section.

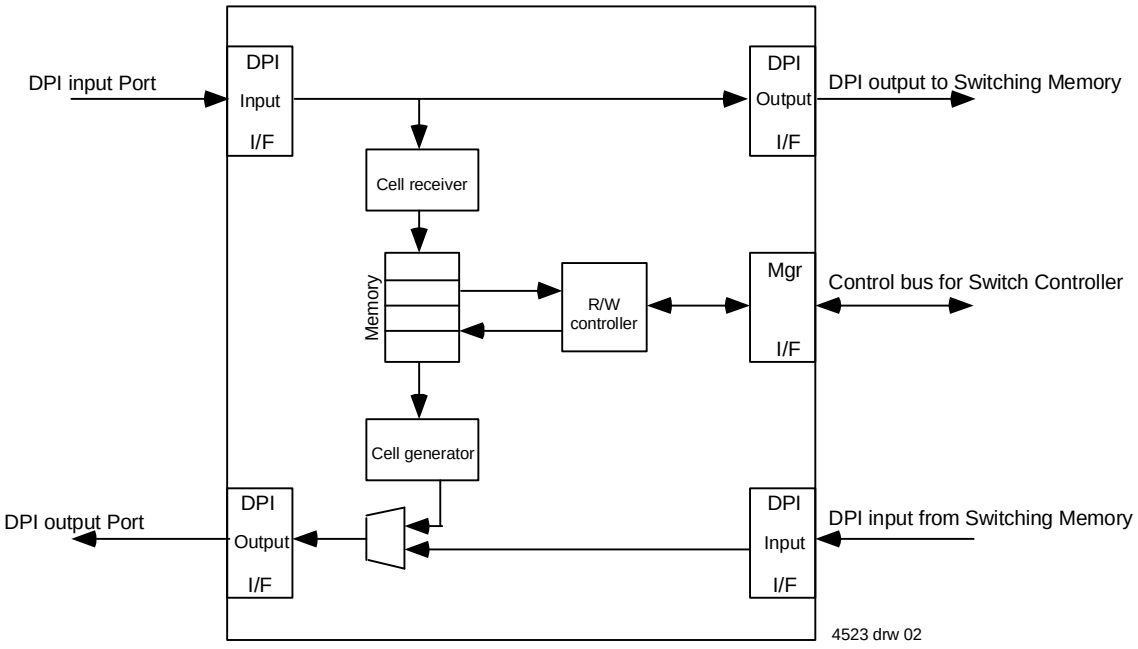


Figure 2 Basic Block Configuration of the Switch Manager

Pin Configurations

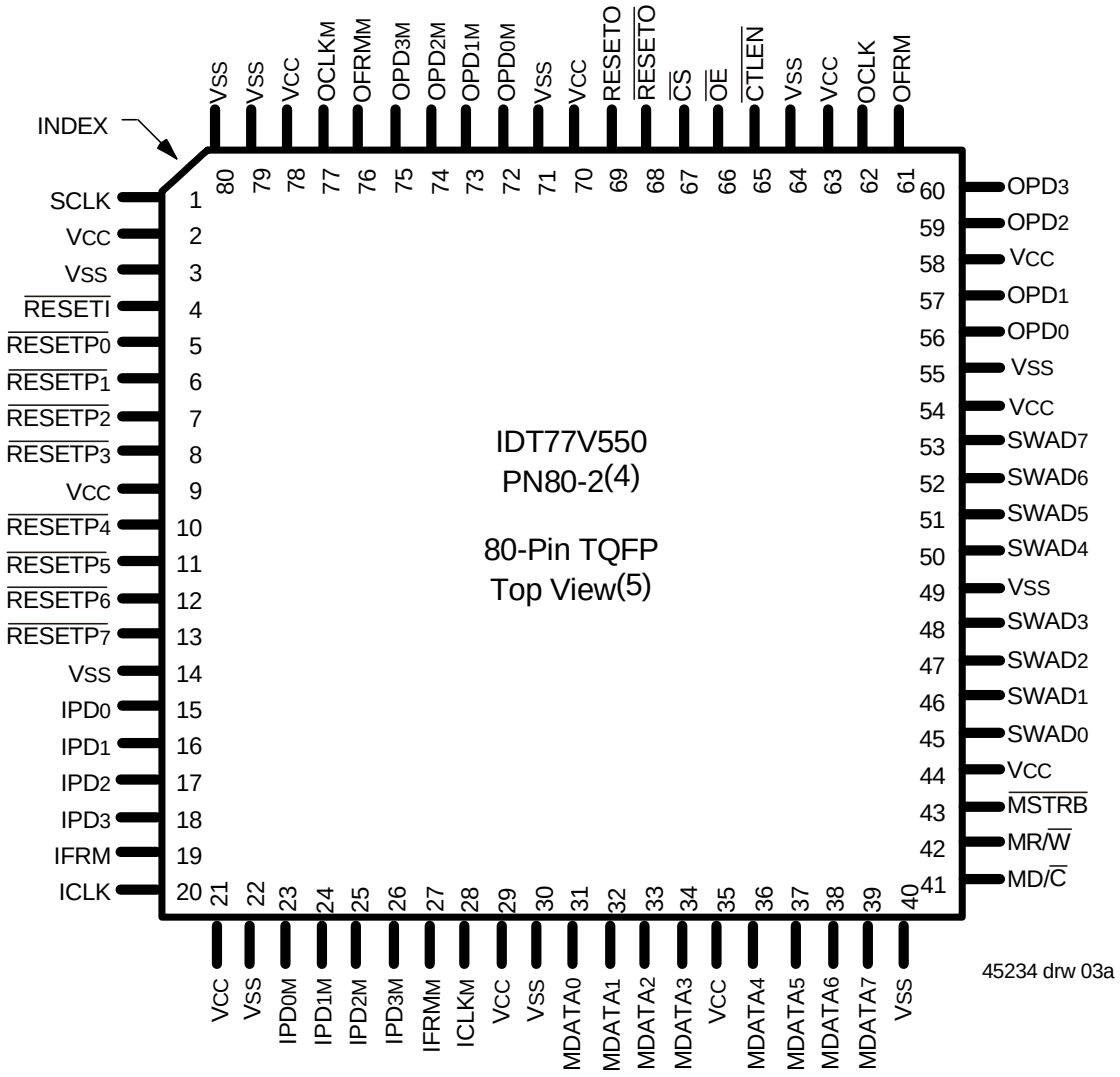


Figure 3 Pin Configuration

Note: 1.All VCC pins must be connected to power supply.
2.All VSS pins must be connected to ground supply.
3.Package body is approximately 12 mm x 12 mm x 1.4 mm.
4.This package code is used to reference the package diagram.
5.This text does not indicate orientation of the actual part marking.
6.OCLK pin 83 is associated with OFRM pin 61 (to external control); OCLKM pin 62 is associated with pin 82 (from Switching Memory).
7.NC represents No Connection; these pins should not be connected to either VCC or VSS.

Pin Definitions

Pin Number	Symbol	Type	Description
1	SCLK	Input	40 MHz system clock.
4	$\overline{\text{RESETI}}$	Input	Reset input. Active low.
68	$\overline{\text{RESETO}}$	Output	Reset output. Active low.
69	RESETO	Output	Reset output. Active high.
5	$\overline{\text{RESETP0}}$	Output	Reset output to port number 0. Active low.
6	$\overline{\text{RESETP1}}$	Output	Reset output to port number 1. Active low.
7	$\overline{\text{RESETP2}}$	Output	Reset output to port number 2. Active low.
8	$\overline{\text{RESETP3}}$	Output	Reset output to port number 3. Active low.
10	$\overline{\text{RESETP4}}$	Output	Reset output to port number 4. Active low.
11	$\overline{\text{RESETP5}}$	Output	Reset output to port number 5. Active low.
12	$\overline{\text{RESETP6}}$	Output	Reset output to port number 6. Active low.
13	$\overline{\text{RESETP7}}$	Output	Reset output to port number 7. Active low.
45	SWAD0	Input	Switch VCI address. LSB.
46	SWAD1	Input	Switch VCI address.
47	SWAD2	Input	Switch VCI address.
48	SWAD3	Input	Switch VCI address.
50	SWAD4	Input	Switch VCI address.
51	SWAD5	Input	Switch VCI address.
52	SWAD6	Input	Switch VCI address.
53	SWAD7	Input	Switch VCI address. MSB.
41	MD/$\overline{\text{C}}$	Output	Control bus. Selector for accessing data or control word.
42	MR/$\overline{\text{W}}$	Output	Control bus. Selector for read or write operation.
43	$\overline{\text{MSTRB}}$	Output	Control bus. Master strobe. Latching on positive edge.
31	MDATA0	I/O	Control bus. Data bus to Switch Controller. LSB.
32	MDATA1	I/O	Control bus. Data bus to Switch Controller.
33	MDATA2	I/O	Control bus. Data bus to Switch Controller.
34	MDATA3	I/O	Control bus. Data bus to Switch Controller.
36	MDATA4	I/O	Control bus. Data bus to Switch Controller.
37	MDATA5	I/O	Control bus. Data bus to Switch Controller.
38	MDATA6	I/O	Control bus. Data bus to Switch Controller.
39	MDATA7	I/O	Control bus. Data bus to Switch Controller. MSB.
15	IPD0	Input	DPI to Switch Manager interface. Data bus.
16	IPD1	Input	DPI to Switch Manager interface. Data bus.
17	IPD2	Input	DPI to Switch Manager interface. Data bus.
18	IPD3	Input	DPI to Switch Manager interface. Data bus.
19	IFRM	Input	Linecard to Switch Manager DPI interface. New frame.

Table 1 Pin Descriptions (Part 1 of 2)

Pin Number	Symbol	Type	Description
20	ICLK	Input	Linecard to Switch Manager DPI interface. Data clock connect.
23	IPD0M	Output	Switch Manager to Switching Memory DPI interface. Data bus.
24	IPD1M	Output	Switch Manager to Switching Memory DPI interface. Data bus.
25	IPD2M	Output	Switch Manager to Switching Memory DPI interface. Data bus.
26	IPD3M	Output	Switch Manager to Switching Memory DPI interface. Data bus.
27	IFRMM	Output	Switch Manager to Switching Memory DPI interface. New frame.
28	ICLKM	Output	Switch Manager to Switching Memory DPI interface. Data clock.
56	OPD0	Output	Switch Manager to DPI interface. Data bus.
57	OPD1	Output	Switch Manager to DPI interface. Data bus.
59	OPD2	Output	Switch Manager to DPI interface. Data bus.
60	OPD3	Output	Switch Manager to DPI interface. Data bus.
61	OFRM	Output	Switch Manager to DPI interface. New frame.
62	OCLK	Input	Switch Manager to DPI interface. Data clock.
72	OPD0M	Input	Switching Memory to Switch Manager DPI interface. Data bus.
73	OPD1M	Input	Switching Memory to Switch Manager DPI interface. Data bus.
74	OPD2M	Input	Switching Memory to Switch Manager DPI interface. Data bus.
75	OPD3M	Input	Switching Memory to Switch Manager DPI interface. Data bus.
76	OFRMM	Input	Switching Memory to Switch Manager DPI interface. New frame.
77	OCLKM	Output	Switching Memory to Switch Manager DPI interface. Data clock.
67	$\overline{CS}$	Output	Chip select for 77V400 Switching Memory.
66	$\overline{OE}$	Output	Output enable for 77V400 Switching Memory.
65	$\overline{CTLEN}$	Output	Control Enable for 77V400 Switching Memory.
2,9,21,29,35,44, 54,58,63,70,78	VCC	Power	3.3V Power Supply Pins.
3,14,22,30,40,49, 55,64,71,79,80	VSS	GND	Ground Pins

Table 1 Pin Descriptions (Part 2 of 2)

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +3.9	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	20	mA

Table 2 Ratings

Note: 1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.VTERM must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to < 20mA for the period of VTERM > Vcc + 0.3V.

Maximum Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

Table 3 Maximum Operating Temperature and Supply Voltage

Note: 1.This is the parameter T_A.
2.Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operations Conditions[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0		V_{CC}+0.3V[2]	V
V_{IL}	Input Low Voltage	-0.3[1]		0.8	V

Table 4 Recommended DC Operations Conditions

Note: 1.$V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2.V_{TERM} must not exceed Vcc + 0.3V.

Capacitance[1] (TA = +25°C, f = 1.0mhz) PLCC Package

Symbol	Parameter	Condition[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

Table 5 Capacitance

Note: 1.This parameter is determined by device characterization but is not production tested.
2.3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC Electrical Characteristics over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V550		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.15	—	V

Table 6 DC Electrical Characteristics over the Operating Temperature and Supply Voltage Range

Note: 1.At Vcc $\leq$ 2.0V, input leakages are undefined.

Symbol	Parameter	Test Conditions	77V550S25DLI		77V550S25DL		Unit
			Typ.	Max.	Typ.	Max.	
ICC	Operating Current	VCC = 3.6V, IOUT = 0mA, $\overline{\text{RESETI}}$= VIH, f = fmax(1)	100	180	100	160	mA

Table 7 DC Electrical Characteristics over the Operating Temperature and Supply Voltage Range

Note: 1.At f = fmax SCLK, ICLK, and OCLK are cycling at their maximum frequency and all inputs are cycling at 1/tCYC1, using AC input levels of VSS to 3.0V.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 4 and 5

Table 8 AC Test Conditions

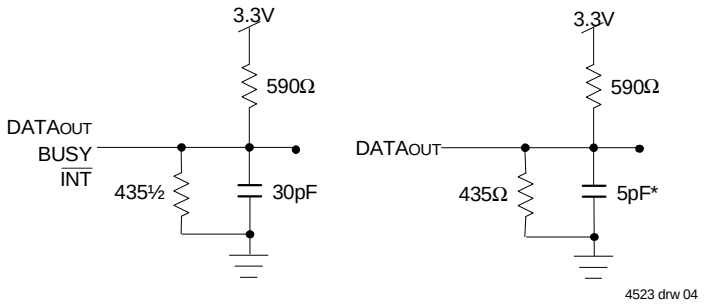


Figure 4 AC Output Test Load (left side) and Output Test Load (for tLZ, tHZ, twz, tow) *Including scop and jig (right side)

DPI Interface

The Data Path Interface (DPI) is a synchronous bus interface designed to transfer ATM cells between two devices. The IDT77V550 DPI interface supports a 4-bit wide data bus (DPI-4), with separate transmit and receive interfaces. All signals are sampled on the rising edge of their respective clock.

DPI Receive Path

The DPI Receive Path is used to transfer cells through the IDT77V550 Switch Manager to the IDT77V400 Switching Memory or other DPI device. It has 4-bit Data Buses (IPD[3:0] and IPDM[3:0]) and follows the standard DPI timing characteristics as described in the DPI specification (IDT Technical Note TN-34). Other signals associated with this interface are DPI Receive Start of Frame (IFRM and IFRMM) and DPI Receive Clock (ICLK and ICLKM).

ICLK is an input to the IDT77V500, and ICLKM to the IDT77V400 (an Output) is generated from ICLK.

IFRM/IFRMM is the start of frame marker. This signal is one ICLK/ICLKM cycle long and is asserted HIGH one ICLK/ICLKM cycle before the first nibble of valid data.

Figure 5 and Figure 6 illustrate these timing relationships for a single cell transfer and a Back-to-Back cell transfer on the receive DPI bus.

DPI Transmit Path

The DPI Transmit Path is used to transfer cells from the IDT77V400 Switching Memory or other DPI device to and through the IDT77V550 Switch Manager. It has 4-bit input data buses (OPD[3:0] and OPDM[3:0]) and follows the standard DPI timing characteristics as described in the DPI specification. Other signals associated with this interface are DPI Transmit Start of Frame (OFRM and OFRMM), and DPI Transmit Clock (OCLK and OCLKM).

OCLK is an input to the Switch Manager, and OCLKM to the IDT77V400 Switching Memory (an output) is generated from OCLK.

OFRM/OFRMM is the start of frame marker. This signal is one OCLK/OCLKM cycle long and is asserted high one OCLK/OCLKM cycle before the first valid nibble of data.

Figure 7 and Figure 8 illustrate these timing relationships for a signal cell transfer and a Back-to-Back cell transfer on the transmit DPI bus.

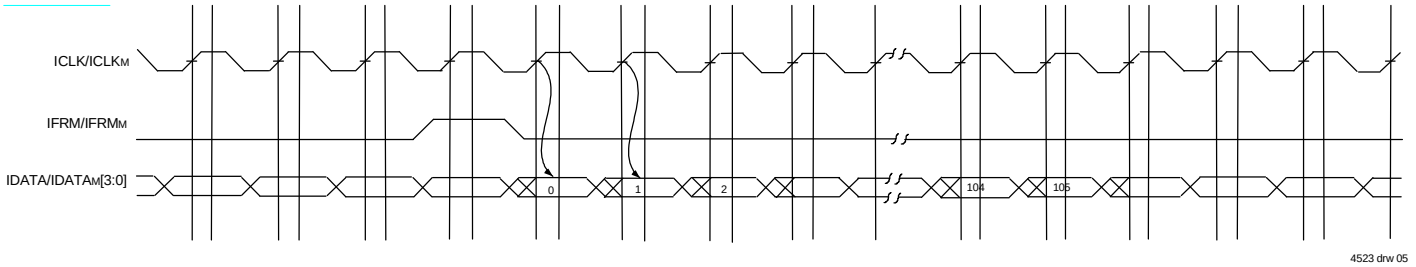


Figure 5 One Cell Transfer on Receive DPI Bus

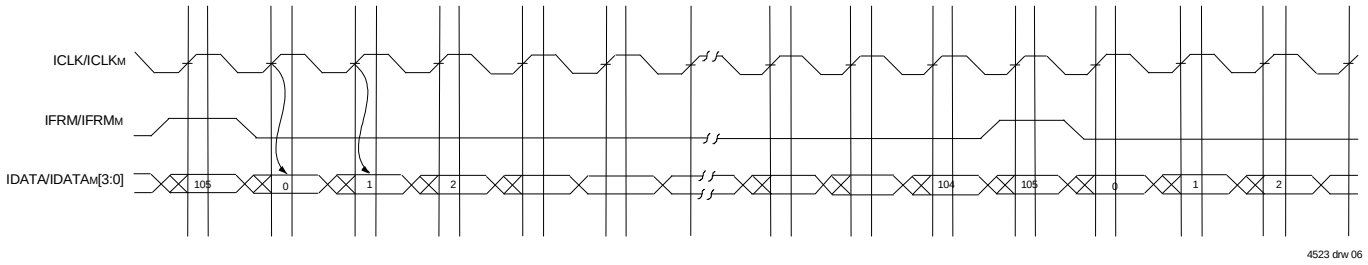


Figure 6 Back-to-Back Cell Transfer on Receive DPI Bus

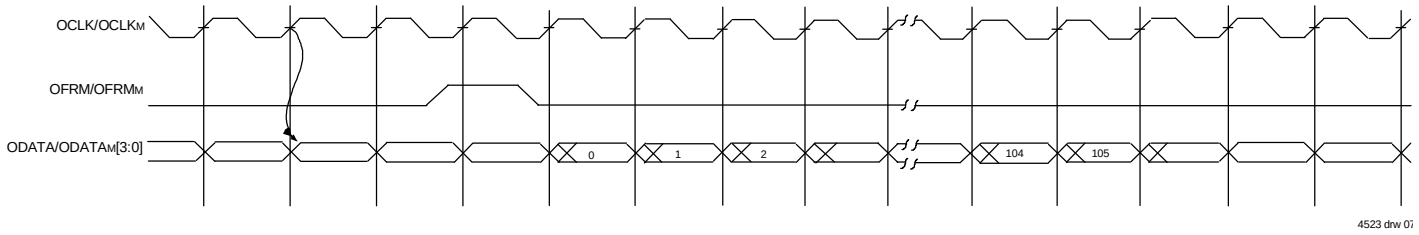


Figure 7 One Cell Transfer on Transmit DPI Bus

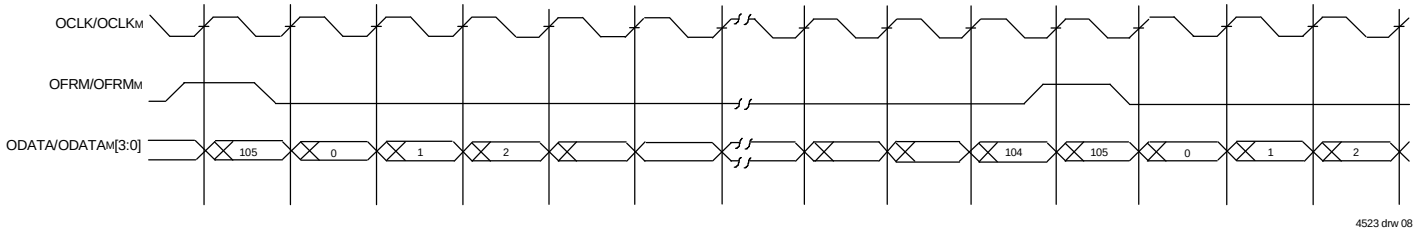


Figure 8 Back-to-Back Cell Transfer on Transmit DPI Bus

Generic ATM Cell to DPI-4 Mapping

DPI Nibble Count	DPI Content	Comments
0	GFC [3:0]	GFC bits for the ATM cell header. First nibble to be transmitted/received.
1	VPI [7:4]	VPI bits MSB of the ATM cell header.
2	VPI [3:0]	VPI bits LSB of the ATM cell header.
3	VCI [15:12]	VCI bits MSB of the ATM cell header.
4	VCI [11:8]	VCI bits of the ATM cell header.
5	VCI [7:4]	VCI bits of the ATM cell header.
6	VCI [3:0]	VCI bits of the ATM cell header.
7	PTI [2:0], CLP	PTI and CLP bits of the ATM cell header.
8	HEC [7:4]	HEC Most Significant nibble.
9	HEC [3:0]	HEC Least Significant nibble.
10	First data byte [7:4]	First data Most Significant nibble of the ATM cell header.
11	First data byte [3:0]	First data Least Significant nibble of the ATM cell header.
—	—	—
—	—	—
104	Last data byte [7:4]	Last data byte Most Significant nibble of the ATM cell.
105	Last data byte [3:0]	Last data byte Least Significant nibble of the ATM cell.

Table 9 Generic ATM Cell to DPI-4 Mapping

Manager Bus Interface

The IDT77V550 Switch Manager communicates with the IDT77V500 Switch Controller over the 8-bit Manager bus. An exchange between the Switch Manager and the Switch Controller has been defined to require at most four steps (this is a Read Operation):

1. Load the data registers of the IDT77V500. (Address to be read in READ Mode; Data to be written in WRITE Mode.)
2. Write a command to the command register of the IDT77V500.
3. Read the status register of the IDT77V500 until an acknowledgment occurs.
4. Read the requested data registers of the IDT77V500.

The Acknowledgment function, in which the IDT77V500 sets MDATA7 HIGH after a command has been executed, is a necessary procedure to guarantee that Manager Bus Commands have been completely executed. This is due to the inherent internal activity priority for the State Machine of the IDT77V500.

Since the Manager Bus Commands are the lowest priority in the Switch Controller State Machine, there could be some delays if the actual switch traffic was heavy at a particular time. The manager must wait for an acknowledgment from the IDT77V500 before moving on to execute the next command. Acknowledgment is defined as a HIGH MDATA7 read (MD/$\overline{C}$ LOW and MR/$\overline{W}$ HIGH) after loading of the Command (MD/$\overline{C}$ LOW and MR/$\overline{W}$ LOW). It is not necessary to execute a STATUS command to read this Acknowledgment form the Switch Controller. The timing delay from when the IDT77V550 receives the command cell and when the IDT77V500 acknowledges that the command has been executed can vary greatly. The delay can be as long as 14 µsec during periods of sustained heavy data traffic through the switch, especially when the state machine of the IDT77V500 is unable to perform the acknowledgment function.

Which of the four steps required and the meaning of the bits in the data registers depends on the particular command. For example configuring the IDT77V500 requires the data registers to be loaded while examining status reads them. The command executed will also determine how many of the thirteen Data Registers must be written into or read from to complete the operation. Three control signals, MR/$\overline{W}$, MD/$\overline{C}$, and $\overline{MSTRB}$, are used to access the Switch Controller. MR/W is HIGH to read the controller; LOW to write it. MD/C is LOW to select the command/status register (to issue a command) and HIGH for the data registers (to Read/Write data into the Controller). During a read operation $\overline{MSTRB}$ LOW enables the controller to drive MDATA, effectively acting like an Output Enable pin. On a write command the rising edge of $\overline{MSTRB}$ clocks MDATA into the IDT77V500. The

Manager writes and reads the data registers one at a time. On the first write or read register zero is chosen. With each subsequent write or read cycle successively higher numbered registers are selected. Figure 9 gives a typical Read sequence across the manager bus; Figure 10 illustrates a Write operation. Note the need for the acknowledgment before proceeding.

For the IDT77V500 commands available, refer to the IDT77V500 Switch Controller Manager Bus Command Table. Additional command details are available in the SwitchStar User's Manual, Section 3.

Manager Bus Read Timing Waveform(1)

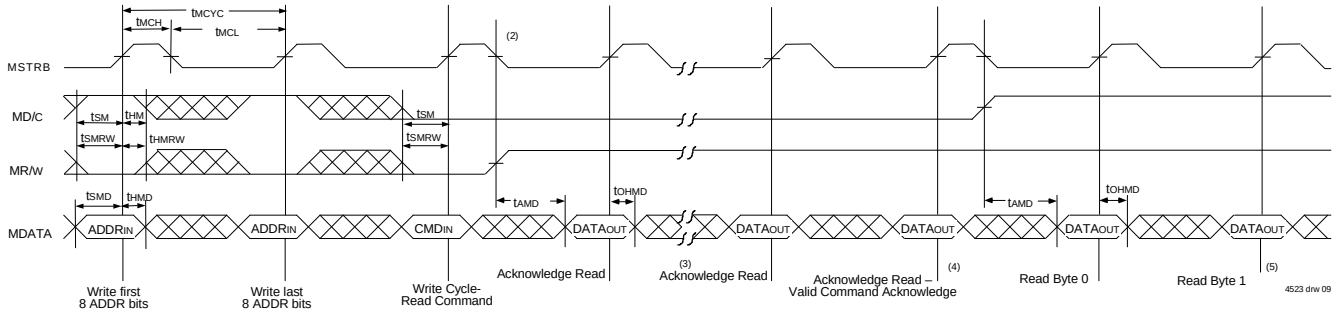


Figure 9 Manager Bus Read Timing Waveform

Note: 1. Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{\text{MSTRB}}$. The data placed on the MDATA pins is determined by the state of the MD/C pin.
2. The combination of $\overline{\text{MSTRB}}$ Low and MR/$\overline{\text{W}}$ High (Read mode) asynchronously enables the MDATA pins as outputs. That is, data is available to be read one asynchronous tAMD time after the falling edge of $\overline{\text{MSTRB}}$ if MR/$\overline{\text{W}}$ is HIGH.
3. After the Command is written, the Manager must take MR/$\overline{\text{W}}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.
4. A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).
5. Waveform illustrates first two bytes of data only. Additional bytes may be available based on command used.
6.The tHMRW delay time is guaranteed by design to be two SCLK cycles in duration. The tHM delay time is guaranteed by design to be between two and four clocks in duration.

Manager Bus Write Timing Waveform(1)

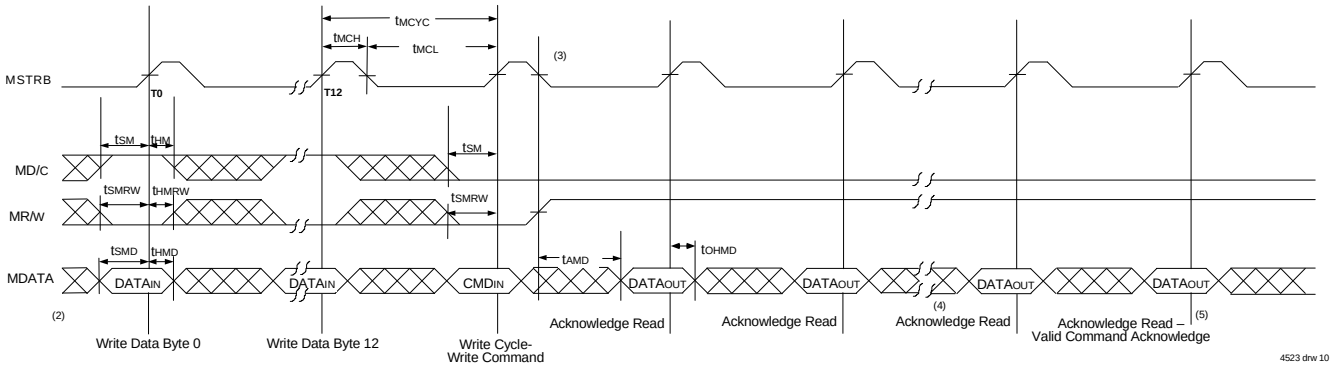


Figure 10 Manager Bus Write Timing Waveform

Note: 1. Write operations, both for Commands and Data, are synchronous to the rising edge of $\overline{\text{MSTRB}}$. The data placed on the MDATA pins is determined by the state of the MD/C pin.
2. Either a Read cycle was completed or a Status Acknowledge was executed immediately prior to the first $\overline{\text{MSTRB}}$ of this write waveform.
3. The combination of $\overline{\text{MSTRB}}$ Low and MR/$\overline{\text{W}}$ High (Read mode) asynchronously enables the MDATA pins as outputs. The data placed on the MDATA pins is determined by the state of the MD/C pin.
4. After the Command is written, the Manager must take MR/$\overline{\text{W}}$ High (Read mode) to wait for a valid Command Acknowledge from the IDT77V500 before proceeding. Reading a High Bit 7 of the status register under these conditions indicates the command has been acknowledged by the IDT77V500. This may take multiple IDT77V500 SCLK cycles based on possible higher priority operations that the IDT77V500 must support.
5. A valid Acknowledge from the IDT77V500 is indicated by a High Command Acknowledge bit (Bit 7 of the Status Register).
6.The tHMRW and tHMD delay times are guaranteed by design to be two SCLK cycles in duration. The tHM delay time is guaranteed by design to be between two and four clocks in duration.

IDT77V500 Switch Controller Manager Bus Commands(1)

Command	Command Description	Code (In Hex)
WRV	Write Per VC Table	01
RDV	Read Per VC Table	02
WRSL	Write Service Link Memory	03
RDSL	Read Service Link Memory	04
WRL	Write Cell Link Memory	05
RDL	Read Cell Link Memory	06
STAT	Read IDT77V500 status	07
LDCFG	Load IDT77V400 configuration bits	08
SUP	Cell setup	09
INIT	Initialize IDT77V500	0A
SEL	Select a IDT77V500	0B
START	End of IDT77V500 Initialization	0C
CBR	Set up a CBR Scheduler	0D
PARM	Set Parameters of the IDT77V500	0E

Table 10 IDT77V500 Switch Controller Manager Bus Commands

Note: 1.This table is provided as a reference of the available IDT77V500 Switch Controller commands. Additional information, including command parameters and register definition, is available in the SwitchStar User's Manual, Section 3.

ATM Cell Format

The Switch Manager can either interpret a cell received on port number 7 or generate a cell to send back to the external control logic. The format of Receive Control Cells and Transmit Control Cells is shows in the Tables below.

At power up the VPI/VCI address of a signaling cell will be set to VPI = 0x00, VCI[5:8] = 0x00, and VCI[7:0] is by pins SWAD0-7. By using the change VCI address command it's possible to change the VCI[7:0] while VPI and VCI[15:8] is static 0x00, providing a total of 256 different addresses to chose from. The same address is always used to both receive and transmit cells in the Switch Manager.

The Command number field is returned in an acknowledge cell. This field can have an unique value for each consecutive command send by the controlling host, and thus can be used to make a sliding window mechanism for the command cells.

The VPI/VCI address of a transmitted cell will at power up be VPI = 0x00, VCI[15:8] = 0x00 and VCI[7:0] determined by pins SWAD0-7. The VCI[7:0] can be changed by using the Change Switch Address command. The address of received and transmitted cells will always be the same.

The HEC field will be generated by the PHY.

IDT77V500 Switch Controller Manager Bus Commands(1)

Byte	Bits	Field Name	Value	Function
0	7-4	GFC	0xX	Ignored by Switch Manager
0-1	3-0; 7-4	VPI	0x00	Must be set to 0x00
1-2	3-0; 7-4	VCI 15-8	0x00	Must be set to 0x00
2-3	3-0; 7-4	VCI 7-0	0x00-0xFF	Set by SWAD0-7 or programmed in register

Table 11 IDT77V500 Switch Controller Manager Bus Commands (Part 1 of 2)

Byte	Bits	Field Name	Value	Function
3	3-0	PTI, CLP	0xX	Ignored by Switch Manager
4	7-0	HEC	0xXX	Ignored by Switch Manager
5	7-0	Command		Command the Switch Manager to perform an action
6	7-0	Switch Controller command	(1)	The command written to the Switch Controller
7	7-0	Cell number	0x00-0xFF	A unique cell number, used in sliding window applications.
8	7-0	Data count	0x0-0x12	Number of data bytes to be in payload
9-21	7-0	Data0 - Data12		Data bytes in payload, written to Switching Memory

Table 11 IDT77V500 Switch Controller Manager Bus Commands (Part 2 of 2)

Note: 1. See "IDT77V500 Switch Controller Manager Bus Commands" table for available commands.

Transmit Cell Format

Byte	Bits	Field Name	Value	Function
0	7-4	GFC	0x0	Set to default value 0x0
0-1	3-0; 7-4	VPI	0x00	VPI address, set to 0x00
1-2	3-0; 7-4	VCI 15-8	0x00	VCI address MSB, set to 0x00
2-3	3-0; 7-4	VCI 7-0	0x00-0xFF	VCI address, $SWAD_{0-7}$ or programmed in register
3	3-0	PTI, CLP	0x0	Set to default value 0x0
4	7-0	HEC	0x00	Calculated by PHY device
5	7-0	Command		Copy of command from received cell that initiated this cell
6	7-0	Sub Command		Sub command send to Switch Controller
7	7-0	Cell number	0x00-0xFF	A unique cell number, used in sliding window apps.
7	7-0	Data count	0x0-0x12	Number of bytes carried in the data payload area
8-20	7-0	Data0 - Data12		Data payload area, Max 13 bytes

Table 12 Transmit Cell Format

Switch Manager Commands

This section describes the format for Switch Manager commands. In this document there is a difference between instructions and commands. Instructions are passed on to the Switch Controller, while commands are interpreted by the Switch Manager.

Some of the commands will return a cell to the controlling workstation. These cells will have the same values in their fields as the initiating cell except for the data field. For example, a read command cell will return with the contents of the registers of the IDT77V500 in the data field.

In the following commands there will be encoded two bits in the upper nibble of the command field. The table below defines the two bits (6 and 7).

By setting bit 7 of the command field, the Switch Manager will return an acknowledge cell, signalling the proper execution of a command.

When reading the Switch Manager's status register before doing a read or write, make sure that the Switch Controller is actually read to receive a new command. If bit 7 of the status register is not set HIGH the Switch Manager will continue to poll until it has been set, and then do the read/write command. Bit 6 of the Command Field is only valid for a read or write commands.

Command Field Format

Bit Number	Description
7	Return an acknowledge cell signaling the execution of the current command.
6	Read the switch managers status register before doing a read or write.
5	Don't care.
4	Don't care.
3	Don't care.
2	MSB of command bit pattern.
1	Bit of command bit pattern.
0	LSB of command bit pattern.

Table 13

Note: The command bit pattern is defined in the command field of Format Tables on pages 15-17.

Null Command

When transmitted to the Switch Manager this command generates a null cell. When a null command cell is received from a Switch Manager the managing workstation should look in the sub command field to see why this cell has been sent.

There are two possible situations when a null cell will be received by the Switch Manager:

1. This is a returned cell from a null command (no execution performed).
2. The switch has been manually reset or power cycled (all information in the switch has been lost) and a null cell was returned.

Null Command Format

Field	Value	Description
Command	0x00	Null command used in Transmit Cell Format bits 0-2.
Sub Command	0x00-0x01	Meaning on receiving cell at workstation: 0x00 Returning null cell command 0x01 Switch has been reset Should be 0x00 when transmitted to Switch Manager.
Data Count	0xXX	Don't care.
DataCount 0-17	0xXX	Don't care.

Table 14 Null Command Format

Read Data Command

This command reads data from the Switch Controller. If bit 6 in the command field is set, the Switch Manager will first make sure the Controller is ready by reading the status register before reading data.

The content fields (Data0-17) of a returned read command cell are only valid for the number of data bytes which is in the Data count field. The rest of the data bytes may contain random data (not zero).

Read Data Command Format

Field	Value	Description
Command	0x01	Read data from Switch Controller and send it back to external control logic.
Sub Command	0xXX	Don't care.
Data Count	0x00-0x12	Number of data registers to read from Switch Controller.
Data0 - 17	0xXX	On return cell these fields will hold the read data.

Table 15 Read Data Command Format

Write Data Command

This command writes data to the Switch Controller. If bit 6 in the command field is set, the Switch Manager will first make sure the controller is ready by reading the status register before writing data. After writing the data the sub command field will be written to the Switch Controller instruction register.

Finally if bit 7 in the command field is set the Switch Manager will return an acknowledge cell. The data content fields (Data0-17) of a returned cell are not valid data. That is, it will contain the same data as was put in the write command cell, and it may contain random data (not zero).

Write Data Command Format

Field	Value	Description
Command	0x02	Write data to Switch Controller.
Sub Command		Sub command is written to the Switch Controller instruction register as the last byte written.
Data Count		Number of data registers to write to Switch Controller.
Data0 - 17		Data to write to Switch Controller.

Table 16 Write Data Command Format

Reset Switch Controller

The Switch Manager generation a reset signal which is connected to the Controller Switch. This command forces a reset of the Switch Controller only.

Reset Switch Controller Command Format

Field	Value	Description
Command	0x03	Reset the Switch Controller.
Sub Command	0xXX	Don't care.
Data Count	0xXX	Don't care.
Data0 - 17	0xXX	Don't care.

Table 17 Reset Switch Controller Command Format

Global Reset Command

This command is equivalent to pushing the reset button on the switch. That is, it generates reset signals for the complete switch including devices on individual ports of the switch.

Global Reset Command Format

Field	Value	Description
Command	0x04	Do a global reset.
Sub Command	0xXX	Don't care.
Data Count	0xXX	Don't care.
Data0 - 17	0xXX	Don't care.

Table 18 Global Reset Command Format

Reset Port Device Command

The Sub Command field indicates which port to reset. Each bit in the Sub Command field controls one reset line to the 8 line cards. This is an active HIGH filter meaning each bit set enables reset of the corresponding port.

Reset Port Device Command Format

Field	Value	Description
Command	0x05	Reset port number #, given in sub command field.
Sub Command	0x00-0xFF	Each bit indicates port to be reset. This is an active HIGH filter. Direction MSB = port 7, LSB = port 0.
Data Count	0xXX	Don't care.
Data0 - 17	0xXX	Don't care.

Table 19 Reset Port Device Command Format

Read Switch Manager Revision Command

The revision number is returned in the first Data byte of the ATM cell send back to the external control logic. The format for the revision number is four bits are used to report the digit before the decimal point; four bits are used for the digit after the decimal point. For example, the current revision is 2.1, represented as 0x21.

After the command is issued, the Switch Manager revision information is returned in Data0. Data1-12 do not contain valid information and should be ignored.

Read Switch Manager Revision Command Format

Field	Value	Description
Command	0x06	Read the revision number of the Switch Manager.
Sub Command	0xXX	Don't care.
Data Count	0xXX	Don't care.
Data0 - 17	0xXX	Don't care.

Table 20 Read Switch Manager Revision Command Format

Change Switch VCI Address Command

This command allows you to change the Switch VCI Address used to identify control cells that are received by the Switch Manager.

Transmit Cell Format

Field	Value	Description
Command	0x07	Change the Switch VCI address to the value in the Sub Command field.
Sub Command	0x00-0xFF	New switch VCI address.
Data Count	0xXX	Don't care.
Data0 - 17	0xXX	Don't care.

Table 21 Read Switch Manager Revision Command Format

Reset Operations

The Switch Manager controls all reset operations in the switch. It can either do a complete switch reset which includes all components, or it can do a dedicated reset of a port or Switch Controller.

There are two different ways of initiating a reset.

1. Manually resetting the switch, which will generate a complete reset of the switch.
2. Use one of the reset commands of the Switch Manager.

The table below illustrates how the different reset operations affect the Reset Outputs of the Switch Manager.

Reset Conditions Table

Reset Output Pins	Manual Switch Reset Button	Global Reset Command	Reset Switch Controller Command	Reset Port# Command
$\overline{\text{RESETO}}$	X	X		
RESET0	X	X	X	
$\overline{\text{RESETP}}$ [0..7]				X

Table 22 Reset Conditions Table

AC Electrical Characteristics over the Operating Temperature Range

(Vcc = 3.3V ± 0.3V)

Symbol	Parameter	77V550S25		Unit
		Min.	Max.	
tCYC	SCLK Cycle Time	25	—	ns
tCH	SCLK High Time	10	—	ns
tCL	SCLK Low Time	10	—	ns
tOCYC	OCLK/OCLKM DPI Clock Cycle Time	25	—	ns
tOCH	OCLK/OCLKM DPI Clock High Time	10	—	ns
tOCL	OCLK/OCLKM DPI Clock Low Time	10	—	ns
tICYC	ICLK/ICLKM DPI Clock Cycle Time	25	—	ns
tICH	ICLK/ICLKM DPI Clock High Time	10	—	ns
tICL	ICLK/ICLKM DPI Clock Low Time	10	—	ns
tSD	OFRMM, OPDM[0-3] Setup Time	9	—	ns
tH	OFRMM, OPDM[0-3] Hold Time	0	—	ns
tSD	IFRMM, IPDM[0-3] Setup Time	4.0	—	ns
tH	IFRMM, IPDM[0-3] Hold Time	0	—	ns
tCD	OFRMM, OPDM[0-3] Propagation delay to Valid Output	3	12	ns
tCD	IFRMM, IPDM[0-3] Propagation delay to Valid Output	3	11	ns
tPDICLK	ICLK to ICLKM Propagation Delay	3	13	ns
tPDOCLK	OCLK to OCLKM Propagation Delay	1	7	ns

Table 23 AC Electrical Characteristics over the Operating Temperature Range

System Clock Timing Waveform

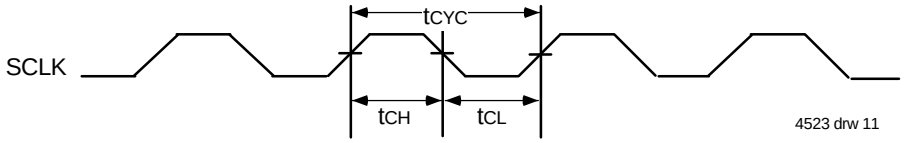


Figure 11 System Clock Timing Waveform

DPI Transmit Timing Waveform 1

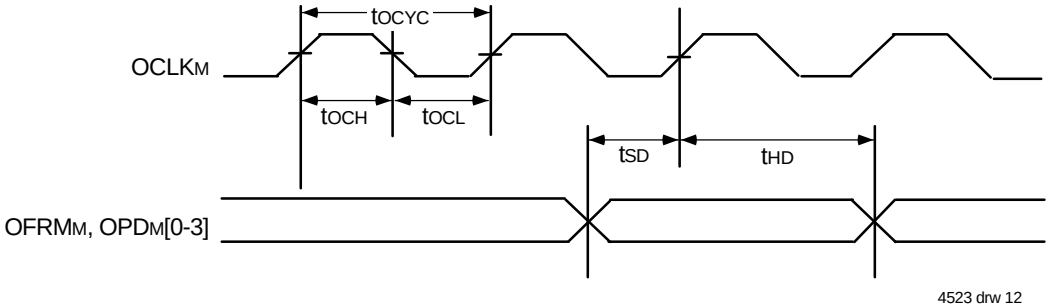


Figure 12 DPI Transmit Timing Waveform 1

DPI Transmit Timing Waveform 2

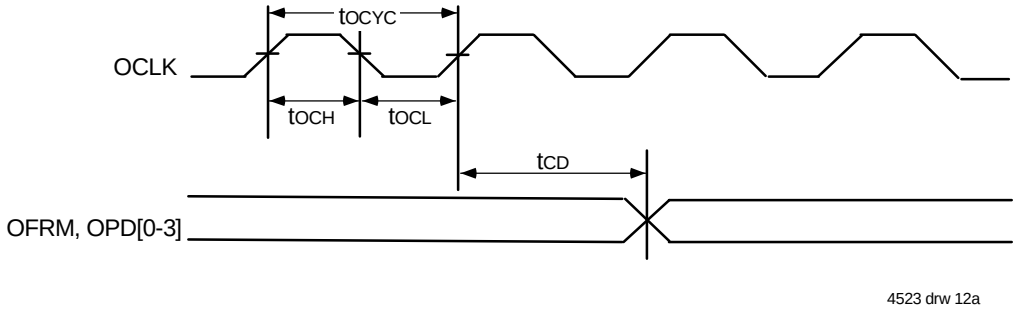


Figure 13 DPI Transmit Timing Waveform 2

DPI Receive Timing Waveform 1

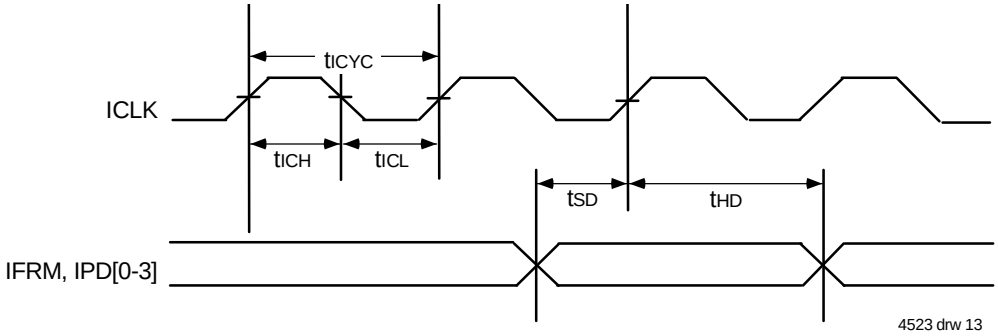


Figure 14 DPI Receive Timing Waveform 1

DPI Receive Timing Waveform 2

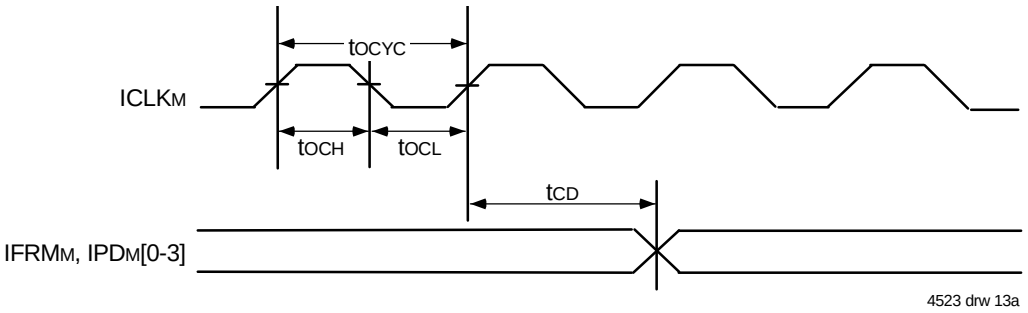


Figure 15 DPI Receive Timing Waveform 2

ICLK to ICLKM Propagation Delay Timing Waveform

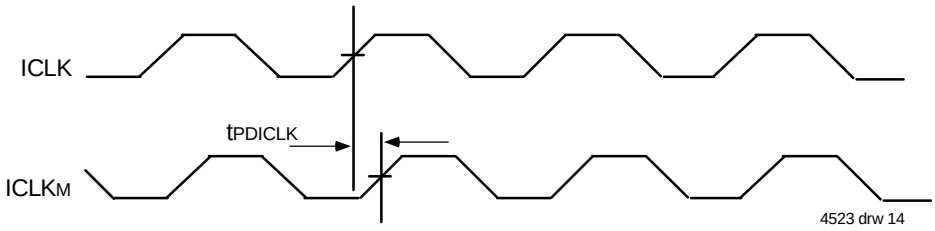


Figure 16 ICLK to ICLKM Propagation Delay Timing Waveform

OCLK to OCLKM Propagation Delay Timing Waveform

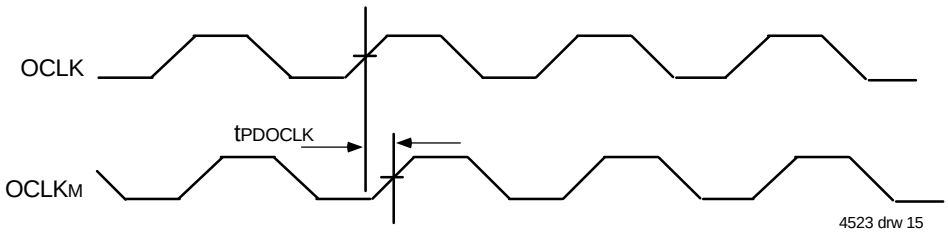
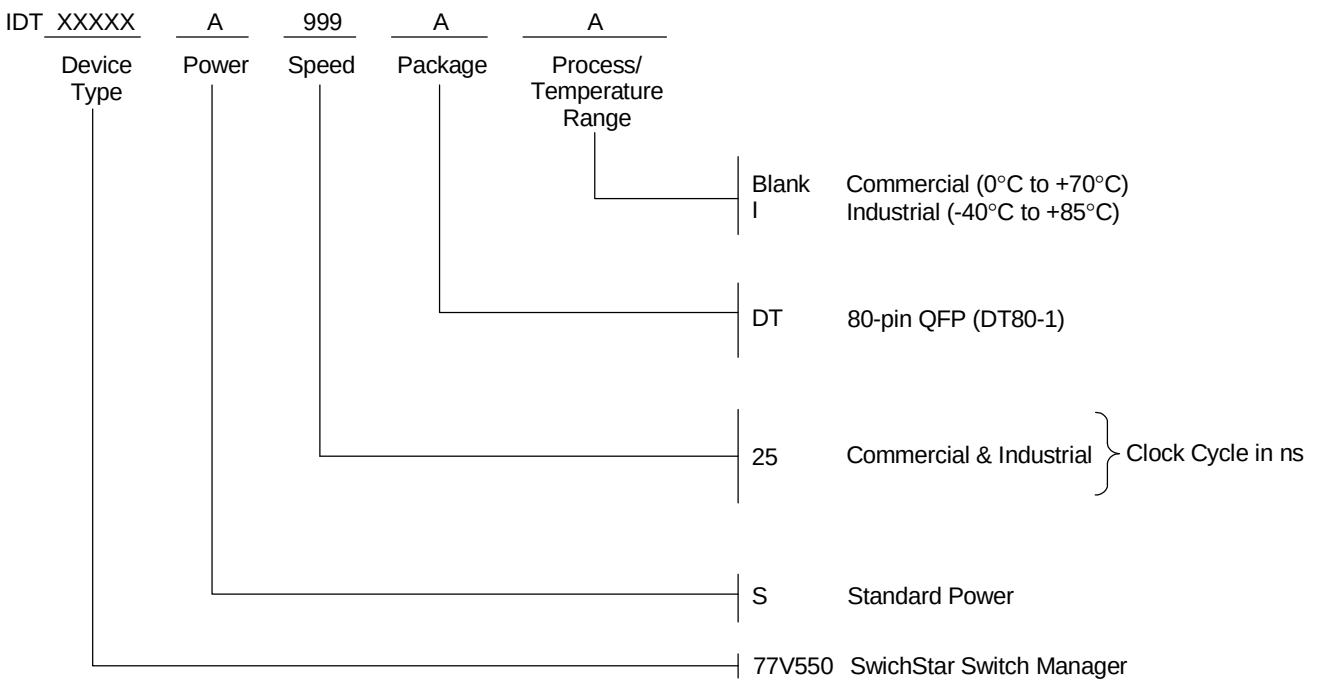


Figure 17 OCLK to OCLKM Propagation Delay Timing Waveform

Ordering Information



4523 drw 16

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