4-Lane 4-Port Gen2 PCI Express® Switch

89HPES4T4G2
Data Sheet
Advance Information*

Device Overview

The 89HPES4T4G2, a 4-lane 4-port Gen2 PCI Express® switch, is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES4T4G2 is a peripheral chip that performs PCI Express base switching with a feature set optimized for servers, storage, communications, and consumer applications. It provides connectivity and switching functions between a PCI Express upstream port and three downstream ports or peer-to-peer switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Four Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operations*
  - *Four switch ports*
    - *One x1 upstream port*
    - *Three x1 downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2Kbytes*
  - *Supports one virtual channel and eight traffic classes*
  - *PCI Express Base Specification Revision 2.0 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates four 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)*
    - *Receive equalization (RxEQ)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Support PCI Power Management Interface specification (PCI-PM 2.0)*

Advance Information

Block Diagram

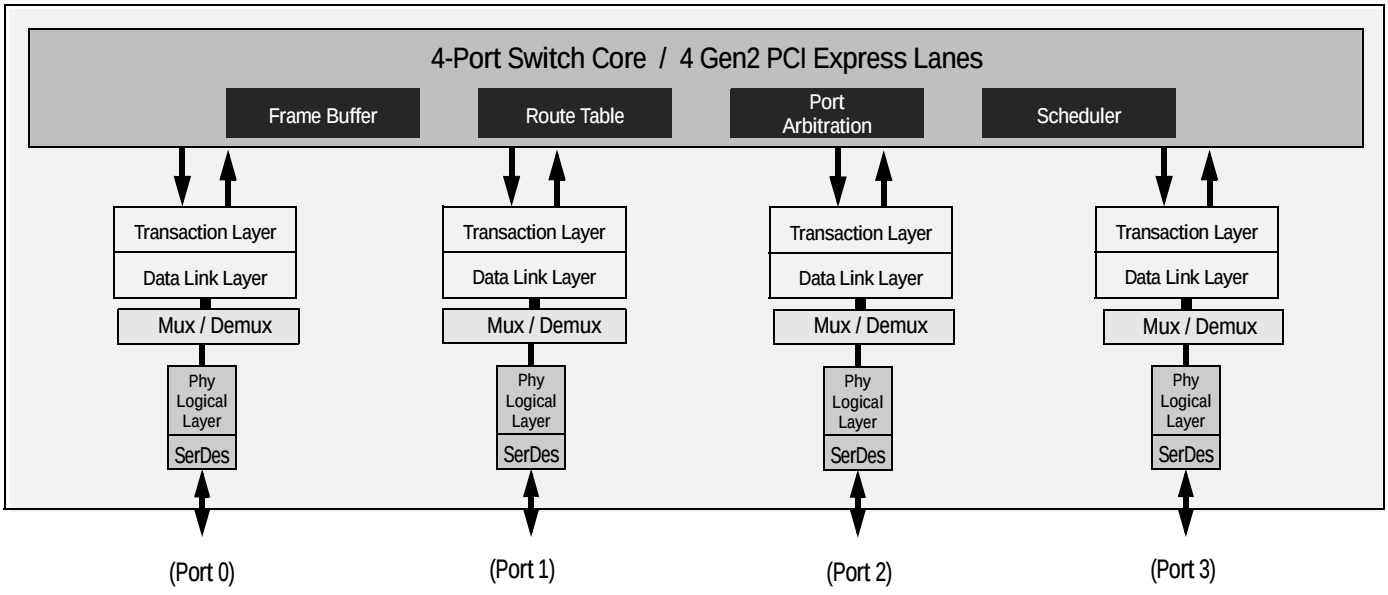

Figure 1 Internal Block Diagram

*Notice: The information in this document is subject to change without notice

- *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*

– *Support for PCI Express Active State Power Management (ASPM) link state*

- *Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3*

– *Supports PCI Express Power Budgeting Capability*

– *Configurable SerDes power consumption*

- *Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode*
- *Supports numerous SerDes Transmit Voltage Margin settings*

– *Unused SerDes are disabled*

◆ Testability and Debug Features

– *Built in Pseudo-Random Bit Stream (PRBS) generator*

– *Numerous SerDes test modes*

– *Ability to read and write any internal register via the SMBus*

– *Ability to bypass link training and force any link into any mode*

– *Provides statistics and performance counters*

◆ General Purpose Input/Output Pins

– *Each pin may be individually configured as an input or output*

– *Each pin may be individually configured as an interrupt input*

– *Some pins have selectable alternate functions*

◆ Packaged in a 19mm x 19mm, 324-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect the PES4T4G2 provides the most efficient high-performance I/O connectivity device for applications requiring high throughput, low latency and simple board layout. It provides PCI Express connectivity across 4 lanes and 4 ports. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 2.0.

The PES4T4G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES4T4G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

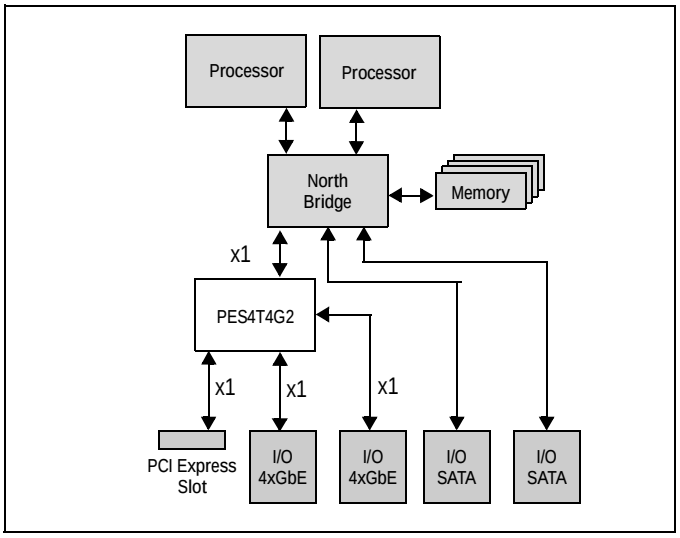

Figure 2 I/O Expansion Application

SMBus Interface

The PES4T4G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES4T4G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES4T4G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Two pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin and an SMBus data pin. The Master SMBus address is hardwired to 0x50, and the slave SMBus address is hardwired to 0x77.

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES4T4G2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES4T4G2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES4T4G2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES4T4G2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

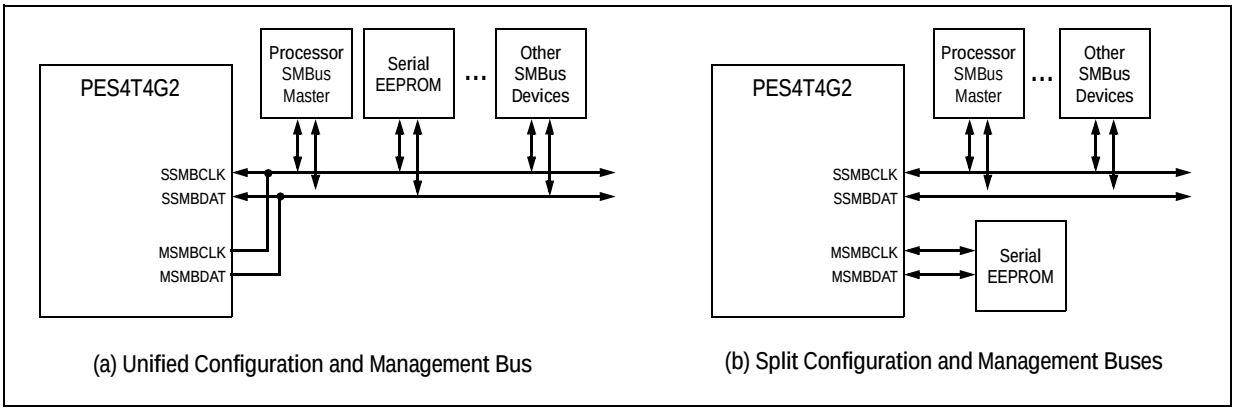

Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES4T4G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES4T4G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES4T4G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES4T4G2. In response to an I/O expander interrupt, the PES4T4G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES4T4G2 provides 7 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Most GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES4T4G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[0] PE0RN[0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pair for port 0. Port 0 is the upstream port.
PE0TP[0] PE0TN[0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pair for port 0. Port 0 is the upstream port.
PE1RP[0] PE1RN[0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pair for port 1.
PE1TP[0] PE1TN[0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pair for port 1.
PE2RP[0] PE2RN[0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pair for port 2.
PE3RP[0] PE3RN[0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pair for port 3.
PEREFCLKP PEREFCLKN	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is set at 100MHz.

Table 1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus which operates at 400 KHz.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus which operates at 400 KHz.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O expander interrupt 0 input.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 3 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register.
CCLKUS	I	**Common Clock Upstream.** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES4T4G2 and initiates a PCI Express fundamental reset.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES4T4G2 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN.

Table 4 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode.** The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset.** This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins

Signal	Type	Name/Description
REFRES0	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES1	I/O	**Port 1 External Reference Resistor.** Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES2	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES3	I/O	**Port 3 External Reference Resistor.** Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core $V_{DD.}$** Power supply for core logic.
V_{DD}I/O	I	**I/O $V_{DD.}$** LVTTL I/O buffer power supply.
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 6 Power, Ground, and SerDes Resistor Pins

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Pin Characteristics

Note: Some input pads of the PES4T4G2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[0]	I	CML	Serial Link		
	PE0RP[0]	I				
	PE0TN[0]	O				
	PE0TP[0]	O				
	PE1RN[0]	I				
	PE1RP[0]	I				
	PE1TN[0]	O				
	PE1TP[0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PEREFCLKN	I		Diff. Clock Input		Refer to Table 8
	PEREFCLKP	I				
SMBus	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[10:7, 2:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I		Input	pull-up	
	PERSTN	I		STI		
	SWMODE[2:0]	I		Input	pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 7 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
SerDes Reference Resistors	REFRES0	I/O	Analog	Input		
	REFRES1	I/O				
	REFRES2	I/O				
	REFRES3	I/O				

Table 7 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.

2. Schmitt Trigger Input (STI).

Logic Diagram — PES4T4G2

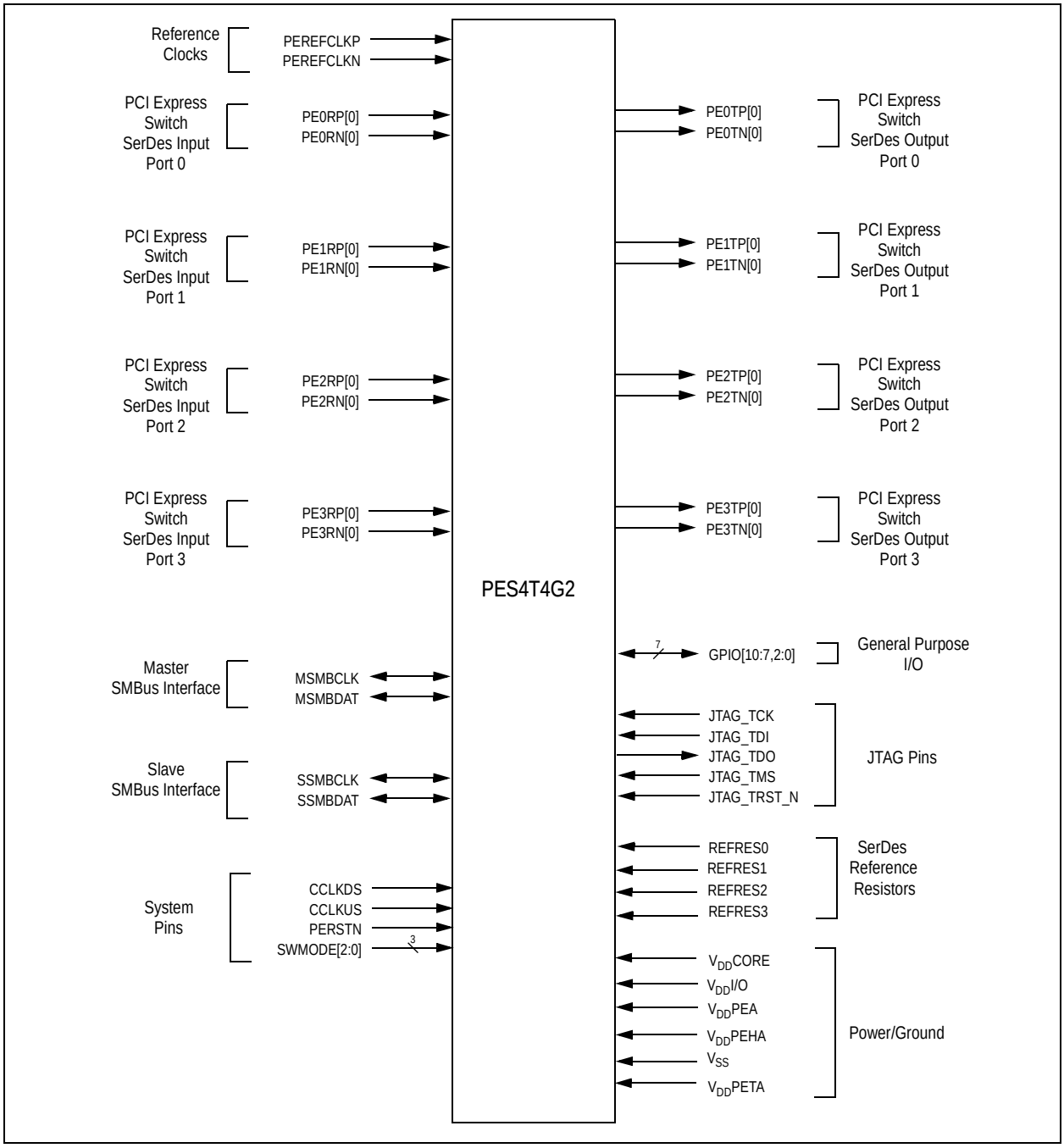

Figure 4 PES4T4G2 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		100[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 8 Input Clock Requirements

1. The input clock frequency is set at 100 MHz.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{MEAS-HPF}$	Transmit Jitter Measurement Filter	HPF: 1.5MHz			HPF: 1.0MHz			MHz
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter	NA					4.2	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver	NA					8.8	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:7,2:0][1]	Tpw[2]	None	50	—	ns	

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

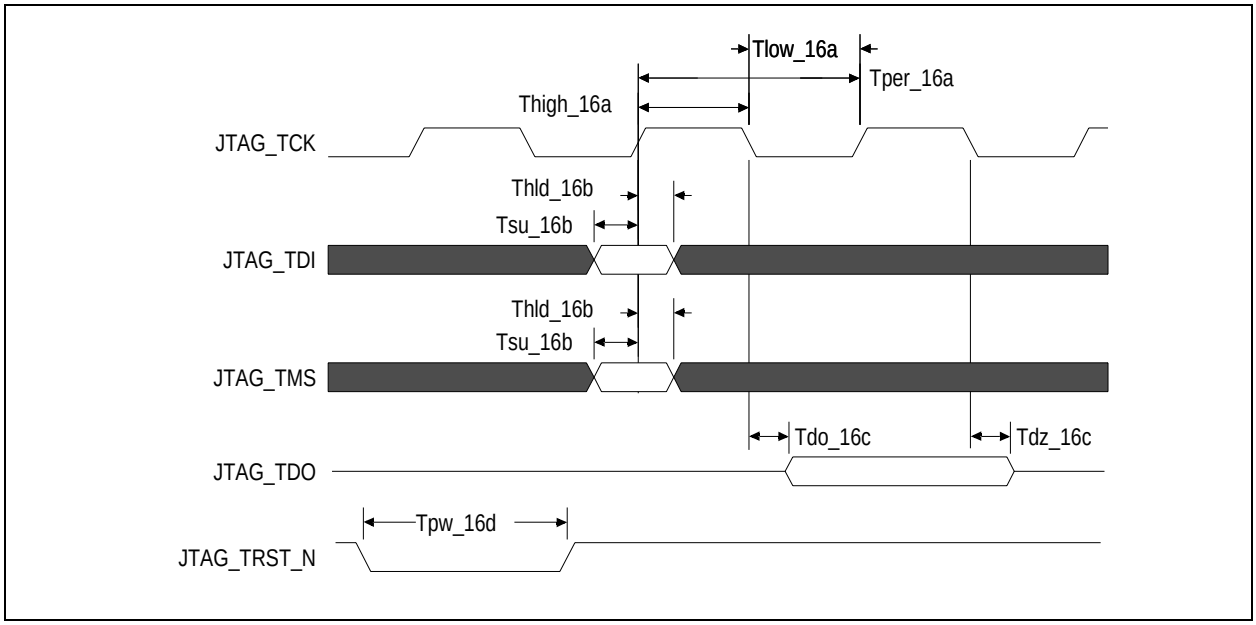


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES4T4G2 Operating Voltages

1. V_{DD}PEA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 13 PES4T4G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 12 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 12 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
1/1/1/1 Full Swing	mA	375	700	703	752	74	83	360	429	2	3		
	Watts	0.38	0.77	0.70	0.83	0.19	0.23	0.36	0.47	0.007	0.01	1.63	2.31
1/1/1/1 Half Swing	mA	375	700	703	752	74	83	180	215	2	3		
	Watts	0.38	0.77	0.70	0.83	0.19	0.23	0.18	0.24	0.007	0.01	1.45	2.07

Table 14 PES4T4G2 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES4T4G2 (19mm^2 FCBGA324 package). The data in Table 15 below contains information that is relevant to the thermal performance of the PES4T4G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum
θ_{JC}	Thermal Resistance, Junction-to-Case	1.1	^{0}C/W	
P	Power Dissipation of the Device	2.31	Watts	Maximum

Table 15 Thermal Specifications for PES4T4G2, 19x19 mm FCBGA324 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 15. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 15), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen 1			Gen 2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10dB: 0.05 - 1.25GHz 8dB: 1.25 - 2.5GHz	dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 16 DC Electrical Characteristics (Part 1 of 3)

I/O Type	Parameter	Description	Gen 1			Gen 2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10dB: 0.05 - 1.25GHz 8dB: 1.25 - 2.5GHz	dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—

Table 16 DC Electrical Characteristics (Part 2 of 3)

I/O Type	Parameter	Description	Gen 1			Gen 2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 16 DC Electrical Characteristics (Part 3 of 3)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Package Pinout — 324-BGA Signal Pinout for PES4T4G2

The following table lists the pin numbers and signal names for the PES4T4G2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B17	NC		D15	V_{DD}CORE		F13	V_{SS}	
A2	V_{DD}I/O		B18	NC		D16	V_{SS}		F14	NC	
A3	V_{DD}I/O		C1	NC		D17	V_{SS}		F15	NC	
A4	V_{DD}I/O		C2	NC		D18	V_{SS}		F16	V_{SS}	
A5	V_{SS}		C3	V_{SS}		E1	NC		F17	NC	
A6	V_{DD}I/O		C4	NC		E2	NC		F18	NC	
A7	V_{SS}		C5	NC		E3	V_{SS}		G1	V_{SS}	
A8	JTAG_TDI		C6	V_{SS}		E4	NC		G2	V_{SS}	
A9	MSMBDAT		C7	JTAG_TCK		E5	NC		G3	V_{SS}	
A10	V_{DD}I/O		C8	JTAG_TRST_N		E6	V_{DD}CORE		G4	V_{DD}CORE	
A11	V_{SS}		C9	SSMBDAT		E7	V_{DD}CORE		G5	V_{DD}CORE	
A12	GPIO_00	1	C10	CCLKDS		E8	V_{DD}CORE		G6	V_{DD}PEA	
A13	V_{DD}I/O		C11	SWMODE_2		E9	V_{SS}		G7	V_{DD}PEA	
A14	V_{DD}I/O		C12	GPIO_02	1	E10	V_{DD}CORE		G8	V_{DD}CORE	
A15	V_{SS}		C13	GPIO_09	1	E11	V_{DD}CORE		G9	V_{DD}CORE	
A16	V_{SS}		C14	NC		E12	V_{DD}CORE		G10	V_{DD}CORE	
A17	V_{DD}I/O		C15	NC		E13	V_{DD}CORE		G11	V_{SS}	
A18	V_{DD}I/O		C16	V_{SS}		E14	NC		G12	V_{DD}PEA	
B1	NC		C17	NC		E15	NC		G13	V_{DD}PEA	
B2	NC		C18	NC		E16	V_{SS}		G14	V_{DD}CORE	
B3	V_{SS}		D1	V_{SS}		E17	NC		G15	V_{DD}CORE	
B4	NC		D2	V_{SS}		E18	NC		G16	V_{SS}	
B5	NC		D3	V_{SS}		F1	PE3TP00		G17	V_{SS}	
B6	V_{DD}I/O		D4	V_{DD}CORE		F2	PE3TN00		G18	V_{SS}	
B7	V_{DD}I/O		D5	V_{DD}CORE		F3	V_{SS}		H1	NC	
B8	JTAG_TMS		D6	V_{SS}		F4	PE3RP00		H2	NC	
B9	SSMBCLK		D7	JTAG_TDO		F5	PE3RN00		H3	V_{SS}	
B10	V_{DD}I/O		D8	MSMBCLK		F6	V_{SS}		H4	NC	
B11	SWMODE_1		D9	CCLKUS		F7	V_{SS}		H5	NC	
B12	GPIO_01		D10	SWMODE_0		F8	V_{DD}CORE		H6	V_{DD}PEA	
B13	GPIO_10		D11	PERSTN		F9	V_{SS}		H7	V_{DD}PEA	
B14	NC		D12	GPIO_07	1	F10	V_{DD}CORE		H8	V_{DD}CORE	
B15	NC		D13	GPIO_08	1	F11	V_{SS}		H9	V_{DD}CORE	
B16	V_{SS}		D14	V_{DD}CORE		F12	V_{SS}		H10	V_{DD}CORE	

Table 17 PES4T4G2 324-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H11	V_{SS}		K13	V_{DD}PETA		M15	NC		P17	V_{DD}CORE	
H12	V_{DD}PEA		K14	V_{DD}CORE		M16	V_{SS}		P18	V_{SS}	
H13	V_{DD}PEA		K15	NC		M17	NC		R1	V_{SS}	
H14	NC		K16	V_{SS}		M18	NC		R2	V_{DD}CORE	
H15	NC		K17	NC		N1	V_{SS}		R3	V_{DD}CORE	
H16	V_{SS}		K18	NC		N2	V_{SS}		R4	NC	
H17	NC		L1	NC		N3	V_{SS}		R5	NC	
H18	NC		L2	NC		N4	V_{DD}CORE		R6	NC	
J1	NC		L3	V_{SS}		N5	V_{DD}CORE		R7	NC	
J2	NC		L4	NC		N6	V_{SS}		R8	PE1RP00	
J3	V_{SS}		L5	NC		N7	V_{SS}		R9	V_{DD}CORE	
J4	NC		L6	V_{DD}PETA		N8	V_{DD}PEA		R10	NC	
J5	NC		L7	V_{DD}PETA		N9	V_{DD}PEHA		R11	NC	
J6	V_{DD}PEHA		L8	V_{DD}PEA		N10	V_{DD}PETA		R12	V_{DD}CORE	
J7	V_{DD}PEHA		L9	V_{DD}PEHA		N11	V_{DD}PEA		R13	NC	
J8	V_{DD}CORE		L10	V_{DD}PETA		N12	V_{DD}PEHA		R14	PE0RP00	
J9	V_{SS}		L11	V_{DD}PEA		N13	V_{SS}		R15	V_{DD}CORE	
J10	V_{DD}CORE		L12	V_{DD}PEHA		N14	V_{SS}		R16	V_{DD}CORE	
J11	V_{SS}		L13	V_{DD}PETA		N15	V_{DD}CORE		R17	V_{DD}CORE	
J12	V_{DD}PEHA		L14	NC		N16	V_{SS}		R18	V_{SS}	
J13	V_{DD}PEHA		L15	NC		N17	V_{SS}		T1	V_{SS}	
J14	NC		L16	V_{SS}		N18	V_{SS}		T2	V_{SS}	
J15	NC		L17	NC		P1	V_{SS}		T3	V_{SS}	
J16	V_{SS}		L18	NC		P2	V_{DD}CORE		T4	V_{SS}	
J17	NC		M1	PE2TP00		P3	V_{DD}CORE		T5	V_{SS}	
J18	NC		M2	PE2TN00		P4	NC		T6	V_{SS}	
K1	REFRES2		M3	V_{SS}		P5	NC		T7	V_{SS}	
K2	REFRES3		M4	PE2RP00		P6	V_{DD}CORE		T8	V_{SS}	
K3	V_{SS}		M5	PE2RN00		P7	NC		T9	V_{SS}	
K4	V_{DD}CORE		M6	V_{DD}PETA		P8	PE1RN00		T10	V_{SS}	
K5	V_{DD}CORE		M7	V_{DD}PETA		P9	V_{DD}CORE		T11	V_{SS}	
K6	V_{DD}PETA		M8	V_{DD}PEA		P10	NC		T12	V_{SS}	
K7	V_{DD}PETA		M9	V_{DD}PEHA		P11	NC		T13	V_{SS}	
K8	V_{DD}CORE		M10	V_{DD}PETA		P12	V_{DD}CORE		T14	V_{SS}	
K9	V_{SS}		M11	V_{DD}PEA		P13	NC		T15	V_{SS}	
K10	V_{DD}CORE		M12	V_{DD}PEHA		P14	PE0RN00		T16	V_{SS}	
K11	V_{SS}		M13	V_{SS}		P15	V_{DD}CORE		T17	V_{SS}	
K12	V_{DD}PETA		M14	NC		P16	V_{DD}CORE		T18	V_{SS}	

Table 17 PES4T4G2 324-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U1	V_{SS}		U10	NC		V1	V_{SS}		V10	NC	
U2	PEREFCLKN		U11	NC		V2	PEREFCLKP		V11	NC	
U3	V_{SS}		U12	V_{SS}		V3	V_{SS}		V12	V_{SS}	
U4	NC		U13	NC		V4	NC		V13	NC	
U5	NC		U14	PE0TN00		V5	NC		V14	PE0TP00	
U6	REFRES1		U15	V_{SS}		V6	REFRES0		V15	V_{SS}	
U7	NC		U16	V_{SS}		V7	NC		V16	V_{SS}	
U8	PE1TN00		U17	V_{SS}		V8	PE1TP00		V17	V_{SS}	
U9	V_{SS}		U18	V_{SS}		V9	V_{SS}		V18	V_{SS}	

Table 17 PES4T4G2 324-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
A12	GPIO_00	P2RSTN
C12	GPIO_02	IOEXPINTN0
D12	GPIO_07	GPEN
D13	GPIO_08	P1RSTN
C13	GPIO_09	P3RSTN

Table 18 PES4T4G2 Alternate Signal Functions

No Connection Pins

NC Pins	NC Pins	NC Pins	NC Pins	NC Pins	NC Pins
B1	C18	H4	K17	P5	U10
B2	E1	H5	K18	P7	U11
B4	E2	H14	L1	P10	U13
B5	E4	H15	L2	P11	V4
B14	E5	H17	L4	P13	V5
B15	E14	H18	L5	R4	V7
B17	E15	J1	L14	R5	V10
B18	E17	J2	L15	R6	V11
C1	E18	J4	L17	R7	V13
C2	F14	J5	L18	R10	
C4	F15	J14	M14	R11	
C5	F17	J15	M15	R13	
C14	F18	J17	M17	U4	
C15	H1	J18	M18	U5	
C17	H2	K15	P4	U7	

Table 19 PES4T4G2 No Connection Pins

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEHA	V_{DD}PETA
D4	G9	N15	A2	G6	J6	K6
D5	G10	P2	A3	G7	J7	K7
D14	G14	P3	A4	G12	J12	K12
D15	G15	P6	A6	G13	J13	K13
E6	H8	P9	A10	H6	L9	L6
E7	H9	P12	A13	H7	L12	L7
E8	H10	P15	A14	H12	M9	L10
E10	J8	P16	A17	H13	M12	L13
E11	J10	P17	A18	L8	N9	M6
E12	K4	R2	B6	L11	N12	M7
E13	K5	R3	B7	M8		M10
F8	K8	R9	B10	M11		N10
F10	K10	R12		N8		
G4	K14	R15		N11		
G5	N4	R16				
G8	N5	R17				

Table 20 PES4T4G2 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D18	G17	M16	T3	U3
A5	E3	G18	N1	T4	U9
A7	E9	H3	N2	T5	U12
A11	E16	H11	N3	T6	U15
A15	F3	H16	N6	T7	U16
A16	F6	J3	N7	T8	U17
B3	F7	J9	N13	T9	U18
B16	F9	J11	N14	T10	V1
C3	F11	J16	N16	T11	V3
C6	F12	K3	N17	T12	V9
C16	F13	K9	N18	T13	V12
D1	F16	K11	P1	T14	V15
D2	G1	K16	P18	T15	V16
D3	G2	L3	R1	T16	V17
D6	G3	L16	R18	T17	V18
D16	G11	M3	T1	T18	
D17	G16	M13	T2	U1	

Table 21 PES4T4G2 Ground Pins

Signals Listed Alphabetically

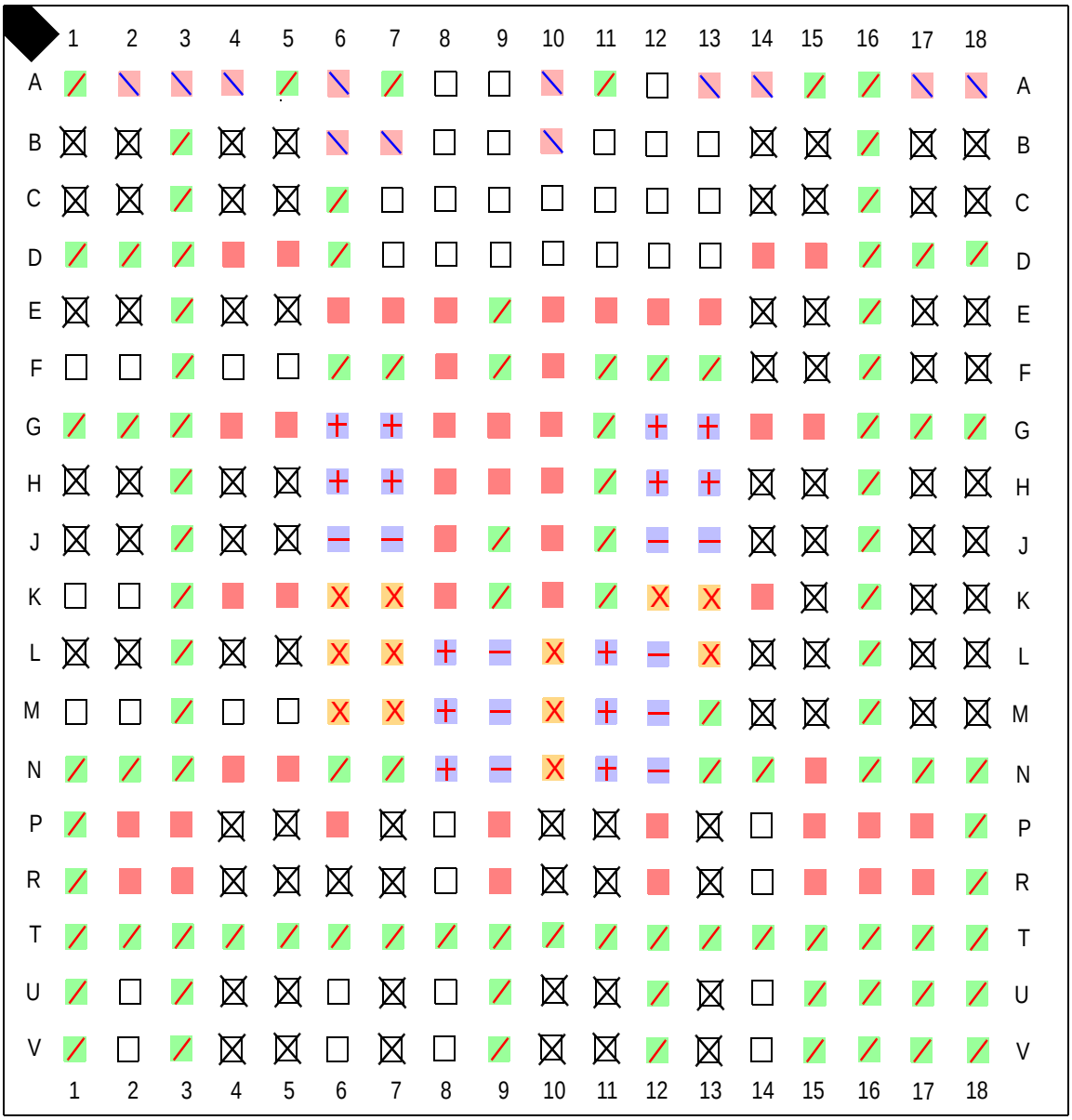
Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	C10	System
CCLKUS	I	D9	
GPIO_00	I/O	A12	General Purpose Input/Output
GPIO_01	I/O	B12	
GPIO_02	I/O	C12	
GPIO_07	I/O	D12	
GPIO_08	I/O	D13	
GPIO_09	I/O	C13	
GPIO_10	I/O	B13	
JTAG_TCK	I	C7	JTAG
JTAG_TDI	I	A8	
JTAG_TDO	O	D7	
JTAG_TMS	I	B8	
JTAG_TRST_N	I	C8	
MSMBCLK	I/O	D8	SMBus
MSMBDAT	I/O	A9	
NO CONNECTION	See Table 19		
PE0RN00	I	P14	PCI Express
PE0RP00	I	R14	
PE0TN00	O	U14	
PE0TP00	O	V14	
PE1RN00	I	P8	
PE1RP00	I	R8	
PE1TN00	O	U8	
PE1TP00	O	V8	
PE2RN00	I	M5	
PE2RP00	I	M4	
PE2TN00	O	M2	
PE2TP00	O	M1	
PE3RN00	I	F5	
PE3RP00	I	F4	
PE3TN00	O	F2	
PE3TP00	O	F1	

Table 22 89PES4T4G2 Alphabetical Signal List (Part 1 of 2)

Signal Name	I/O Type	Location	Signal Category
PEREFCLKN	I	U2	PCI Express (cont.)
PEREFCLKP	I	V2	
PERSTN	I	D11	System
REFRES0	I/O	V6	SerDes Reference Resistors
REFRES1	I/O	U6	
REFRES2	I/O	K1	
REFRES3	I/O	K2	
SSMBCLK	I/O	B9	SMBus
SSMBDAT	I/O	C9	
SWMODE_0	I	D10	System
SWMODE_1	I	B11	
SWMODE_2	I	C11	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Table 20 for a listing of power pins.		
V_{SS}	See Table 21 for a listing of ground pins.		

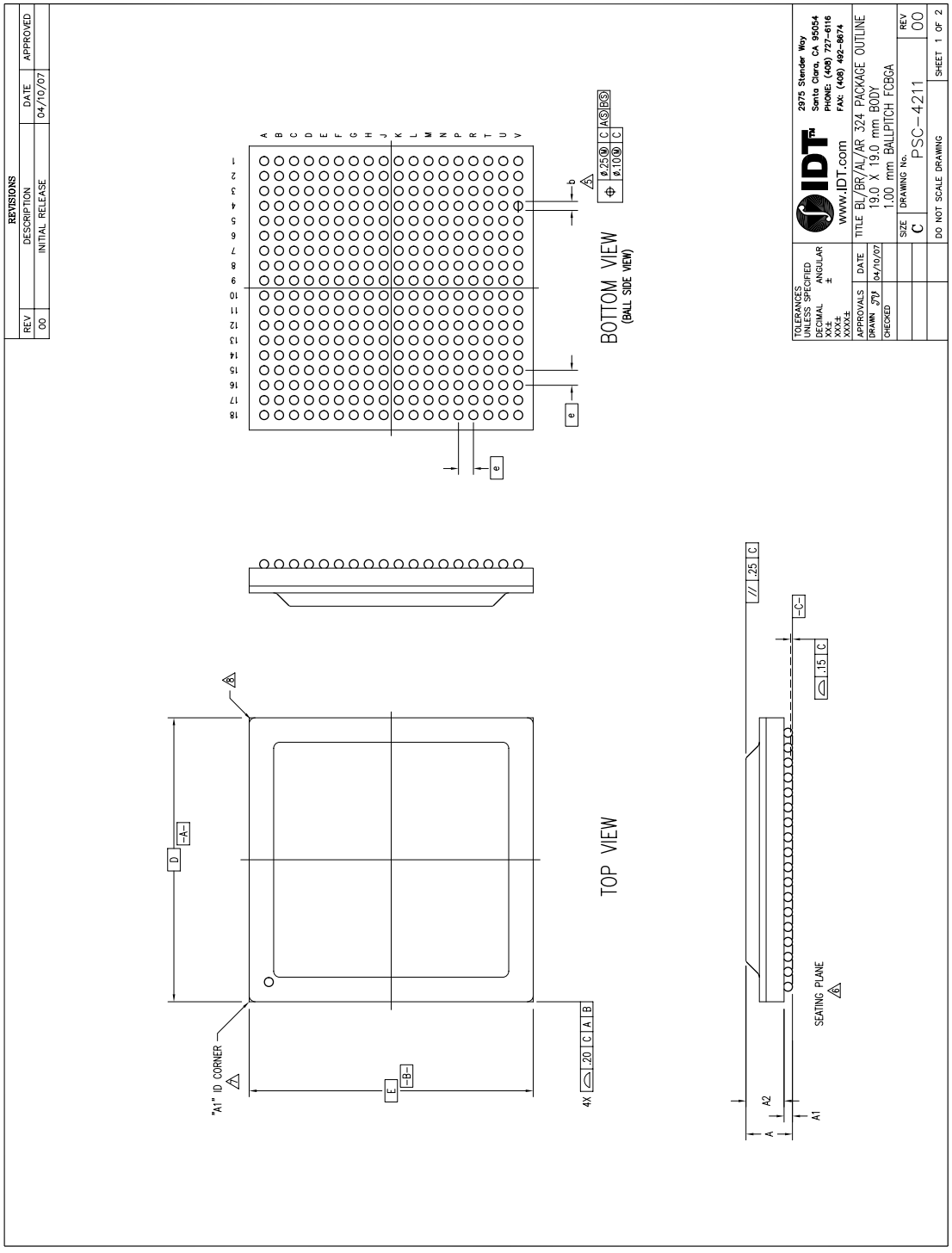
Table 22 89PES4T4G2 Alphabetical Signal List (Part 2 of 2)

PES4T4G2 Pinout — Top View



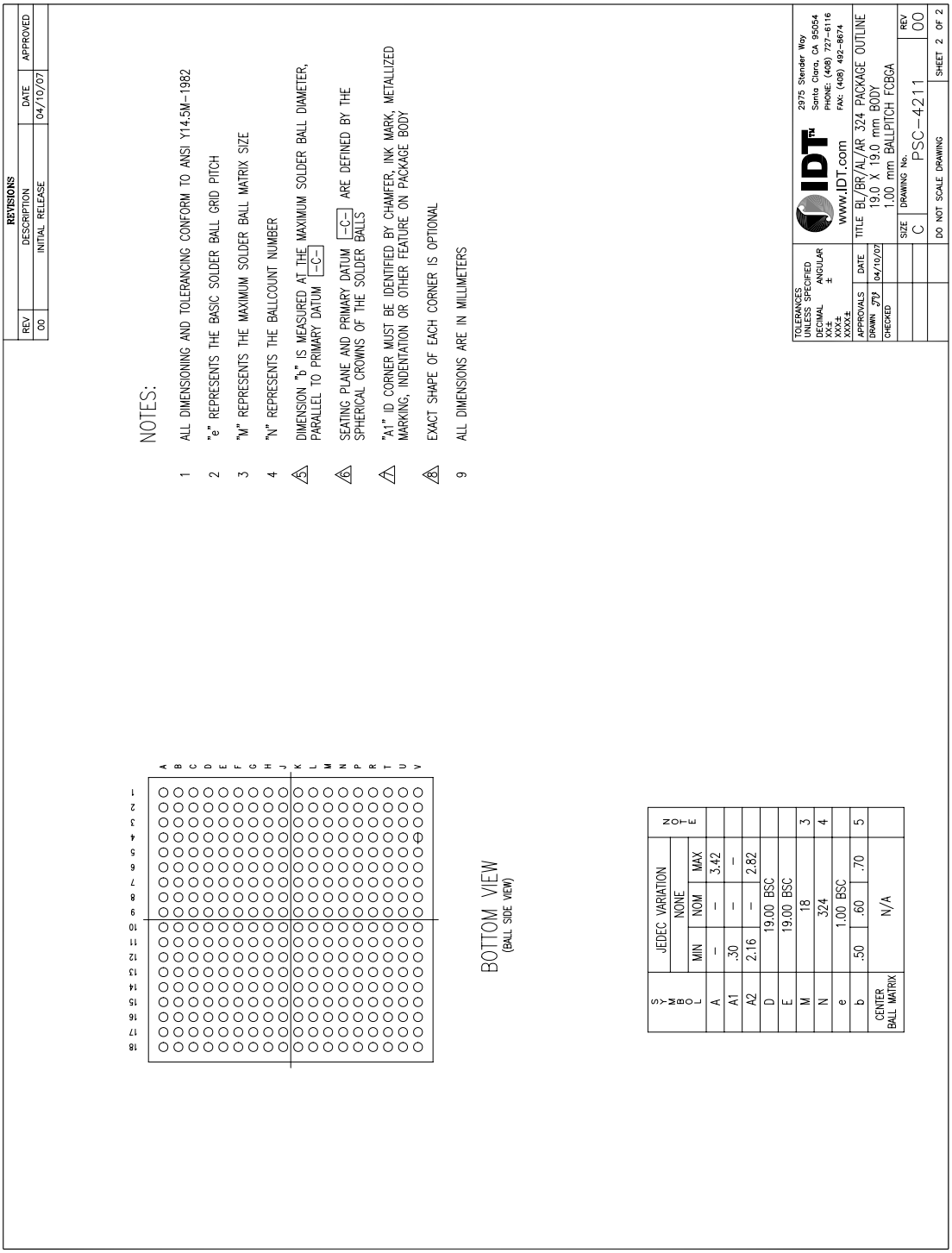
Advance Information

PES4T4G2 Package Drawing — 324-Pin AL324/AR324



Advance Information

PES4T4G2 Package Drawing — Page Two



Advance Information

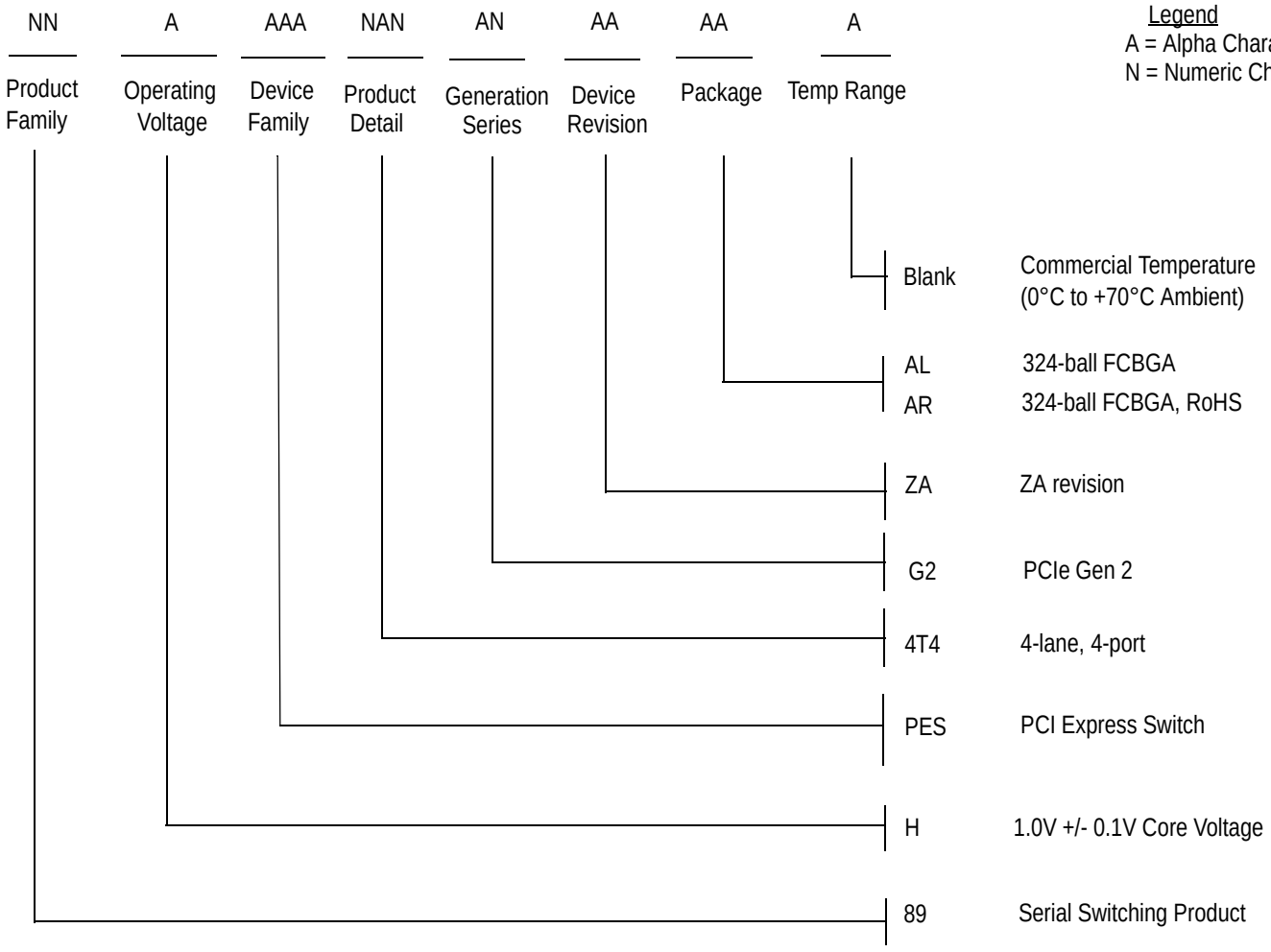
Revision History

November 12, 2007: Initial publication of Advanced data sheet.

December 4, 2007: Added address location for MSMBADDR (0x50) and SSMBADDR (0x77).

January 25, 2008: Revised pinout tables and pinout graphic.

Ordering Information



Advance Information

Valid Combinations

89HPES4T4G2ZAAL	324-ball FCBGA package, Commercial Temperature
89HPES4T4G2ZAAR	324-ball RoHS FCBGA package, Commercial Temperature

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