

## DEVICE DESCRIPTION

The TRAC family of Field Programmable Analog Devices offers an integrated path from signal processing problems to working silicon solutions - in minutes! The Totally Reconfigurable Analog Circuit is a highly flexible single chip solution to the signal processing problems found in many markets.

Introducing a Top-Down, Structured design discipline, TRAC enables rapid implementation, prototyping and product release. Rather than working at the component level, TRAC champions the Computational Approach, providing designers with benefits formerly associated only with programmable digital devices. TRAC brings a truly integrated Signal Processing problem solving process, offering a path to Custom Silicon for higher volume users.

TRAC devices have to be loaded with program data at power-up and run from a split 5V supply. By integrating the loading interface circuitry, voltage regulation, supply monitoring and thermal protection, the TRAC support circuit (TRAC-S2) further simplifies circuit integration and interface with memory devices.

An adjustable frequency oscillator clocks program data out of a serial output memory device and into any number of cascaded TRAC devices. By monitoring the bit stream pattern, TRAC-S2 can sense when loading is complete and stop clocking automatically.

An adjustable 'rail-splitter' generates the ground supply rail, and the supply monitoring function initiates program load on power-up, and after power failure or serious fluctuation. Thermal shutdown further protects the device against overheating.

## FEATURES & BENEFITS

- Makes designing TRAC circuits easier, production prototyping quicker
- Reduces component count and manufacturing costs
- Enables simple connection of a serial output EEPROM or other memory device to TRAC
- Compatible with current and future TRAC devices
- Automatic program loading at power-up
- Supply monitor function reloads program after power failure or fluctuation
- Frequency of on-chip oscillator user-defined
- Senses number of cascaded TRAC devices automatically
- Automatically stops clocking when program loading complete
- Simplifies generation of TRAC supply voltages
- Ground voltage user defined
- Thermal shutdown function protects against overloading due to circuit failures
- Full industrial temperature range

## ORDERING INFORMATION

PART NUMBER	PACKAGE	PART MARK
TRAC-S2Q16	QSOP16	TRAC-S2

# TRAC-S2

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage	0V to +7V
Supply Current	50mA
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-55°C to 125°C

## ELECTRICAL CHARACTERISTICS

**Test Conditions: Temperature=25°C, V<sub>DD</sub>=5V, V<sub>SS</sub>=0V, CLCR\_IN=0V, 100nF between AGND\_OUT and V<sub>SS</sub>, unless otherwise stated.**

PARAMETER	CONDITIONS	MIN	TYPICAL	MAX
Supply Voltage Operating Range		4.8V	5.0V	5.2V
Supply Current	Standby (CLCR_IN = 0V) Clocking (CLCR_IN = 5V)	1.5mA 2.9mA	1.9mA 3.7mA	2.8mA 5.5mA
<b>RAIL SPLITTER</b>				
SETV(Input Current)	SETV = 2.50V		50nA	200nA
AGND_OUT (Output Voltage)	SETV = 2.50V (No Load) SETV = 2.0V (No Load)	2.49V 1.99V	2.50V 2.00V	2.51V 2.01V
AGND_OUT (Output Voltage)	SETV = 2.50V; I <sub>SINK</sub> = 20mA  SETV = 2.50V; I <sub>SOURCE</sub> = 20mA			AGND_OUT + 0.010V  AGND_OUT - 0.010V
<b>SUPPLY MONITOR</b>				
RESET_OUT (Threshold Voltage)	High State Output (VDD increasing) Low State Output (VDD decreasing)	4.35V 4.35V	4.67V 4.65V	4.75V 4.75V
RESET_OUT (Hysteresis)		0.01V	0.02V	0.08V
RESET_OUT (Onstate output sink current)	VDD = RESET_OUT = 4V		0.14mA	
RESET_OUT (Offstate output current)	VDD = RESET_OUT = 5V		0.18mA	
PROPAGATION DELAY	VDD step from 5.0V to 4.0V		1μS	
<b>PROGRAMMING LOGIC</b>				
CLK_OUT (Frequency)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	7kHz	10kHz	15kHz
CLK_OUT (Max Programming Frequency)	47pF between CAP and V <sub>SS</sub> CLCR_IN = 5V			200kHz
CLK_OUT (High output voltage)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	3.90V	4.10V	4.50V
NOT CLK_OUT(Frequency)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	7kHz	10kHz	15kHz
NOT CLK_OUT(High output voltage)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	4.00V	4.20V	4.60V

# TRAC-S2

**ELECTRICAL CHARACTERISTICS**

**Test Conditions: Temperature=25°C, V<sub>DD</sub>=5V, V<sub>SS</sub>=0V, CLCR\_IN=0V, 100nF between AGND\_OUT and V<sub>SS</sub>, unless otherwise stated.**

DATA_OUT(Frequency)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	1.7kHz	2.5kHz	4.0kHz
DATA_OUT(High output voltage)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	3.90V	4.10V	4.50V
SELECT (Output Voltage)	2.2nF between CAP and V <sub>SS</sub> CLCR_IN = 5V	4.8V	4.99V	5.00V

**DESCRIPTION OF PIN FUNCTIONS**

**Inputs**

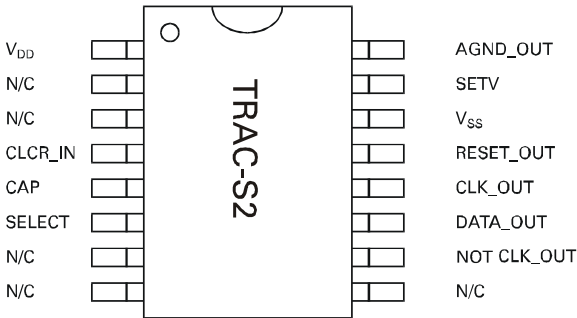
- SETV** Defines the AGND\_OUT voltage. Normally set by potential divider
- CLCR\_IN** Active high to enable clock
- CAP** Capacitor to V<sub>SS</sub> sets clock frequency

**Outputs**

- AGND\_OUT** Analog Ground. Able to source and sink current
- SELECT** Active high when CLCR\_IN is logic high. Enables memory device
- CLK\_OUT** Fed to EEPROM clock input
- NOT CLK\_OUT** Fed to TRAC clock input
- DATA\_OUT** CLK\_OUT divided by four. Fed to serial output memory device
- RESET\_OUT** Reset for TRAC Support Circuit and TRAC devices

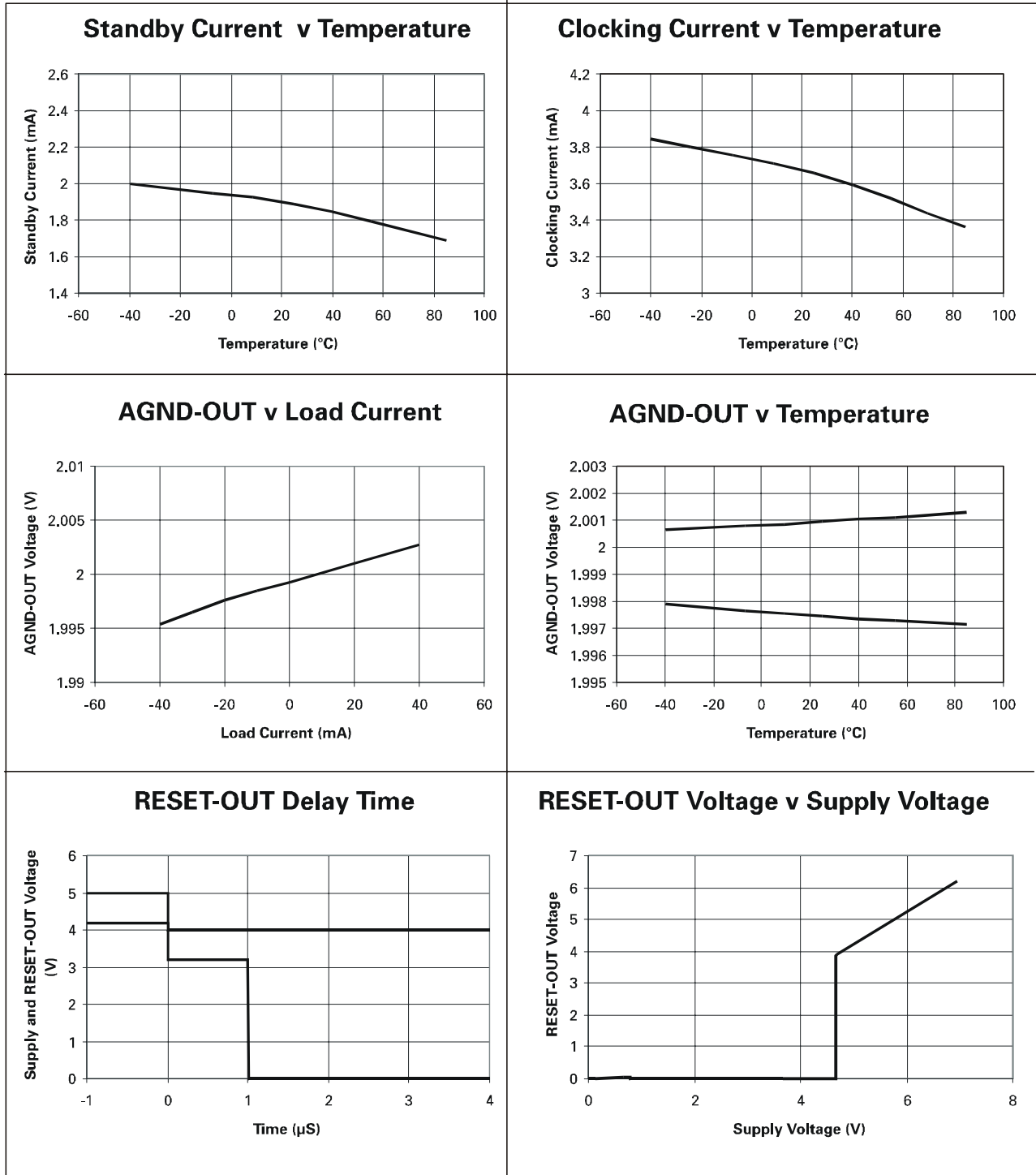
**General notes for the TRAC Support Circuit**

- An on-chip oscillator produces the output CLK\_OUT and NOT CLK\_OUT. CLCR\_IN must be logic high (V<sub>DD</sub>) to activate CLK\_OUT and NOT CLK\_OUT
- The CLK\_OUT output frequency is divided by four to give the DATA\_OUT output. Therefore CLCR\_IN must be logic high (V<sub>DD</sub>) to activate DATA\_OUT
- For AGND\_OUT stability under load, a 100nF capacitor is required between AGND\_OUT and V<sub>SS</sub>



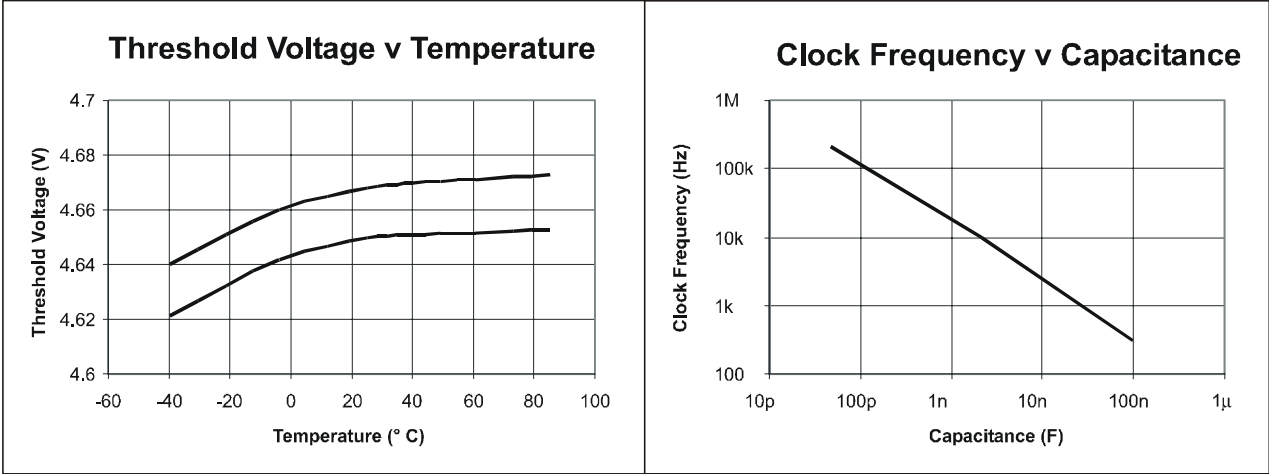
# TRAC-S2

## TYPICAL CHARACTERISTICS



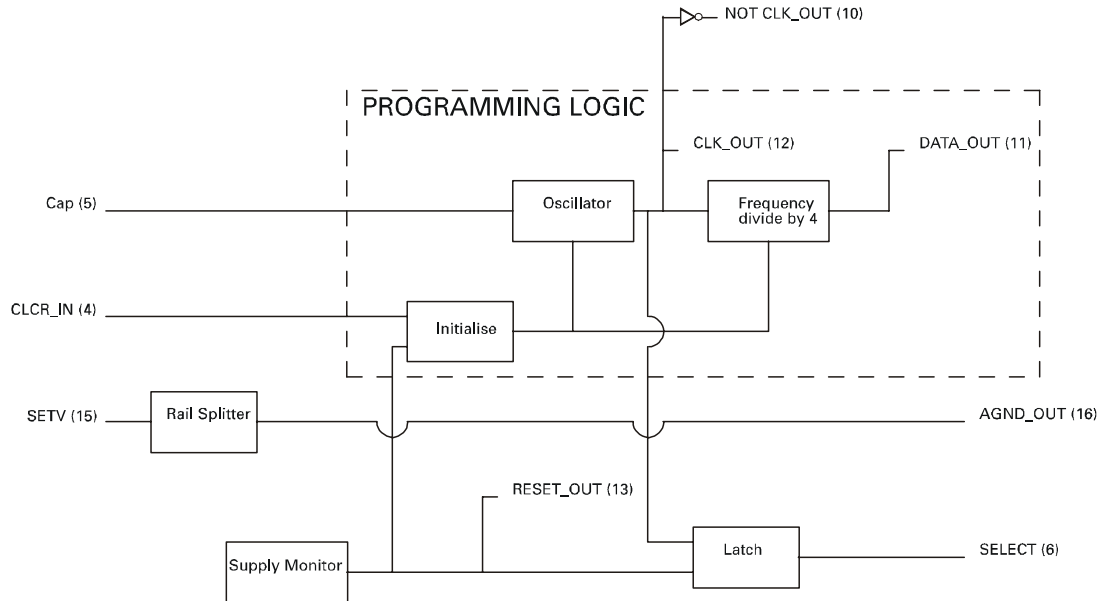
# TRAC-S2

## TYPICAL CHARACTERISTICS



# TRAC-S2

## BLOCK DIAGRAM



## Description of the TRAC Support Circuit

### 1) Rail Splitter

This section provides the analog ground rail between the 5V supply. An external potential divider can be connected to the SETV pin which enables AGND\_OUT to be set to the desired potential. The output stage of the rail splitter has been designed to provide power capabilities for 4 TRAC devices and accompanying circuitry. The circuit has low output resistance enabling a drive capability of +/- 20mA.

### 2) Supply Monitor

This section utilises the precision ZSM560 supply monitor design. The RESET\_OUT provides a signal to reset all the devices included in the programming and operation of TRAC. This ensures that all devices are switched on and off simultaneously.

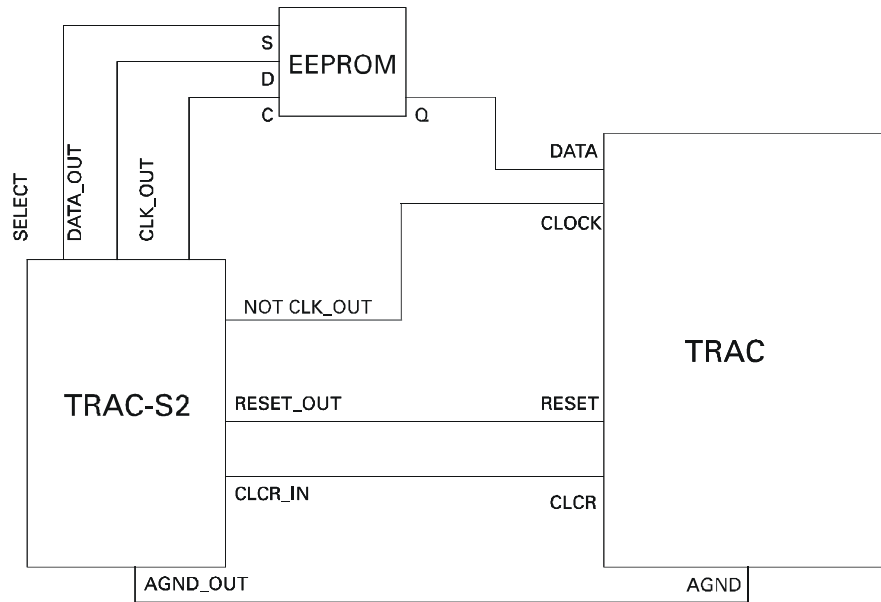
### 3) Programming Logic

This section provides TRAC and memory with the signals required for programming. The clock is generated on chip, with the frequency set by an external capacitor. The DATA\_OUT signal is generated by dividing the clock frequency by 4. This provides the code to initialise an EEPROM and prompt it to output data. The SELECT pin enables EEPROM chip select.

This section also takes an input signal from the final TRAC device, CLCR\_IN. This signal is normally 'high' and goes 'low' when programming is complete, and is used to terminate the CLK\_OUT and DATA\_OUT signals.

# TRAC-S2

## APPLICATION CIRCUIT



Connections between the support circuit, the EEPROM and the TRAC device are shown above.

For a more detailed explanation of the circuit see the application note AN27, "How to use the TRAC support chip". This also shows the circuit required to program multiple TRAC devices.

### LIST OF COMPATIBLE MEMORY DEVICES

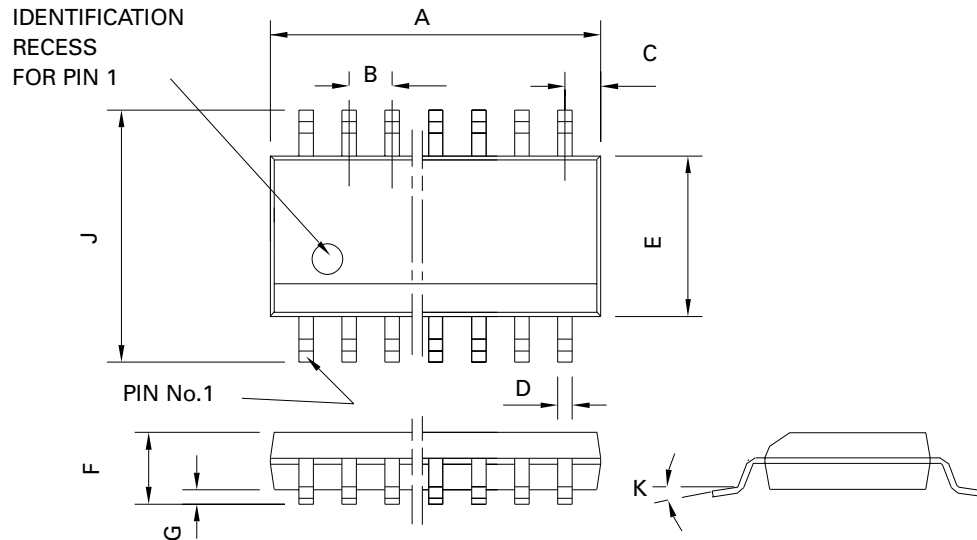
ST9346CB1 (SGS-Thomson)

93LC46B (Microchip)

NM92C46 (National Semiconductor)

# TRAC-S2

## PACKAGE DIMENSIONS



## QSOP16

PIN	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	4.80	4.98	0.189	0.196
B	0.635		0.025 NOM	
C	0.177	0.267	0.007	0.011
D	0.20	0.30	0.008	0.012
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.053	0.069
G	0.10	0.25	0.004	0.01
J	5.79	6.20	0.228	0.244
K	0°	8°	0°	8°



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