CS5307

Four-Phase VRM 9.0 Buck Controller

Multiphase controllers provide fast, accurate regulation with the control features required to power the next generation of processors in desktop, workstation and server applications. Combined with external gate drivers and power components, the CS5307 implements a compact, highly integrated buck converter. Enhanced V^{2}™ control inherently compensates for variations in both line and load. Current sharing between phases is achieved by Peak Current Sharing.

The CS5307 includes Power Good with a programmable lower threshold.

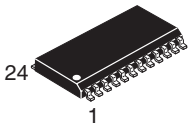
Applications include Embedded Processor Power and low voltage/high current power supplies.

Features

- Switching Regulator Controller
  - Lossless Current Sensing
  - Enhanced V^{2} Control Method Provides Excellent Regulation and Fast Transient Response
  - Programmable 200 to 800 kHz Switching Frequency (Per Phase)
  - Duty Cycle – 0% to 100%
  - Programmable Adaptive Voltage Positioning Reduces Output Capacitor Requirements
  - Programmable Soft Start
- Accurate Current Sharing
- Protection Features
  - Pulse–by–Pulse Current Limit for Each Phase
  - Programmable Hiccup Overcurrent Protection
  - All “1” DAC Code Fault
  - Processor Overvoltage Protection through Bottom MOSFETs
  - Undervoltage Lockout
- System Power Management
  - 5–Bit DAC With 1.0% Tolerance Compatible with VRM 9.0
  - Power Good Output
  - Programmable Power Good Lower Threshold
  - Guaranteed Startup at –20°C

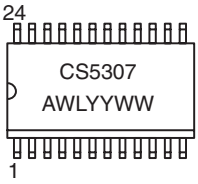
ON Semiconductor®

http://onsemi.com



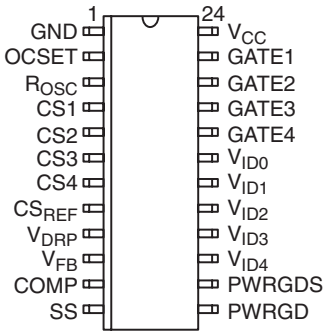
SO–24L
DW SUFFIX
CASE 751E

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5307GDW24	SO–24L	30 Units/Rail
CS5307GDWR24	SO–24L	1000 Tape & Reel

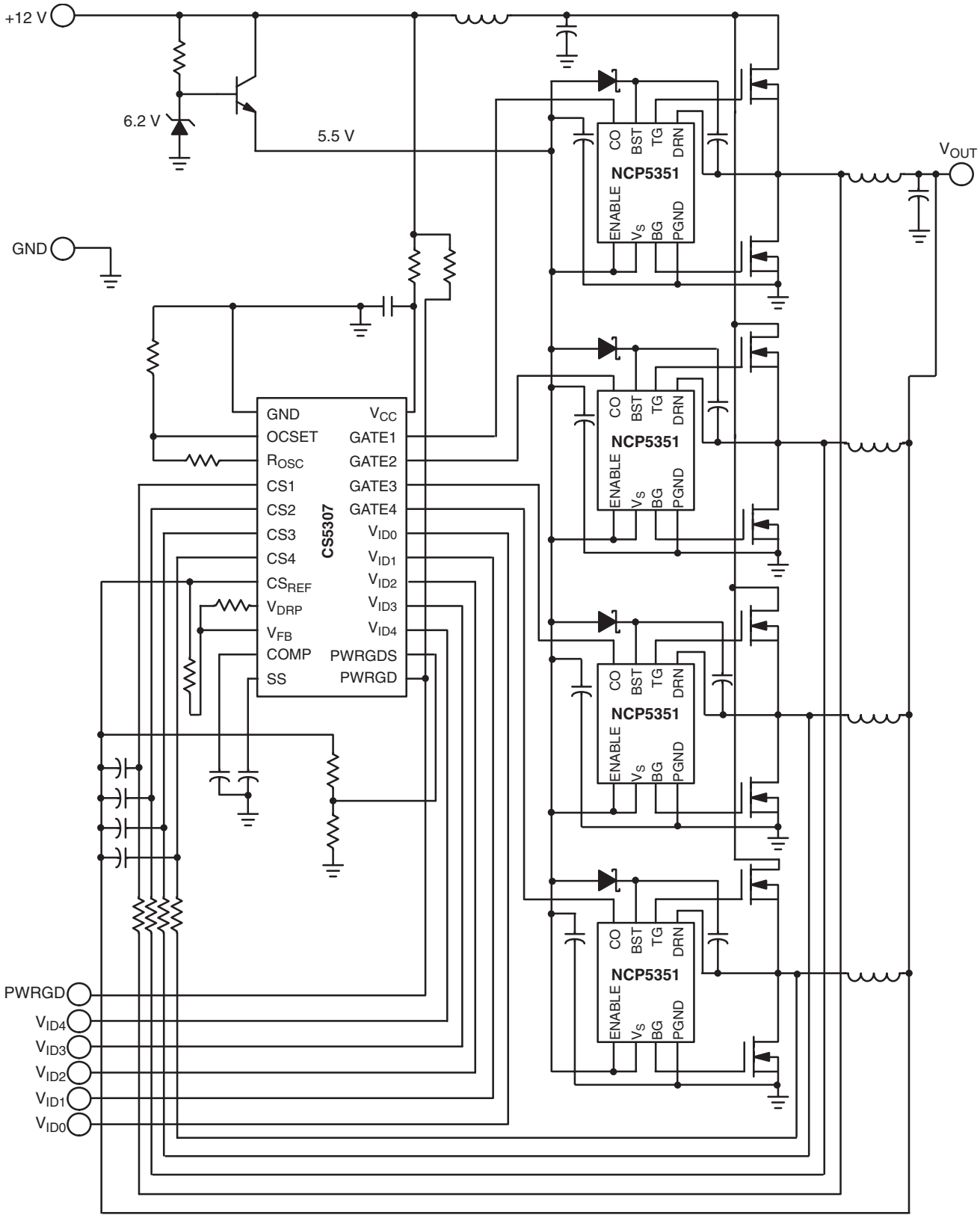


Figure 1. Application Diagram, 12 V to 1.5 V/80 A Four–Phase Converter

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature	150	°C
Storage Temperature Range	–65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Package Thermal Resistance Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$	 16 80	 °C/W °C/W
Lead Temperature Soldering: Reflow (Note 1.)	230 peak	°C
MSL	Level 1	–

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Number	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	GND	N/A	N/A	0.4 A, 1.0 μs, 100 mA DC	N/A
2	OCSET	7.0 V	–0.3 V	1.0 mA	1.0 mA
3	R_{OSC}	7.0 V	–0.3 V	1.0 mA	1.0 mA
4–7	CS1–CS4	7.0 V	–0.3 V	1.0 mA	1.0 mA
8	CS_{REF}	7.0 V	–0.3 V	1.0 mA	1.0 mA
9	V_{DRP}	7.0 V	–0.3 V	1.0 mA	1.0 mA
10	V_{FB}	7.0 V	–0.3 V	1.0 mA	1.0 mA
11	COMP	7.0 V	–0.3 V	1.0 mA	1.0 mA
12	SS	7.0 V	–0.3 V	1.0 mA	1.0 mA
13	PWRGD	18 V	–0.3 V	1.0 mA	10 mA
14	PWRGDS	7.0 V	–0.3 V	1.0 mA	1.0 mA
15–19	V_{ID4}–V_{ID0}	18 V	–0.3 V	1.0 mA	1.0 mA
20–23	GATE4–GATE1	7.0 V	–0.3 V	0.1 A, 1.0 μs, 25 mA DC	0.1 A, 1.0 μs, 25 mA DC
24	V_{CC}	18 V	–0.3 V	100 mA	1.0 mA

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.5\ V < V_{CC} < 14\ V$; $C_{GATEx} = 100\ pF$, $C_{COMP} = 0.01\mu F$, $C_{SS} = 0.1\mu F$, $C_{VCC} = 0.1\mu F$, $R_{ROSC} = 32.4\ k\Omega$, $V_{OCSET} = 0.54\ V$, DAC Code 01110; unless otherwise stated.)

Parameter					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC (0 = Connected to GND, 1 = Open or Pull–Up to Internal 3.3 V or External Voltage 12 V)									
Accuracy (all codes) V_{ID} code					Connect V_{FB} to COMP, Measure COMP	–1.0	–	+1.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
1	1	1	1	1			Fault		
1	1	1	1	0		1.089	1.100	1.111	V
1	1	1	0	1		1.114	1.125	1.136	V
1	1	1	0	0		1.139	1.150	1.162	V
1	1	0	1	1		1.163	1.175	1.187	V
1	1	0	1	0		1.188	1.200	1.212	V
1	1	0	0	1		1.213	1.225	1.237	V
1	1	0	0	0		1.238	1.250	1.263	V
1	0	1	1	1		1.263	1.275	1.288	V
1	0	1	1	0		1.287	1.300	1.313	V
1	0	1	0	1		1.312	1.325	1.338	V
1	0	1	0	0		1.337	1.350	1.364	V
1	0	0	1	1		1.361	1.375	1.389	V
1	0	0	1	0		1.386	1.400	1.414	V
1	0	0	0	1		1.411	1.425	1.439	V
1	0	0	0	0		1.436	1.450	1.465	V
0	1	1	1	1		1.460	1.475	1.490	V
0	1	1	1	0		1.485	1.500	1.515	V
0	1	1	0	1		1.510	1.525	1.540	V
0	1	1	0	0		1.535	1.550	1.566	V
0	1	0	1	1		1.560	1.575	1.591	V
0	1	0	1	0		1.584	1.600	1.616	V
0	1	0	0	1		1.609	1.625	1.641	V
0	1	0	0	0		1.634	1.650	1.667	V
0	0	1	1	1		1.658	1.675	1.692	V
0	0	1	1	0		1.683	1.700	1.717	V
0	0	1	0	1		1.708	1.725	1.742	V
0	0	1	0	0		1.733	1.750	1.768	V
0	0	0	1	1		1.757	1.775	1.793	V
0	0	0	1	0		1.782	1.800	1.818	V
0	0	0	0	1		1.807	1.825	1.843	V
0	0	0	0	0		1.832	1.850	1.869	V
Input Threshold					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	1.00	1.25	1.5	V
Input Pull–Up Resistance					$0\ V < V_{ID4}$, V_{ID3}, V_{ID2},V_{ID1}, $V_{ID0} < 3.3\ V$	25	50	100	kΩ

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.5\ V < V_{CC} < 14\ V$; $C_{GATEx} = 100\ pF$, $C_{COMP} = 0.01\mu F$, $C_{SS} = 0.1\mu F$, $C_{VCC} = 0.1\mu F$, $R_{ROSC} = 32.4\ k\Omega$, $V_{OCSET} = 0.54\ V$, DAC Code 01110; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC (0 = Connected to GND, 1 = Open or Pull–Up to Internal 3.3 V or External Voltage 12 V) (continued)					
Pull–Up Voltage	1.0 MΩ to GND	2.5	2.7	3.0	V
Power Good Output					
Upper Threshold	Force PWRGDS	1.876 (–5%)	1.975	2.074 (+5%)	V
Lower Threshold	Force PWRGDS	–5%	$V_{ID}/2$	+5%	V
Switch Leakage Current	V_{CC} = 14 V, PWRGDS = 1.4 V	–	0.1	1.0	μA
Delay	PWRGDS low to PWRGD low	100	800	2000	μs
Output Low Voltage	PWRGDS = 1.0 V, I_{PWRGD} = 4.0 mA	–	0.15	0.4	V
Voltage Feedback Error Amplifier					
V_{FB} Bias Current	Note 2	9.9	10.25	10.6	μA
Comp Source Current	COMP = 0.5 V to 2.0 V, V_{FB} = 1.8 V, DAC = 00000	15	30	60	μA
Comp Sink Current	COMP = 0.5 V to 2.0 V, V_{FB} = 1.15 V, DAC = 11110	15	30	60	μA
Transconductance	$-10\ \mu A < I_{COMP} < +10\ \mu A$, Note 3	200	500	750	μmho
Output Impedance	–	–	2.5	–	MΩ
Open Loop DC Gain	Note 3	45	95	–	dB
Unity Gain Bandwidth	–	–	50	–	kHZ
PSRR @ 1.0 kHz	–	–	60	–	dB
COMP Max Voltage	V_{FB} = 0 V	2.4	2.7	–	V
COMP Min Voltage	V_{FB} = 1.6 V	–	50	150	mV
PWM Comparators					
Minimum Pulse Width	Measured from CSx to GATEx, $V_{FB} = CS_{REF}$ = 0.5 V, COMP = 0.5 V, 60 mV step on CSx; measure at GATEx = 1.0 V	–	40	70	ns
Transient Response Time	Measured from CS_{REF} to GATEx, COMP = 2.1 V, $CSx = CS_{REF}$ = 0.5 V, CS_{REF} stepped from 1.2 V – 2.0 V	–	40	60	ns
Channel Start–Up Offset	$CSx = CS_{REF} = V_{FB}$ = 0 V, measure V_{COMP} when GATEx switch high	350	600	750	mV
Artificial Ramp Amplitude	50% Duty Cycle, Note 3	–	115	–	mV
Gates					
High Voltage	Measure GATEx I_{GATEx} = 1.0 mA	2.0	2.6	3.0	V
Low Voltage	Measure GATEx, I_{GATEx} = 1.0 mA	–	0.5	0.7	V

2. The V_{FB} Bias Current changes with the value of R_{OSC} per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.5\ V < V_{CC} < 14\ V$; $C_{GATEx} = 100\ pF$, $C_{COMP} = 0.01\mu F$, $C_{SS} = 0.1\mu F$, $C_{VCC} = 0.1\mu F$, $R_{ROSC} = 32.4\ k\Omega$, $V_{OCSET} = 0.54\ V$, DAC Code 01110; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Gates					
Rise Time	0.8 V < GATEx < 2.0 V, V_{CC} = 10 V	–	5.0	20	ns
Fall Time	2.0 V > GATEx > 0.8 V, V_{CC} = 10 V	–	5.0	20	ns
Oscillator					
Switching Frequency	$R_{OSC} = 32.4\ k\Omega$	300	400	500	kHz
Switching Frequency	$R_{OSC} = 63.4\ k\Omega$, Note 4	150	200	250	kHz
Switching Frequency	$R_{OSC} = 16.2\ k\Omega$, Note 4	600	800	1000	kHz
R_{OSC} Voltage		0.90	1.00	1.10	V
Phase Delay	–	75	90	105	deg
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CSx = CS_{REF}, V_{FB} = COMP, Measure V_{DRP} – COMP	–5.0	0	5.0	mV
Maximum V_{DRP} Voltage	CSx – CS_{REF} = 50 mV, V_{FB} = COMP, $T_A = 25°C$, Measure V_{DRP} – COMP	500	555	610	mV
Current Sense Input to V_{DRP} Gain	CSx – CS_{REF} = 50 mV, V_{FB} = COMP, $T_A = 25°C$, Measure V_{DRP} – COMP	2.5	2.78	3.05	V/V
Temperature Coefficient of V_{DRP} Gain	$\frac{(V@temp - V@room) \cdot 10^6}{\Delta T \cdot V@room}$	–	–685	–	ppm/°C
V_{DRP} Source Current Limit	CSx – CS_{REF} = 50 mV, V_{FB} = COMP, Measure V_{DRP} – COMP V_{DRP} = 1.5 V	1.0	7.0	14	mA
Soft Start					
SS Source Current	V_{CC} = 10 V	130	160	200	μA
SS Sink Current	V_{CC} = 7.0 V	4.0	5.0	6.25	μA
SS Min Threshold	V_{CC} = 10 V	0.25	0.3	0.35	V
SS Max Threshold	V_{CC} = 10 V	2.4	2.7	–	V
SS Source/Sink Ratio	–	20	32	48	–
SS COMP Pull Down Current	V_{CC} = 10 V	200	900	3000	μA
Current Sense Amplifiers					
CS_{REF} Input Bias Current	CS_{REF} = CSx = 0 V	–	3.4	4.0	μA
CSx Input Bias Current	CS_{REF} = CSx = 0 V	–	0.1	1.0	μA
Sense Amp Gain	CS_{REF} = 0 V, CSx = 0.05 V, Measure V(COMP) when GATEx switches high	–	2.65	–	V/V
Common Mode Input Range	Note 4	0	–	2.0	V
Bandwidth	–	–	7.0	–	MHz
Single Phase Pulse by Pulse Current Limit	$V_{FB} = CS_{REF}$ = 0.5 V, COMP = 2.0 V, Measure CSx – CS_{REF} when GATEx goes low	75	85	100	mV

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (0°C < T_A < 70°C; 0°C < T_J < 125°C; 9.5 V < V_{CC} < 14 V; C_{GATEx} = 100 pF, C_{COMP} = 0.01μF, C_{SS} = 0.1μF, C_{VCC} = 0.1μF, R_{ROSC} = 32.4 kΩ, V_{OCSET} = 0.54 V, DAC Code 01110; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Current Sense Amplifiers					
OCSET Input Bias Current	OCSET = 0 V	–	0.1	1.0	μA
Current Sense Input to OCSET Gain	OCSET/(CSx–CS_{REF}), 0.25 V < OCSET < 0.6 V, GATEx not switching	2.5	2.8	3.1	V/V
Current Limit Filter Slew Rate	CS_{REF} = 1.1 V, CSx = 1.0 V, pulse CSx to 1.16 V, Note 5.	2.0	5.0	13	mV/μs
General Electrical Specification					
V_{CC} Operating Current	COMP = 0.3 V (no switching)	–	20	30	mA
UVLO Start Threshold	SS Charging Gates Switching	8.5	9.0	9.5	V
UVLO Stop Threshold	Gates not switching, SS & COMP discharging	7.5	8.0	8.5	V
UVLO Hysteresis	Start–Stop	0.8	1.0	1.2	V

5. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

Pin Number	Pin Symbol	Pin Name	Function
1	GND	Ground	IC power supply return. Connected to IC substrate.
2	OCSET	Overcurrent Set	Resistor divider from R_{OSC} to GND. Programs the threshold of the hiccup overcurrent protection.
3	R_{OSC}	Oscillator Frequency Adjust	R_{OSC} is a regulated 1.0 V output and programs the oscillator frequency with a resistor to GND.
4–7	CS1–CS4	Current Sense Inputs	Non–inverting inputs to the current sense amplifiers.
8	CS_{REF}	Current Sense Reference	Inverting input to the current sense amplifiers and reference for Power Good.
9	V_{DRP}	Current Sense Amp Output	Programs the voltage drop due to loading. A resistor from V_{DRP} to FB programs the amount of Adaptive Voltage Positioning. Omitting this resistor defeats the AVP function.
10	V_{FB}	Voltage Feedback	Error Amplifier inverting input. Input bias current is used to program AVP light load offset via a resistor connected to the converter output voltage.
11	COMP	Error Amp Output and PWM Comparator Input	Provides loop compensation and is clamped by SS.
12	SS	Soft Start	Controls fault timing and startup.
13	PWRGD	Power Good Output	Open collector output, which is “low” when the converter output is out of regulation.
14	PWRGDS	Power Good Sense	A resistor divider from V_{OUT} to GND programs the Power Good lower threshold.
15–19	V_{ID4}–V_{ID0}	DAC V_{ID} Inputs	TTL–compatible logic input used to program the converter output voltage. Internal 50 kΩ pull–ups to 3.3 V via a blocking diode are provided. All high generates fault.
20–23	GATE4–1	Channel Outputs	PWM outputs to drive FET driver IC.
24	V_{CC}	Supply Input	IC bias input.

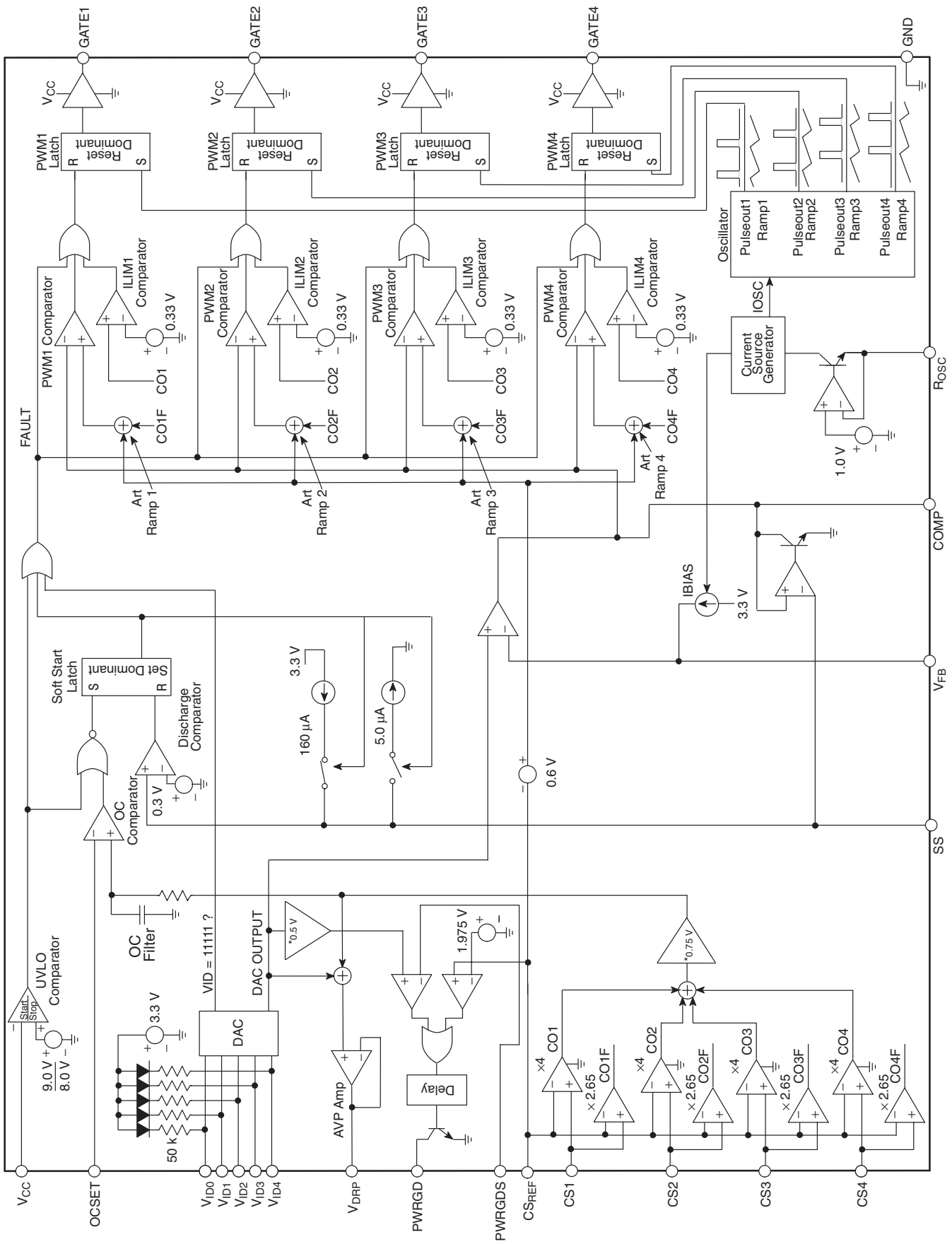


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

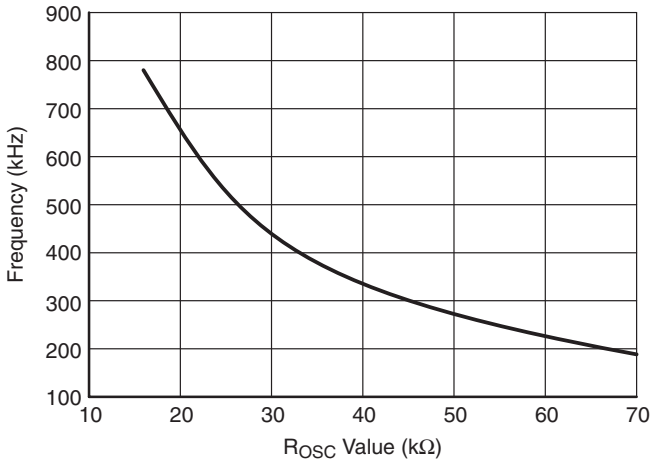


Figure 3. Oscillator Frequency

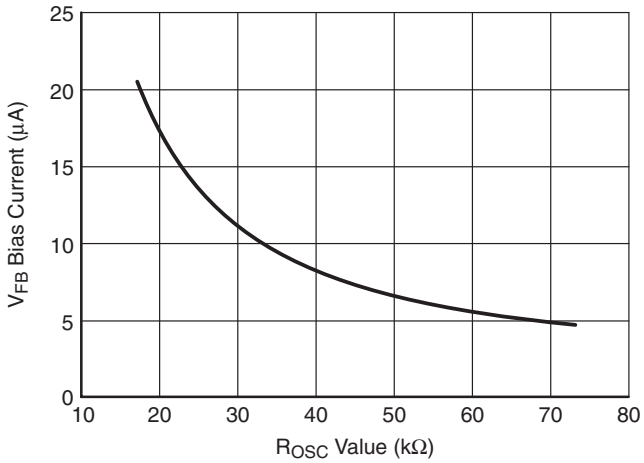


Figure 4. V_{FB} Bias Current vs. R_{OSC} Value

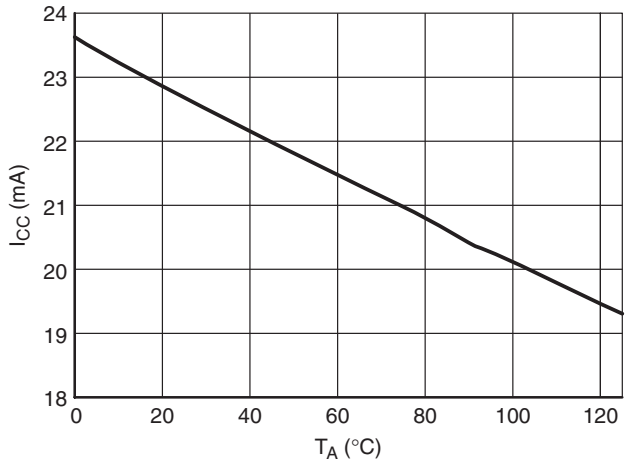


Figure 5. I_{CC} vs. Temperature

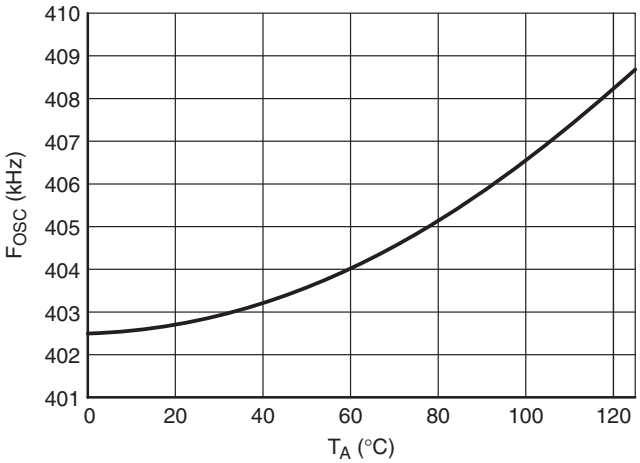


Figure 6. Oscillator Frequency vs. Temperature (R_{OSC} = 32.4 kΩ)

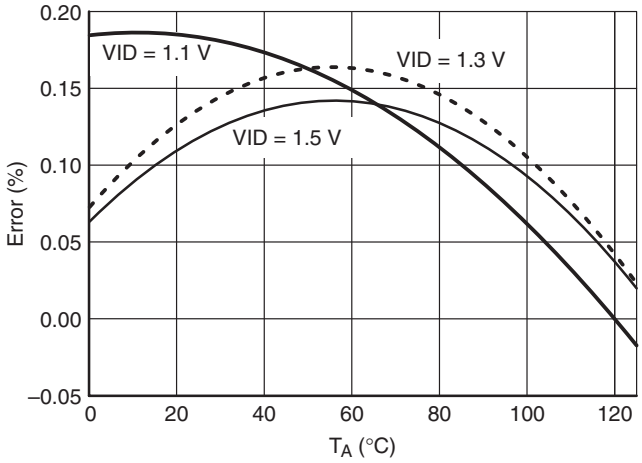


Figure 7. DAC Output Error vs. Temperature

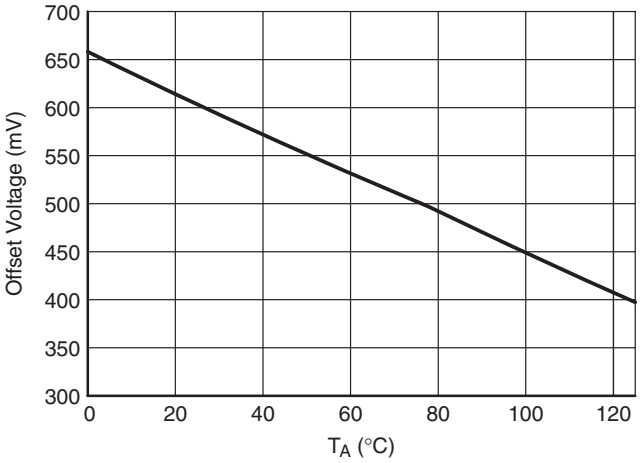


Figure 8. Current Sense Amplifier Channel Startup Offset Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

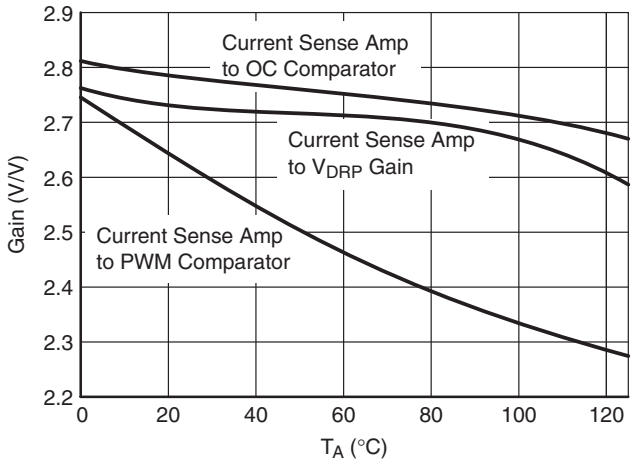


Figure 9. Sense Amp Gains vs. Temperature

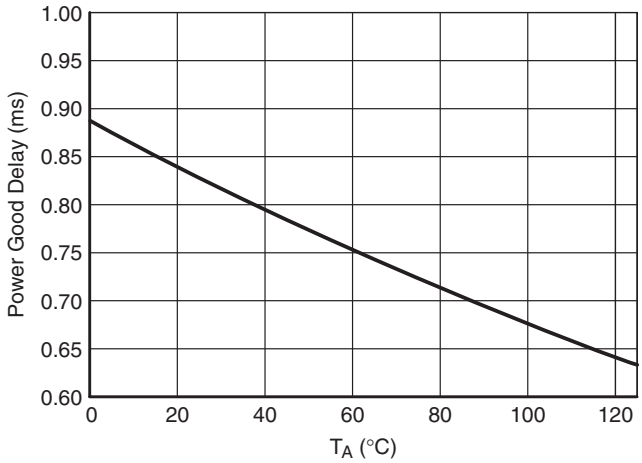


Figure 10. Power Good Delay vs. Temperature

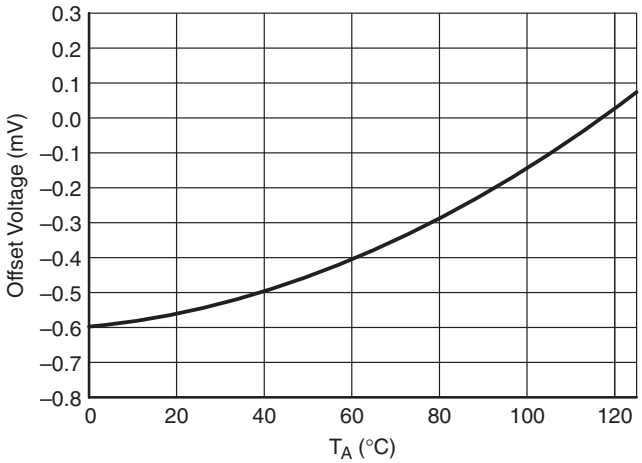


Figure 11. V_{DRP} to DAC Output Offset Voltage vs. Temperature

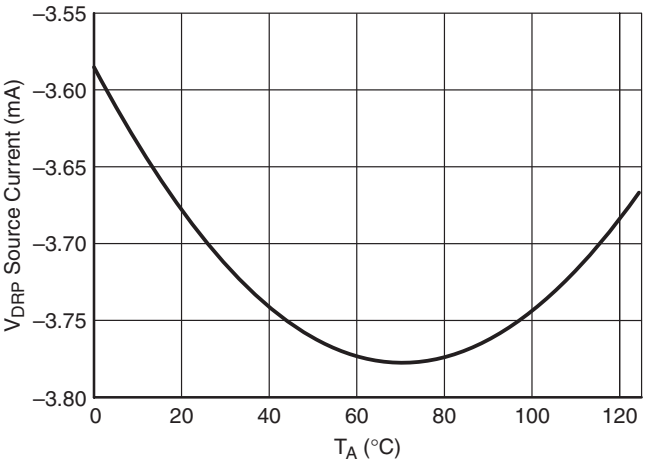


Figure 12. V_{DRP} Source Current vs. Temperature

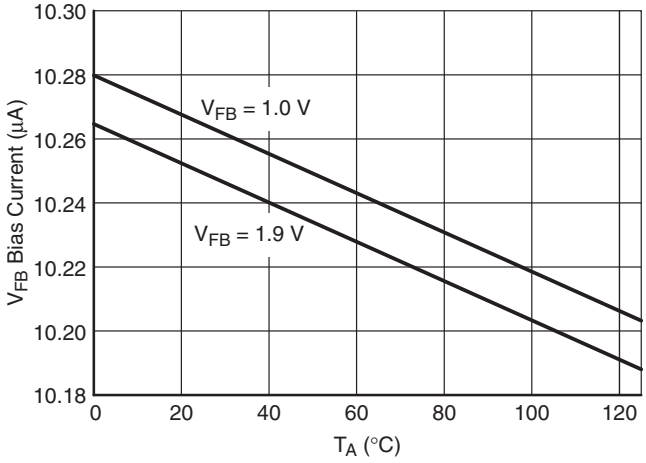


Figure 13. V_{FB} Bias Currents vs. Temperature (R_{OSC} = 32.4 kΩ)

APPLICATIONS INFORMATION

Overview

The CS5307 DC/DC controller from ON Semiconductor was developed using the Enhanced V^2 topology. Enhanced V^2 combines the original V^2 topology with peak current–mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast–feedback directly from Vcore has improved transient response and simplified design. The CS5307 includes Power Good (PWRGD), providing a highly integrated solution to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi–phase converter over a single–phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single–phase converter. The smaller inductor will produce larger ripple currents but the total per–phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off– time and the ripple voltage of the multi–phase converter will be less than that of a single–phase converter.

Fixed Frequency Multi–Phase Control

In a multi–phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5307 controller uses four–phase, fixed–frequency, Enhanced V^2 architecture to measure and control currents in individual phases. Each phase is delayed 90° from the previous phase. Normally, GATEx transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATEx low. Once GATEx goes low, it will remain low until the beginning of the next oscillator cycle. While GATEx is high, the Enhanced V^2 loop will respond to line and load variations. On the other hand, once GATEx is low, the loop cannot respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced V^2 will typically respond to disturbances within the off–time of the converter.

The Enhanced V^2 architecture measures and adjusts the output current in each phase. An additional input (CSx) for inductor current information has been added to the V^2 loop for each phase as shown in Figure 14. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the channel startup offset, the internal ramp and the output voltage at the non–inverting input of the PWM comparator. The purpose of the internal ramp is to compensate for propagation delays in the CS5307. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation and PWM duty cycles above 50% without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The CS5307 provides a CSx input for each phase, but the CS_{REF} and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same CS_{REF} and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.

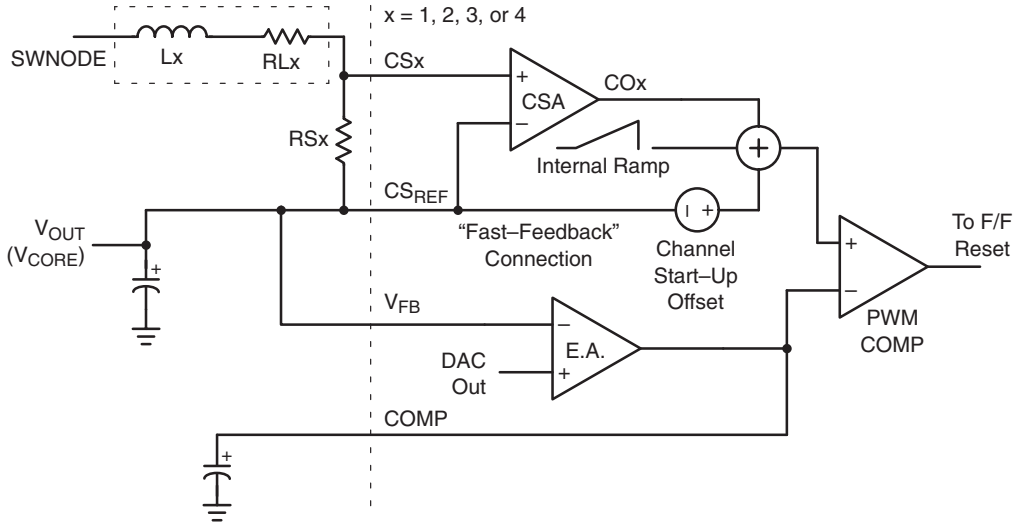


Figure 14. Enhanced V^2 Control Employing Resistive Current Sensing and Internal Ramp

Enhanced V^2 responds to disturbances in V_{CORE} by employing both “slow” and “fast” voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier’s external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in one or two PWM cycles. Fast voltage feedback is implemented by a direct connection from Vcore to the non–inverting pin of the PWM comparator via the summation with the inductor current, internal ramp and offset. A rapid increase in output current will produce a negative offset at Vcore and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty cycle in one PWM cycle.

As shown in Figure 14, an internal ramp (nominally 115 mV at a 50% duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty–cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $R_{CSx}C_{CSx}$ time constant of the feedback components from V_{CORE} to the CSx pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$V_{COMP} = V_{OUT} @ 0\ A + Channel\_Startup\_Offset + Int\_Ramp + G_{CSA} \cdot Ext\_Ramp/2$$

Int_Ramp is the “partial” internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak–to–peak external steady–state ramp at 0 A, G_{CSA} is the current sense amplifier gain (nominally 2.65 V/V) and the channel startup offset is typically 0.60 V. The magnitude of the Ext_Ramp can be calculated from:

$$Ext\_Ramp = D \cdot (V_{IN} - V_{OUT})/(R_{CSx} \cdot C_{CSx} \cdot f_{SW})$$

For example, if V_{OUT} at 0 A is set to 1.700 V with AVP and the input voltage is 12.0 V, the duty cycle (D) will be 1.700/12.0 or 14.2%. Int_Ramp will be 115 mV/50% · 14.2% = 33 mV. Realistic values for R_{CSx}, C_{CSx} and f_{SW} are 10 kΩ, 0.015 μF and 650 kHz. Using these and the previously mentioned formula, Ext_Ramp will be 15.0 mV.

$$V_{COMP} = 1.700\ V + 0.60\ V + 33\ mV + 2.65\ V/V \cdot 15.0\ mV/2 = 2.353\ Vdc.$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$\Delta V = R_S \cdot G_{CSA} \cdot \Delta I_{OUT}$$

The single–phase power stage output impedance is:

$$\text{Single Stage Impedance} = \Delta V_{OUT}/\Delta I_{OUT} = R_S \cdot G_{CSA}$$

The total output impedance will be the single stage impedance divided by 4.

The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:

$$I_{OUT,PEAK} = (V_{COMP} - V_{OUT} - Offset)/(R_S \cdot G_{CSA})$$

Figure 15 shows the step response of the COMP pin at a fixed level. Before T1, the converter is in normal steady–state operation. The inductor current provides a portion of the PWM ramp through the current sense amplifier. The PWM cycle ends when the sum of the current ramp, the “partial” internal ramp voltage signal and offset exceed the level of the COMP pin. At T1, the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the V_{FB} pin and the cycle ends at T2. After T2, the output voltage remains lower than at light load and the average current signal level (CSx output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system, the COMP pin would move higher to restore the output voltage to the original level.

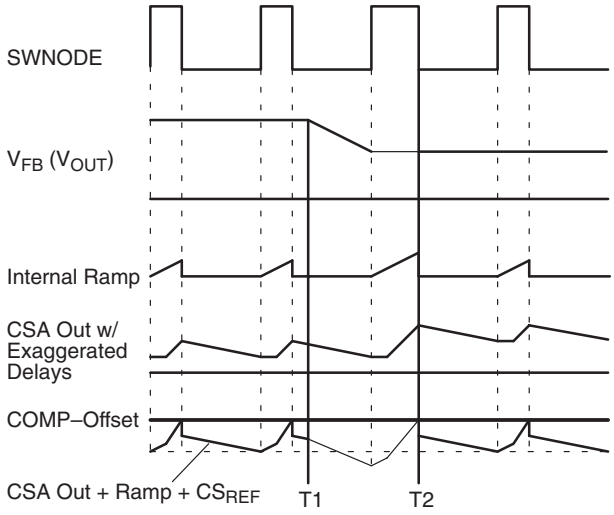


Figure 15. Open Loop Operation

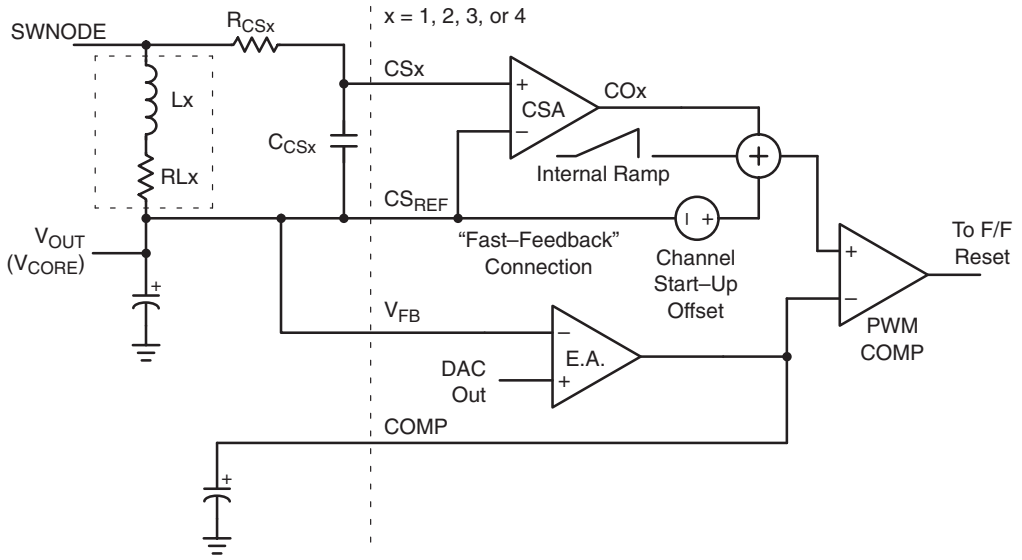


Figure 16. Enhanced V^2 Control Employing Lossless Inductive Current Sensing and Internal Ramp

Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 16. In the diagram, L is the output inductance and R_L is the inherent inductor resistance. To compensate the current sense signal, the values of R_{CSx} and C_{CSx} are chosen so that $L/R_L = R_{CSx} \cdot C_{CSx}$. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSx will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value R_L was used.

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per °C. The increase in winding resistance at higher temperatures should be considered when setting the OCSET threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 14.

Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the CS_{REF} pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSx input and the CS_{REF} input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case CSA input mismatch is ±10 mV and will typically be within 4.0 mV. The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance, a 3.0 mV mismatch with a 2.0 mΩ sense resistance will produce a 1.5 A difference in current between phases.

External Ramp Size and Current Sensing

The internal ramp allows flexibility in setting the current sense time constant. Typically, the current sense $R_{CSx} \cdot C_{CSx}$ time constant should be equal to or slightly slower than the inductor's time constant. If RC is chosen to be smaller (faster) than L/R_L, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady–state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $R_{CSx} \cdot C_{CSx}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $R_{CSx} \cdot C_{CSx}$. If this error is excessive, it will affect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the V_{DRP} signal will overshoot which will produce too much transient droop in the output voltage. The single–phase pulse–by–pulse overcurrent protection will trip earlier than it would if compensated correctly and hiccup–mode current limit will have a lower threshold for fast rising step loads than for slowly rising output currents.

The waveforms in Figure 17 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of L = 500 nH, R_L = 1.6 mΩ, R_{CSx} = 20 kΩ and C_{CSx} = .01 µF. In this case, ideal current signal compensation would require R_{CSx} to be 31 kΩ.

Due to the faster than ideal RC time constant, there is an overshoot of 50% and the overshoot decays with a 200 μs time constant. With this compensation, the OCSET pin threshold must be set more than 50% above the full load current to avoid triggering current limit during a large output load step.

Transient Response and Adaptive Voltage Positioning

For applications with fast transient currents, the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak–peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications, a droop resistor can provide fast, accurate adaptive positioning. However, at high currents, the loss in a droop resistor becomes excessive. For example, a 50 A converter with a 1 mΩ resistor would provide a 50 mV change in output voltage between no load and full load and would dissipate 2.5 W.

Lossless adaptive voltage positioning (AVP) is an alternative to using a droop resistor, but it must respond to changes in load current. Figure 18 shows how AVP works. The waveform labeled “normal” shows a converter without AVP. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) AVP, the peak–to–peak excursions are cut in half. In the slow AVP waveform, the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.

The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 1). To set the no–load positioning, a resistor is placed between the output voltage and V_{FB} pin. The V_{FB} bias current will develop a voltage across the resistor to adjust the no–load output voltage. The V_{FB} bias current is dependent on the value of R_{OSC} as shown in the datasheets.

During no–load conditions, the V_{DRP} pin is at the same voltage as the V_{FB} pin, so none of the V_{FB} bias current flows through the V_{DRP} resistor. When output current increases, the V_{DRP} pin voltage increases proportionally. Current set by the V_{DRP} resistor offsets the V_{FB} bias current, causing the output voltage to decrease.

The response during the first few microseconds of a load transient is controlled primarily by power stage output impedance, and by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow, there will be a long transition to the final voltage after a transient. This will be most apparent with low capacitance output filters.

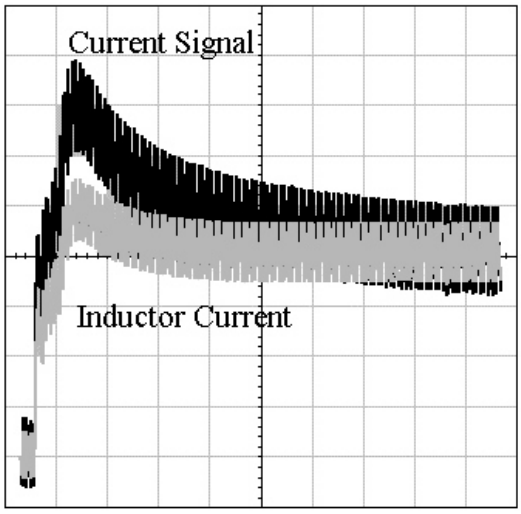


Figure 17. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant (50 μs/div)

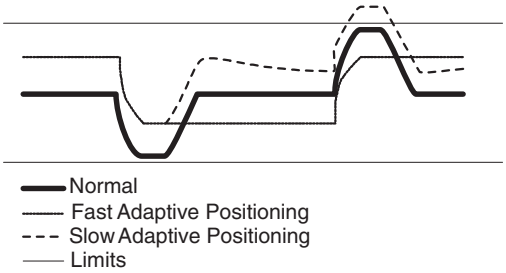


Figure 18. Adaptive Voltage Positioning

Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced V^2 control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 40 ns, causing the GATEx output to shut off. The (external) MOSFET driver should react normally to turn off the top MOSFET and turn on the bottom MOSFET. This results in a “crowbar” action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ends or the input voltage is pulled low.

Power Good

According to the latest specifications, the Power Good (PWRGD) signal must be asserted when the output voltage is within a window defined by the VID code, as shown in Figure 19.

The PWRGDS pin is provided to allow the PWRGD comparators to accurately sense the output voltage. The effect of the PWRGD lower threshold can be modified using a resistor divider from the output to PWRGDS to ground, as shown in Figure 20.

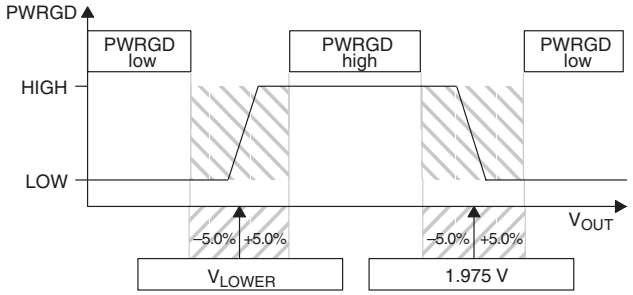


Figure 19. PWRGD Assertion Window

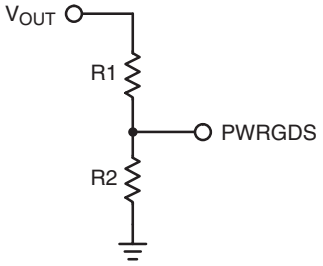


Figure 20. Adjusting the PWRGD Threshold

Since the internally–set thresholds for PWRGDS are VID/2 for the lower threshold and a fixed 1.975V for the upper threshold, a simple equation can be provided to assist the designer in selecting a resistor divider to provide the desired PWRGD performance.

$$V_{LOWER} = \frac{V_{VID}}{2} \cdot \frac{R_1 + R_2}{R_1}$$

$$V_{UPPER} = 1.975\ V$$

The logic circuitry inside the chip sets PWRGD low only after a delay period has been passed. A “power bad” event does not cause PWRGD to go low unless it is sustained through the delay time of 500 µs. If the anomaly disappears before the end of the delay, the PWRGD output will never be set low.

In order to use the PWRGD pin as specified, the user is advised to connect external resistors as necessary to limit the current into this pin to 4 mA or less.

Undervoltage Lockout

The CS5307 includes an undervoltage lockout circuit. This circuit keeps the IC’s output drivers low until V_{CC} applied to the IC reaches 9 V. The GATE outputs are disabled when V_{CC} drops below 8 V.

Soft Start and Hiccup Mode

At initial power–up, both SS and COMP voltages are zero. The total SS capacitance will begin to charge with a current of 160 µA. The error amplifier directly charges the COMP capacitance. An internal clamp ensures that the COMP pin voltage will always be less than the voltage at the SS pin, ensuring proper start–up behavior. All GATE outputs are held low until the COMP voltage reaches 0.6 V. Once this threshold is reached, the GATE outputs are released to operate normally. In current limit, the internal fault latch will initiate a 5 µA discharge current on the SS pin, and the internal clamp will discharge the capacitor connected to the COMP pin at a similar rate. This performance will result in GATE pulses being generated until the overcurrent condition reoccurs and the discharge/soft start cycle begins anew.

Current Limit

Two levels of over–current protection are provided. First, if the voltage on the Current Sense pins (CSx) exceeds CS_{REF} by more than a fixed threshold (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and low–pass filtered to compare an averaged current signal to a user adjustable voltage on the OCSET pin. If the OCSET voltage is exceeded, the fault latch trips and the Soft Start capacitor discharges until the Soft Start pin reaches 0.3 V. Then Soft Start begins. The converter will continue to operate in a low average current hiccup–mode until the fault condition is corrected.

Fault Protection Logic

The CS5307 includes fault protection circuitry to prevent harmful modes of operation from occurring. The fault logic is described in Table 1.

Gate Outputs

The CS5307 is designed to operate with external gate drivers. Accordingly, the gate outputs are capable of driving a 100 pF load with typical rise and fall times of 5 ns.

Digital to Analog Converter (DAC)

The output voltage of the CS5307 is set by means of a 5–bit, 1% DAC. The DAC pins are internally pulled up to a 3.3 V rail through a blocking diode and a set of 50 kΩ resistors. The blocking diode allows external pull up to a bias voltage greater than 3.3 V and less than 13 V.

The output of the DAC is described in the Electrical Characteristics section of the data sheet. These outputs are consistent with the latest VRM and processor specifications. The DAC output is equal to the VID code specification.

In order to produce a workable power supply using the CS5307, the designer is expected to use AVP as described earlier to position the output voltage above the DAC output, resulting in an output voltage somewhere in the middle of the acceptable range.

Table 1. Fault Protection Logic

Fault Modes	Stop Switching	SS Pin Characteristics	Reset Method
Undervoltage Lockout	Yes	–5.0 μA	SS < 0.3 V
VID–11111	Yes	–5.0 μA	Change VID Code
Phase Over Current (0.33 V Limit)	No	Not Affected	Automatic

The latest VRM and processor specifications require a power supply to turn its output off in the event of a 11111 VID code. When the DAC sees such a code, the GATE pins stop switching and go low. This condition is described in Table 1.

Design Procedure

1. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide "hold up" during transient loading. The low impedance capacitors reduce steady–state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ($N_{OUT,MIN}$):

$$N_{OUT,MIN} = \text{ESR per capacitor} \cdot \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad (1)$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to:

$$\Delta V_{O,MAX} = (\Delta I_{O,MAX}/\Delta t) \cdot ESL + \Delta I_{O,MAX} \cdot ESR \quad (2)$$

Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

2. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady–state and transient performance of the converter. When selecting an inductor, the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size and cost (usually the primary concern).

In general, the output inductance value should be elecrrically and physically as small as possible to provide the best transient response at minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc.) resulting in increased dissipation and lower converter efficiency. Increased ripple currents force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors, adversely affecting converter cost.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current (α) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the selected maximum ripple current.

$$L_{OMIN} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{(\alpha \cdot I_{O,MAX} \cdot V_{IN} \cdot f_{SW})} \quad (3)$$

α is the ripple current as a percentage of the maximum output current *per phase* (α = 0.15 for ±15%, α = 0.25 for ±25%, etc.). If the minimum inductor value is used, the inductor current will swing ± α% about its value at the center. Therefore, for a four–phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha) \cdot I_{O,MAX}/4$.

The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response, the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required and the converter cost will be increased. For a given inductor value, it is useful to determine the times required to increase or decrease the current.

For increasing current:

$$\Delta t_{INC} = Lo \cdot \Delta I_O/(V_{IN} - V_{OUT}) \quad (3.1)$$

For decreasing current:

$$\Delta t_{DEC} = Lo \cdot \Delta IO/(V_{OUT}) \quad (3.2)$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. Thus, it may be more difficult for the converter to stay within the regulation limits when the load is removed than when it is applied and excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lo_{MIN}), the number of output capacitors ($N_{OUT,MIN}$) and the per capacitor ESR determined in the previous Section:

$$V_{OUT,P-P} = (\text{ESR per cap} / N_{OUT,MIN}) \cdot [(V_{IN} - \#Phases \cdot V_{OUT}) \cdot D / (Lo_{MIN} \cdot f_{SW})] \quad (4)$$

This formula assumes steady–state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the "time summation" of the four individual phase currents that are 90 degrees out–of–phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi–phase converter.

3. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors, one must first determine the total RMS input ripple current. To this end, begin by calculating the average input current to the converter:

$$I_{IN,AVG} = I_{O,MAX} \cdot D/\eta \quad (5)$$

where:

D is the duty cycle of the converter, $D = V_{OUT}/V_{IN}$;

η is the specified minimum efficiency;

$I_{O,MAX}$ is the maximum converter output current.

The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 21.

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$I_{C,MAX} = I_{Lo,MAX}/\eta - I_{IN,AVG} \quad (6)$$

$$I_{C,MIN} = I_{Lo,MIN}/\eta - I_{IN,AVG} \quad (7)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/4 + \Delta I_{Lo}/2 \quad (8)$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/4 - \Delta I_{Lo}/2 \quad (9)$$

ΔI_{Lo} is the peak–to–peak ripple current in the output inductor of value Lo:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (10)$$

For the four–phase converter, the input capacitor(s) RMS current is then:

$$I_{CIN,RMS} = [4D \cdot (I_{C,MIN}^2 + I_{C,MIN} \cdot \Delta I_{C,IN} + \Delta I_{C,IN}^2/3) + I_{IN,AVG}^2 \cdot (1 - 4D)]^{1/2} \quad (11)$$

Select the number of input capacitors (N_{IN}) to provide the RMS input current ($I_{CIN,RMS}$) based on the RMS ripple current rating per capacitor ($I_{RMS,RATED}$):

$$N_{IN} = I_{CIN,RMS}/I_{RMS,RATED} \quad (12)$$

For a four–phase converter with perfect efficiency ($\eta = 1$), the worst case input ripple–current will occur when the converter is operating at a 12.5% duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to 12.5% of the converter's DC output current. At other duty cycles, the ripple–current will be less. For example, at a duty cycle of either 6% or 19%, the four–phase input ripple–current will be approximately 10% of the converter's DC output current.

In general, capacitor manufacturers require derating to the specified ripple–current based on the ambient temperature. More capacitors will be required because of the current derating. The designer should know the ESR of the input capacitors. The input capacitor power loss can be calculated from:

$$P_{CIN} = I_{CIN,RMS}^2 \cdot ESR\_per\_capacitor/N_{IN} \quad (13)$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced 50% for every 10°C rise in the capacitor's temperature.

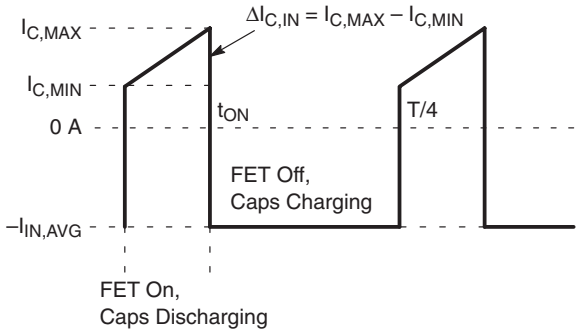


Figure 21. Input Capacitor Current for a Four–Phase Converter

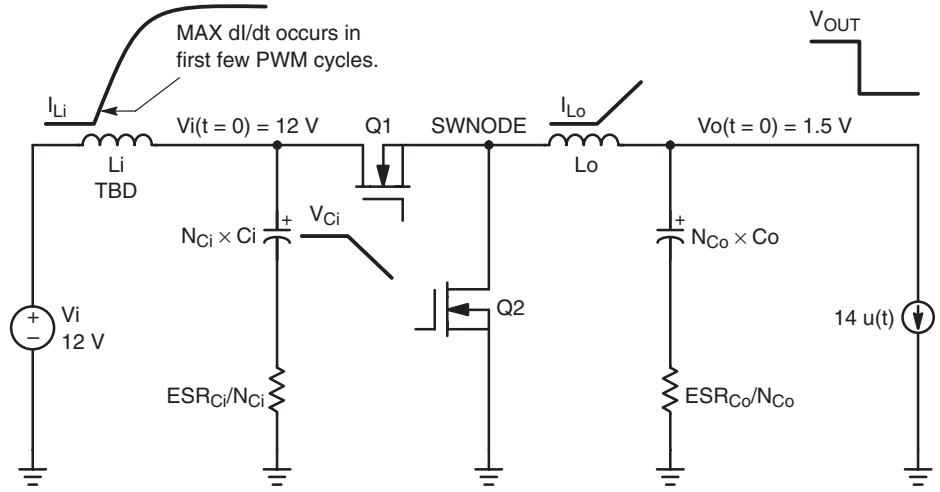


Figure 22. Calculating the Input Inductance

4. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents reduce the expected life of the input capacitors. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients.

The worst case input current slew rate will occur during the first few PWM cycles immediately after a step–load change is applied as shown in Figure 22. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously, so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ($I_{O,MAX}$), the per capacitor ESR of the output capacitors (ESR_{OUT}) and the number of the output capacitors (N_{OUT}) as shown in Figure 22. Assuming the load current is shared equally between the four phases, the output voltage at full transient load will be:

$$V_{OUT,FULL-LOAD} = V_{OUT,NO-LOAD} - (I_{O,MAX}/4) \cdot ESR_{OUT}/N_{OUT} \quad (14)$$

When the control MOSFET (Q1 in Figure 22) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$\Delta V_{Lo} = V_{IN} - V_{OUT,FULL-LOAD} = V_{IN} - V_{OUT,NO-LOAD} + (I_{O,MAX}/4) \cdot ESR_{OUT}/N_{OUT} \quad (15)$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$dI_{Lo}/dt = \Delta V_{Lo}/Lo \quad (16)$$

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors (ΔV_{Ci}) is determined by the number of input capacitors (N_{IN}), their per capacitor ESR (ESR_{IN}) and the current in the output inductor according to:

$$\Delta V_{Ci} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot t_{ON} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot D/f_{SW} \quad (17)$$

Before the load is applied, the voltage across the input inductor (V_{Li}) is very small and the input capacitors charge to the input voltage V_{IN}. After the load is applied, the voltage drop across the input capacitors, ΔV_{Ci}, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from:

$$Li_{MIN} = V_{Li} / dI_{IN}/dt_{MAX} = \Delta V_{Ci} / dI_{IN}/dt_{MAX} \quad (18)$$

dI_{IN}/dt_{MAX} is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very "stiff" and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer's data sheets are worst case high limits. In reality, input voltage "sag," lower capacitor ESRs and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the inductor. Also, for an inexpensive iron powder core, such as the –26 or –52 from Micrometals, the inductance "swing" with DC bias must be taken into account and inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the dI/dt will be higher than expected.

5. MOSFET & Heatsink Selection

Power dissipation, package size and thermal requirements drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non–overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$P_{D,CONTROL} = (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \quad (19)$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the loss associated with the *control and synchronous* MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET. The first two terms are usually adequate to predict the majority of the losses.

$I_{RMS,CNTL}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$I_{RMS,CNTL} = \sqrt{D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (20)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/4 + \Delta I_{Lo}/2 \quad (21)$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/4 - \Delta I_{Lo}/2 \quad (22)$$

$I_{O,MAX}$ is the maximum converter output current.

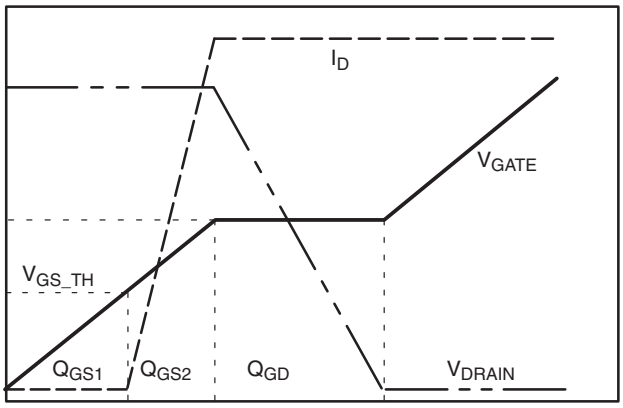


Figure 23. MOSFET Switching Characteristics

D is the duty cycle of the converter:

$$D = V_{OUT}/V_{IN} \quad (23)$$

ΔI_{Lo} is the peak–to–peak ripple current in the output inductor of value L_o:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (24)$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate–to–source charge plus the gate–to–drain charge. This may be specified in the data sheet or approximated from the gate–charge curve as shown in the Figure 23.

$$Q_{switch} = Q_{gs2} + Q_{gd} \quad (25)$$

I_g is the output current from the gate driver IC.
V_{IN} is the input voltage to the converter.
f_{sw} is the switching frequency of the converter.
Q_G is the MOSFET total gate charge to obtain $R_{DS(on)}$. Commonly specified in the data sheet.
V_g is the gate drive voltage.
Q_{RR} is the reverse recovery charge of the *lower* MOSFET.
Q_{oss} is the MOSFET output charge specified in the data sheet.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) + (Vf_{diode} \cdot I_{O,MAX}/4 \cdot t\_nonoverlap \cdot f_{SW}) \quad (26)$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non–overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = \sqrt{1 - D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (27)$$

where:

Vf_{diode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.

t_nonoverlap is the non–overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature.

$$\theta_T < (T_J - T_A)/P_D \quad (28)$$

where:

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$);

θ_{JC} is the junction–to–case thermal impedance of the MOSFET;

θ_{SA} is the sink–to–ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used);

T_J is the specified maximum allowed junction temperature;

T_A is the worst case ambient operating temperature.

For TO–220 and TO–263 packages, standard FR–4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

Pad Size (in^2/mm^2)	Single–Sided 1 oz. Copper
0.50/323	60–65°C/W
0.75/484	55–60°C/W
1.00/645	50–55°C/W
1.50/968	45–50°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading and component variations (i.e., worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, it is advisable to have as much heatsink area as possible. All too often, new designs are found to be too hot and require re–design to add heatsinking.

6. Adaptive Voltage Positioning

There are two resistors that determine the Adaptive Voltage Positioning: R_{FB} and R_{DRP}. R_{FB} establishes the no–load "high" voltage position and R_{DRP} determines the full–load "droop" voltage.

Resistor R_{FB} is connected between V_{CORE} and the V_{FB} pin of the controller. At no load, this resistor will conduct the internal bias current of the V_{FB} pin and develop a voltage drop from V_{CORE} to the V_{FB} pin. Because the error amplifier regulates V_{FB} to the DAC setting, the output voltage, V_{CORE}, will be lower by the amount $IBIAS_{VFB} \cdot R_{FB}$. This condition is shown in Figure 24.

To calculate R_{FB}, the designer must specify the no–load voltage decrease below the VID setting ($\Delta V_{NO–LOAD}$) and determine the V_{FB} bias current. Usually, the no–load voltage increase is specified in the design guide for the processor that is available from the manufacturer. The V_{FB} bias current is determined by the value of the resistor from R_{OSC} to ground (see Figure 4 in the data sheet for a graph of $IBIAS_{VFB}$ versus R_{OSC}). The value of R_{FB} can then be calculated:

$$R_{FB} = \Delta V_{NO–LOAD}/IBIAS_{VFB} \quad (29)$$

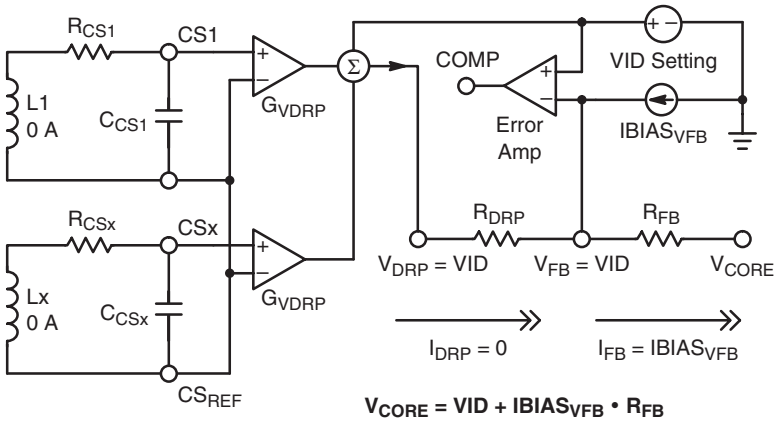
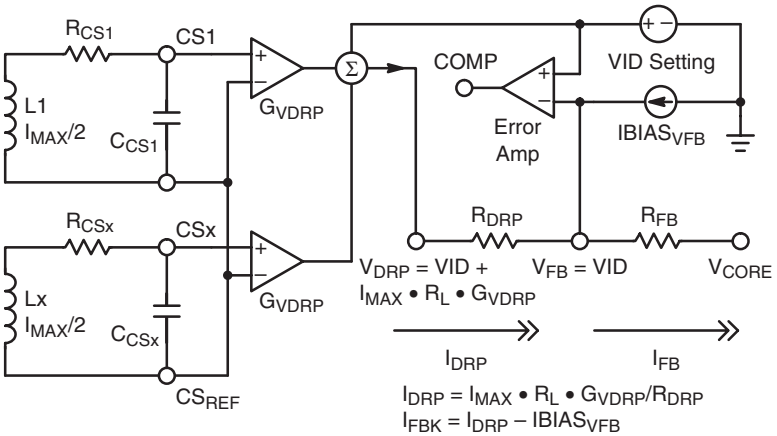


Figure 24. AVP Circuitry at No–Load



$$V_{CORE} = VID - (I_{DRP} - IBIAS_{VFB}) \cdot R_{FB}$$
$$= VID - I_{MAX} \cdot R_L \cdot G_{VDRP} \cdot R_{FB}/R_{DRP} + IBIAS_{VFB} \cdot R_{FB}$$

Figure 25. AVP Circuitry at Full–Load

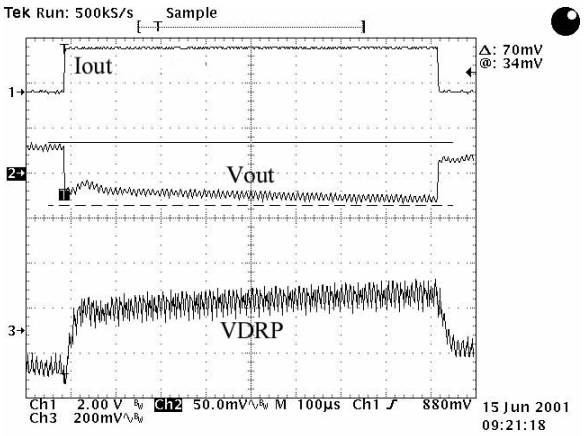


Figure 26. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Long (Slow): V_{DRP} and V_{OUT} Respond Too Slowly.

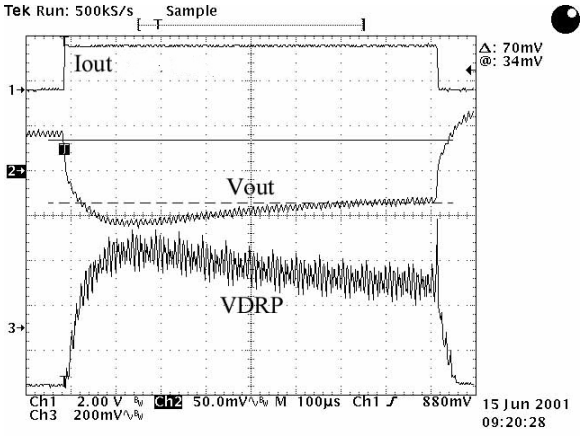


Figure 27. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Short (Fast): V_{DRP} and V_{OUT} Both Overshoot.

Resistor R_{DRP} is connected between the V_{DRP} and the V_{FB} pins. At no–load, the V_{DRP} and the V_{FB} pins will both be at the DAC voltage. This resistor will conduct zero current. However, at full–load, the voltage at the V_{DRP} pin will increase proportional to the output inductor's current while V_{FB} will still be regulated to the DAC voltage. Current will be conducted from V_{DRP} to V_{FB} by R_{DRP}. This current will be large enough to supply the V_{FB} bias current and cause a voltage drop from V_{FB} to V_{CORE} across R_{FB}. The converter's output voltage will be reduced. This condition is shown in Figure 25.

To determine the value of R_{DRP}, the designer must specify the full–load voltage reduction *from the VID* (DAC) setting ($\Delta V_{OUT,FULL–LOAD}$) and predict the voltage increase at the V_{DRP} pin at full–load. Usually, the full–load voltage reduction is specified in the design guide for the processor that is available from the manufacturer. To predict the voltage increase at the V_{DRP} pin at full–load (ΔV_{DRP}), the designer must consider the output inductor's resistance (R_L), the PCB trace resistance between the current sense points (R_{PCB}) and the controller IC's gain from the current sense to the V_{DRP} pin (G_{VDRP}):

$$\Delta V_{DRP} = I_{O,MAX} \cdot (R_L + R_{PCB}) \cdot G_{VDRP} \quad (30)$$

The value of R_{DRP} can then be calculated:

$$R_{DRP} = \frac{\Delta V_{DRP}}{(IBIAS_{VFB} + \Delta V_{OUT,FULL–LOAD}/R_{FB})} \quad (31)$$

$\Delta V_{OUT,FULL–LOAD}$ is the full–load voltage reduction from the VID (DAC) setting. $\Delta V_{OUT,FULL–LOAD}$ is *not* the voltage change from the no–load AVP setting.

7. Current Sensing

For inductive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3, or 4) to satisfy

$$R_{CSx} \cdot C_{CSx} = Lo/(R_L + R_{PCB}) \quad (32)$$

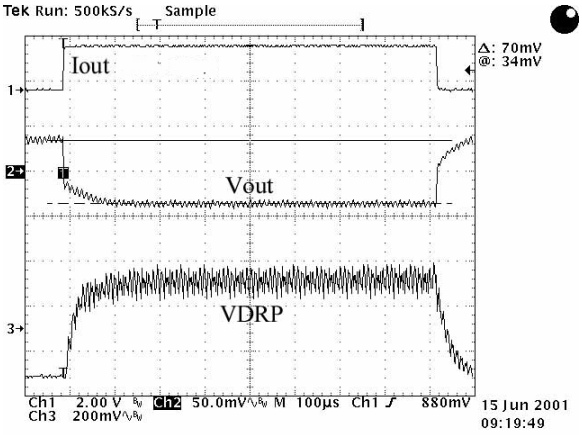


Figure 28. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Optimal: V_{DRP} and V_{OUT} Respond to the Load Current Quickly Without Overshooting.

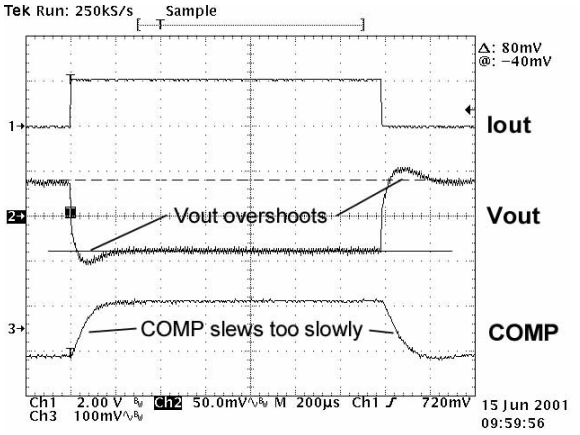


Figure 29. The Value of C_{AMP} Is Too High and the Loop Gain/Bandwidth Too Low. COMP Slews Too Slowly Which Results in Overshoot in V_{OUT}.

For resistive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3, or 4) to satisfy

$$R_{CSx} \cdot C_{CSx} = Lo/(R_{sense}) \quad (33)$$

This will provide an adequate starting point for R_{CSx} and C_{CSx}. After the converter is constructed, the value of R_{CSx} (and/or C_{CSx}) should be fine–tuned in the lab by observing the V_{DRP} signal during a step change in load current. Tune the $R_{CSx} \cdot C_{CSx}$ network to provide a "square–wave" at the V_{DRP} output pin with maximum rise time and minimal overshoot as shown in Figure 28.

8. Error Amplifier Tuning

After the steady–state (static) AVP has been set and the current sense network has been optimized, the Error Amplifier must be tuned. The gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor (C_{AMP} in the Applications Diagram). The bandwidth of the control loop will vary directly with the gain of the error amplifier.

If C_{AMP} is too large, the loop gain/bandwidth will be low, the COMP pin will slew too slowly and the output voltage will overshoot as shown in Figure 29. On the other hand, if C_{AMP} is too small, the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot will occur. Integrator "wind up" is the cause of the overshoot. In this case, the output voltage will transition more slowly because COMP spikes upward as shown in Figure 30. Too much loop gain/bandwidth increases the risk of instability. In general, one should use the lowest loop gain/bandwidth possible to achieve acceptable transient response. This will insure good stability. If C_{AMP} is optimal, the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 32.

After the control loop is tuned to provide an acceptable transient response, the steady–state voltage ripple on the COMP pin should be examined. When the converter is operating at full steady–state load, the peak–to–peak voltage ripple (V_{PP}) on the COMP pin should be less than 20 mV_{PP} as shown in Figure 31. Less than 10 mV_{PP} is ideal. Excessive ripple on the COMP pin will contribute to jitter.

9. Current Limit Setting

When the output of the current sense amplifier (COx in the block diagram) exceeds the voltage on the I_{LIM} pin, the part will enter hiccup mode. For inductive sensing, the OCSET pin voltage should be set based on the inductor's maximum resistance (R_{LMAX}). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is +0.39% per °C. If using a current sense resistor (R_{SENSE}), the OCSET pin voltage should be set based on the maximum value of the sense resistor. To set the level of the OCSET pin:

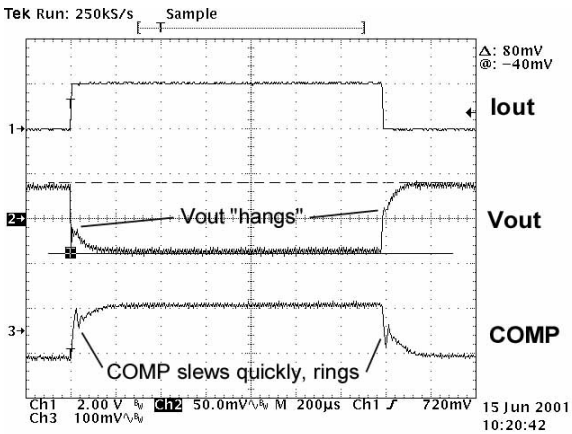


Figure 30. The Value of C_{AMP} Is Too Low and the Loop Gain/Bandwidth Too High. COMP Moves Too Quickly, Which Is Evident from the Small Spike in Its Voltage When the Load Is Applied or Removed. The Output Voltage Transitions More Slowly Because of the COMP Spike.

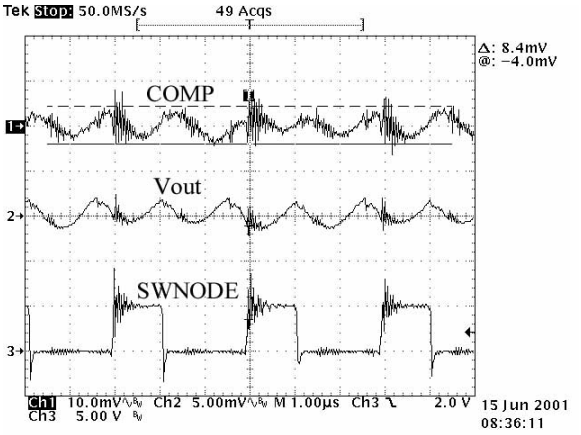


Figure 31. At Full–Load the Peak–to–Peak Voltage Ripple on the COMP Pin Should Be Less than 20 mV for a Well–Tuned/Stable Controller. Higher COMP Voltage Ripple Will Contribute to Output Voltage Jitter.

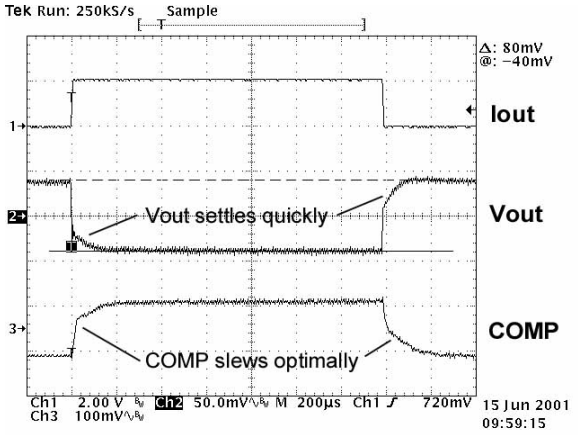


Figure 32. The Value of C_{AMP} Is Optimal. COMP Slews Quickly Without Spiking or Ringing. V_{OUT} Does Not Overshoot and Monotonically Settles to Its Final Value.

$$V_{OCSET} = (I_{OUT,LIM} + \Delta I_{Lo}/2) \cdot R \cdot G_{ILIM} \quad (34)$$

where:

$I_{OUT,LIM}$ is the current limit threshold of the converter;

$\Delta I_{Lo}/2$ is half the inductor ripple current;

R is either (R_{LMAX} + R_{PCB}) or R_{SENSE};

G_{ILIM} is the current sense to OCSET gain.

For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the R_L time constant. If the RC time constant is too fast, a step load change will cause the sensed current waveform to appear larger than the actual inductor current and will trip the current limit at a lower level than expected.

10. PWM Comparator Input Voltage

The voltage at the positive input terminal of the PWM comparator (see Figure 14 or 16) is limited by the internal voltage supply of the controller (3.3 V), the size of the internal ramp and the magnitude of the channel startup offset voltage. To prevent the PWM comparator from saturating, the differential input voltage from CS_{REF} to CSn (n = 1, 2, 3, or 4) must satisfy the following equation:

$$V_{CSREF,MAX} + V_{COx,MAX} + 600\ mV \cdot D \le 2.45\ V \quad (35)$$

where:

$V_{CSREF,MAX}$ = Max VID Setting w/ AVP @ Full Load

$$V_{COn,MAX} = [V_{CSx} - V_{CSREF}] \cdot G_{CSA,MAX} = (I_{O,MAX}/2 + \Delta I_{Lo}/2) \cdot R_{MAX} \cdot G_{CSA,MAX}$$

R_{MAX} = R_{SENSE} or ($R_{L,MAX}$ + $R_{PCB,MAX}$)

11. Soft Start Time

The Soft Start time (T_{SS}) can be calculated from:

$$T_{SS} = C_{SS} \cdot \frac{\Delta V}{I_{SS}} = C_{SS} \cdot \frac{V_{COMP} - Channel\_Startup\_Offset}{160\ \mu A} \quad (36)$$

where:

$$V_{COMP} = V_{OUT}\ @\ 0\ A + Channel\_Startup\_Offset + Int\_Ramp + G_{CSA} \cdot Ext\_Ramp/2$$

$$= 2.353\ V_{dc}\ (from\ page\ 12)$$

If C_{SS} = 0.1 µF, then the Soft Start time will be:

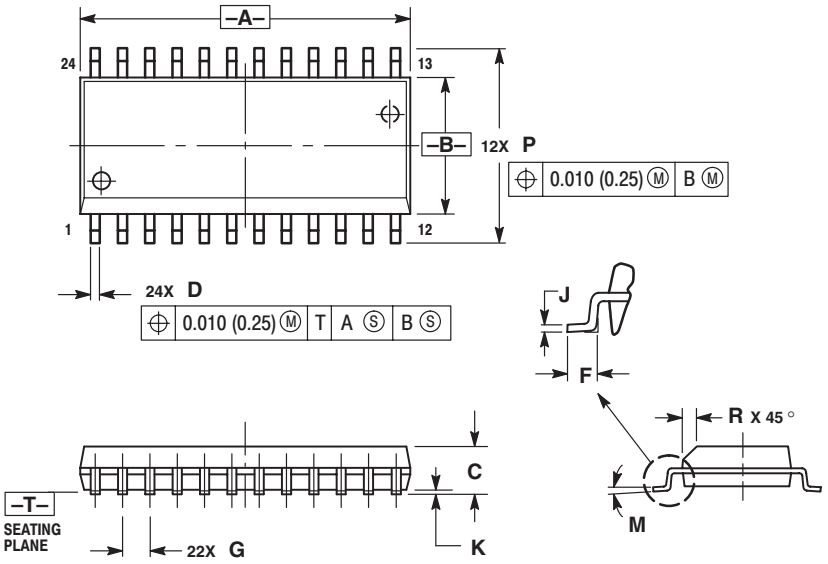
$$T_{SS} = 0.1\ \mu F \cdot \frac{1.753\ V_{dc}}{160\ \mu A} = 1.1\ ms \quad (37)$$

The Channel_Startup_Offset is subtracted from V_{COMP} as the output does not begin to rise until V_{COMP} exceeds this voltage. As the internal and external ramp values are small, the Soft Start time may be approximated by:

$$T_{SS} = C_{SS} \cdot \frac{V_{OUT}\ @\ 0\ A}{I_{SS}} \quad (38)$$

PACKAGE DIMENSIONS

SO–24L
DW SUFFIX
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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