



## ST755C

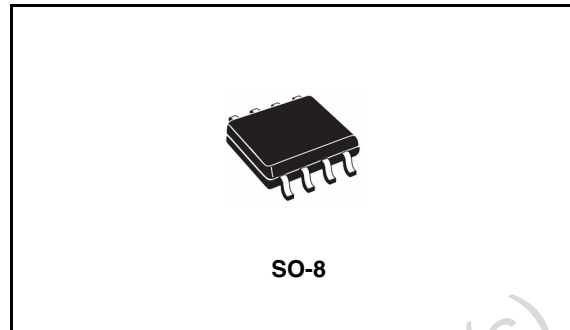
### Adjustable inverting negative output current mode PWM regulators

#### Features

- 2.7V to 11V input to adjustable negative output conversion
- 1W guaranteed output power ( $V_I > 4.5V$ ,  $T_A \leq 70^\circ C$ )
- 68% typ. efficiency at 6V
- Very low quiescent current: 1.2mA in on mode, 10 $\mu$ A in shut down mode
- Soft start
- Very low noise output
- 160KHz fixed frequency oscillator
- Mixed bipolar-CMOS technology

#### Description

The ST755 is an adjustable inverting switch-mode DC-DC regulator with internal Power MOSFET that generates an adjustable negative output from a voltage input of 2.7V to 11V, output current guaranteed at 200mA (for  $V_I > 4.5V$ ,  $V_O = -5V$



and  $T_A = 0^\circ C$  to  $70^\circ C$ ) and 275mA (typical value at  $T_A = 25^\circ C$ ,  $V_O = -5V$ ).

A logic controlled shut down pin that interfaces directly with microprocessor reduces supply current to only 10mA. Input to Output differential voltage is limited to  $V_I + |V_O| < 12.7V$ . No load supply current is 1.2mA

Table 1. Device summary

Part number	Package	Packaging
ST755C	ST755CD-TR	SO-8 (tape & reel)

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# Contents

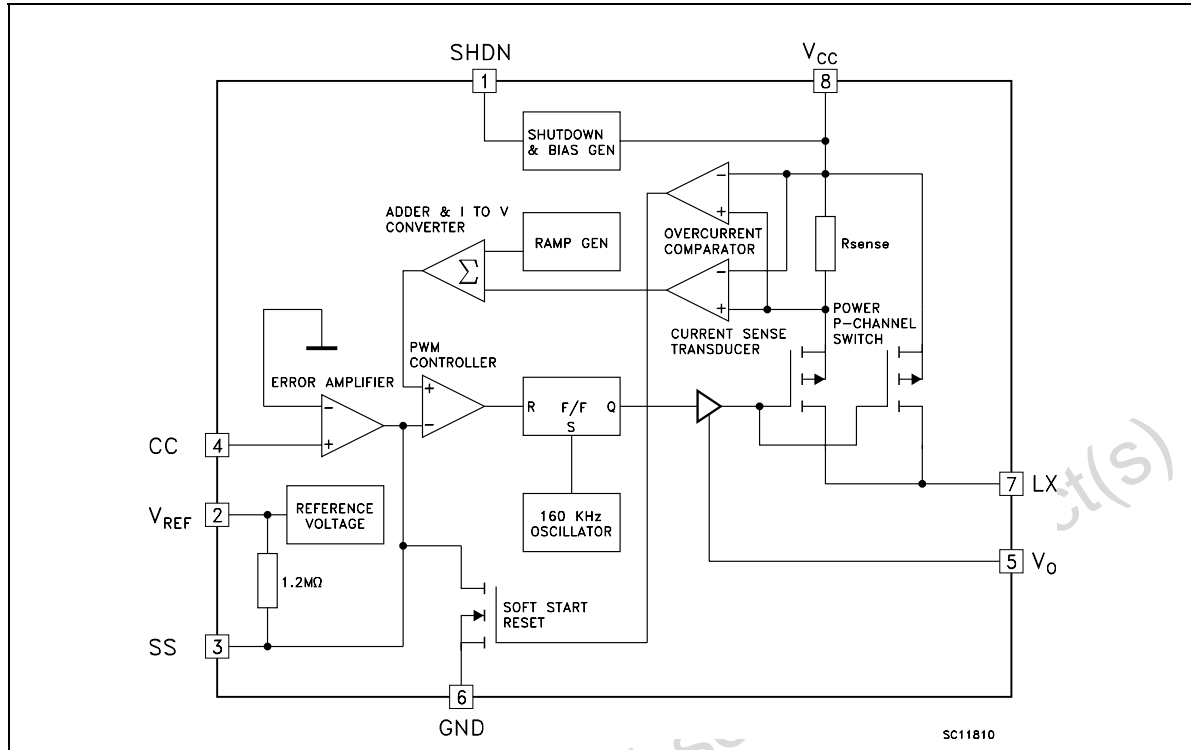
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# 1 Diagram

Figure 1. Schematic diagram



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## 2 Pin configuration

Figure 2. Pin connections (top view)

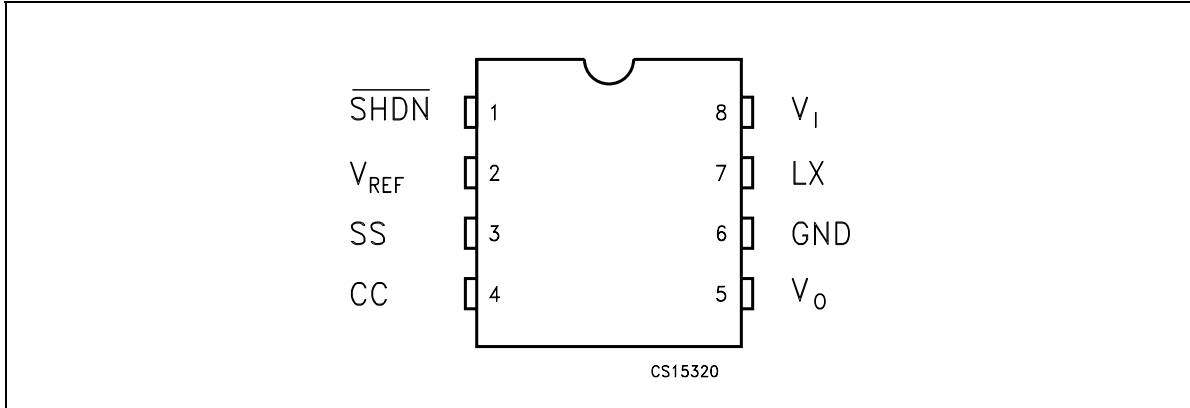


Table 2. Pin description

Pin N°	Symbol	Name and function
1	$\overline{\text{SHDN}}$	SHUT-DOWN control ( $V_{\text{CC}} = \text{ON}$ , GND = Shutdown)
2	$V_{\text{REF}}$	Reference output voltage: (1.25V)
3	SS	Soft start
4	CC	Compensation input
5	$V_{\text{O}}$	Negative output voltage
6	GND	Ground
7	LX	Switch output
8	$V_{\text{CC}}$	Supply voltage input

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC input voltage to GND <sup>(1)</sup>	-0.3 to 12	V
$V_{SHDN}$	Shutdown voltage, SS Voltage, CC Voltage	-0.3 to ( $V_{CC} + 0.3$ )	V
$V_{LX}$	Switch voltage (LX to $V_{CC}$ )	-12.5 to + 0.3	V
$V_{FB}$	Feedback voltage ( $V_O$ to GND)	-11 to + 0.9	V
$I_{LX}$	Peak switch current	2	A
$P_{TOT}$	Continuous power dissipation at $T_A = 70^\circ\text{C}$ (SO-8)	470	mW
$T_{op}$	Operating junction temperature range (C series)	-40 to 185	$^\circ\text{C}$
$T_{stg}$	Storage temperature range	-55 to +150	$^\circ\text{C}$

1. The input to output differential voltage is limited to  $V_{CC} + |V_O| < 12.7\text{V}$

*Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied*

**Table 4. Thermal data**

Symbol	Parameter	SO-8	Unit
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup>	160	$^\circ\text{C/W}$

1. This value depends from thermal design of PCB on which the device is mounted.

## 4 Electrical characteristics

**Table 5. Electrical characteristics** (Refer to the test circuits,  $V_{CC} = 5V$ ,  $V_O = -5.25$  to  $-4.75V$ ,  $I_{LOAD} = 0mA$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified. Typical value are referred at  $T_A = 25^\circ C$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_I$	Input voltage		4		11	V
$V_O$	Output voltage	$V_{CC} = 4.5$ to $6.2V$ , $I_O = 0$ to $200mA$	4.75	5	5.25	V
$I_O$	Output current	$V_{CC} = 4.5$ to $6.2V$ , $T_A = 0$ to $70^\circ C$	200	275		mA
		$V_{CC} = 4.5$ to $6.2V$ , $T_A = -40$ to $85^\circ C$	175			
		$V_{CC} = 4V$ , $V_O = -5V$		175		
		$V_{CC} = 2.7V$ , $V_O = -5V$		125		
$I_{SUPPLY}$	Supply current (including switching current)	No Load, $V_{SHDN} = V_{CC}$		1.2	3.5	mA
$I_{OFF}$	Standby current)	No Load, $V_{SHDN} = 0V$		10	100	$\mu A$
$I_{SC}$	Short circuit current)			1.2		A
$\Delta V_O$	Line regulation	$V_{CC} = 4$ to $6.2V$		0.1		%/V
$\Delta V_O$	Load regulation	$I_O = 0$ to $200mA$		0.003		%/mA
$V_{REF}$	Reference voltage	$T_A = 25^\circ C$	1.18	1.25	1.32	V
$\Delta V_{REF}$	Reference drift	$T_A = T_{MIN}$ to $T_{MAX}$		50		ppm/ $^\circ C$
$R_{DSON}$	LX on resistance			0.7		$\Omega$
$I_{LEAK}$	LX leakage current)	$V_{DS} = 10V$		1		$\mu A$
$I_{SH}$	Shutdown pin current)				1	$\mu A$
$V_{IH}$	SHDN input high threshold		2			V
$V_{IL}$	SHDN input low threshold				0.25	V
$f_{OSC}$	Oscillator frequency			160		KHz
h	Power efficiency	$I_O = 100mA$		68		%
CC	Compensation pin impedance			7.5		K $\Omega$

**Note:** Do not overload or short the Output to Ground. If the above conditions are observed, the device may be damaged.

## 5 Application information

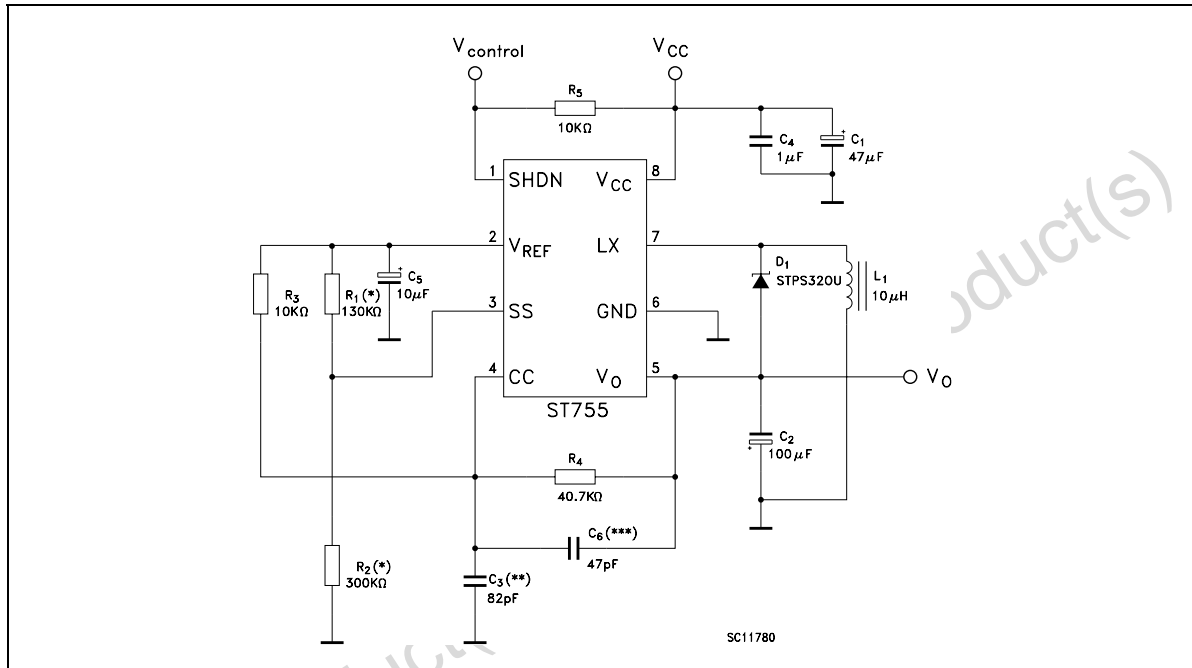
The ST755 is an IC developed for voltage conversion from an input voltage ranging from +2.4V to 11V to a regulated adjustable negative output limited by  $|V_{O}| \leq 12.7V - V_I$ . The circuit adopts a current-mode PWM control scheme to achieve good efficiency, high stability and low noise performance. The figure in the first page shown the detailed block diagram of the device.

ST755 is realized in a BCD technology in order to achieve high temperature stability, the best REFERENCE precision, a very low quiescent current and jitter free operations. The final stage is built around a 0.7 $\Omega$  - 2A P-Channel Power MOS. A fraction of the output current is splitted out for current detection. Internal clock frequency is fixed to 160KHz. Error amplifier drives the PWM comparator in order to keep 0V on the CC input. So  $R_3$  and  $R_4$  resistors are calculated by the following formulae  $R_4 = (|V_{O}|/V_{REF}) * R_3$  (see [Figure 3.](#)). For  $R_3$  can be choose any value between 2K $\Omega$  and 20K $\Omega$  Soft-Start (SS) input is a voltage dependent-output current limit (see [Figure 11.](#), Switch Current Limit vs. SS Input Voltage). SS pin is internally pulled to  $V_{REF}$  through a 1.2 M $\Omega$  resistor. Applying an appropriate capacitor at SS input is possible to obtain a soft-start current imitation during power up. Forcing Soft-Start (SS) input to a lower voltage through a resistive voltage driver ( $R_1$  and  $R_2$ ), the maximum LX current limit can be lowered according the diagram showed in [Figure 11.](#) When SHDN input is low, the total current consumption is reduced to 10 $\mu$ A.

## 6 Application circuit

To achieve the best performances from switching power supply topology, particular care to layout drawing is needed, in order to minimize EMI and obtain low noise, jitter free operation moreover, it ensures the full device functionality. Layout design proposed on demoboard (see [Figure 4.](#)) helps to lower the developing time. Wire lengths must be minimized, filter and by-pass capacitors  $C_1$ ,  $C_2$  and  $C_3$  must be low ESR type, placed as close possible to the integrated circuit. The  $10\mu\text{H}$  inductor must be chosen built on a core, taking care that saturation current should be higher than the peak LX switch current. See the Peak inductor current vs. load current graph ([Figure 6.](#)).

**Figure 3. Typical application circuit**



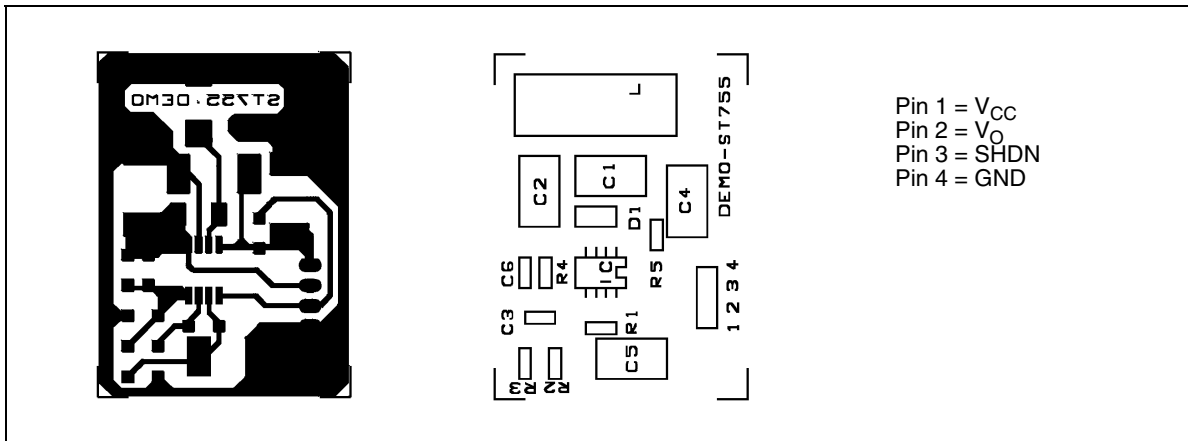
(\*) R1 and R2 can be omitted for  $I_O < 200\text{mA}$ .

(\*\*) C6: Very low noise but poor transient and load response speed.

(\*\*\*) C3 (alternative to C6): faster transient and load response.



Figure 4. Printed demoboard



Note: Drawings not in scale

Table 6. Component values

Capacitor	Value	Unit	Resistor	Value	Unit
C1	47	$\mu\text{F}$	R1	130	$\text{K}\Omega$
C2	100	$\mu\text{F}$	R2	300	$\text{K}\Omega$
C3	82	$\text{pF}$	R3	10	$\text{K}\Omega$
C4	1	$\mu\text{F}$	R4	40.7	$\text{K}\Omega$
C5	10	$\mu\text{F}$	R5	10	$\text{K}\Omega$
C6	47	$\text{pF}$			

## 7 Typical performance characteristics

(Unless otherwise specified  $T_J = 25^\circ\text{C}$ )

Figure 5. Load current vs supply voltage

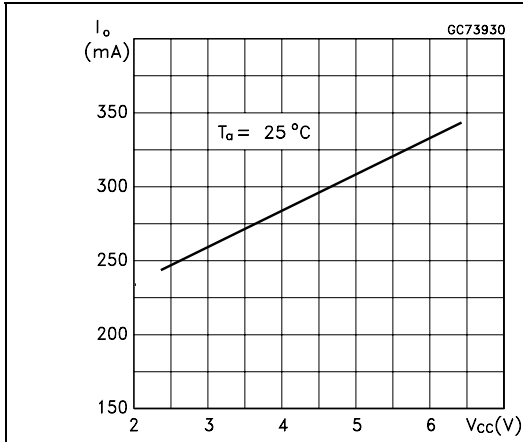


Figure 6. Peak inductor current vs load curr.

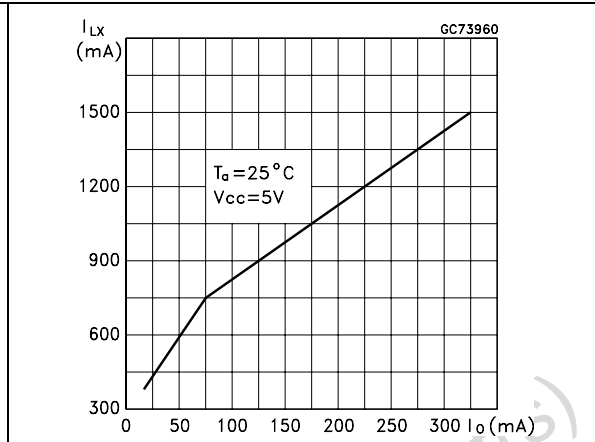


Figure 7. Load current vs supply voltage

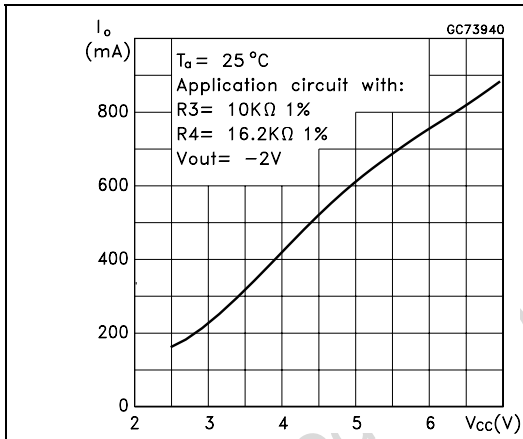


Figure 8. Switch ON resist. vs supply voltage

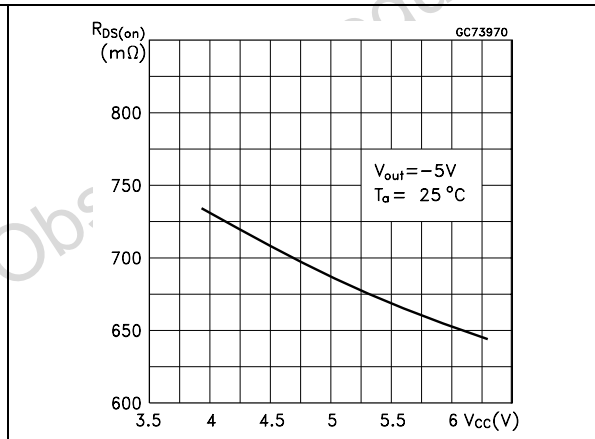


Figure 9. Efficiency vs load current

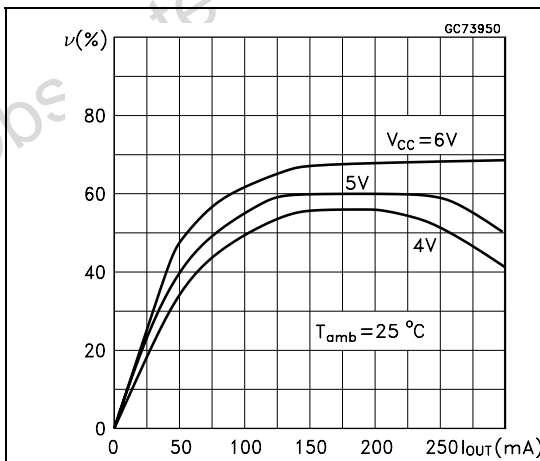


Figure 10. Oscillator frequency vs temperature & supply voltage

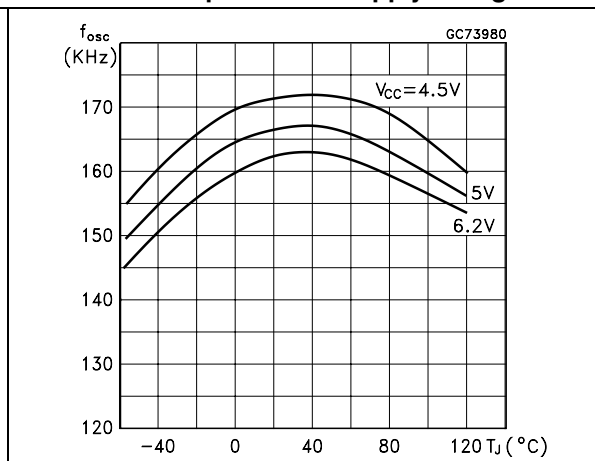


Figure 11. Switch current limit vs soft start voltage

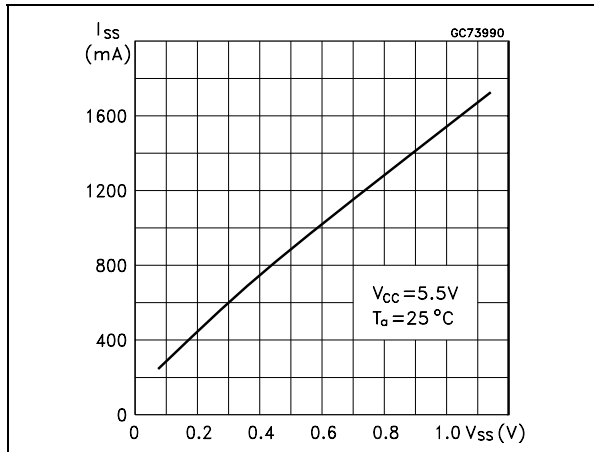


Figure 12. Reference voltage vs temperature

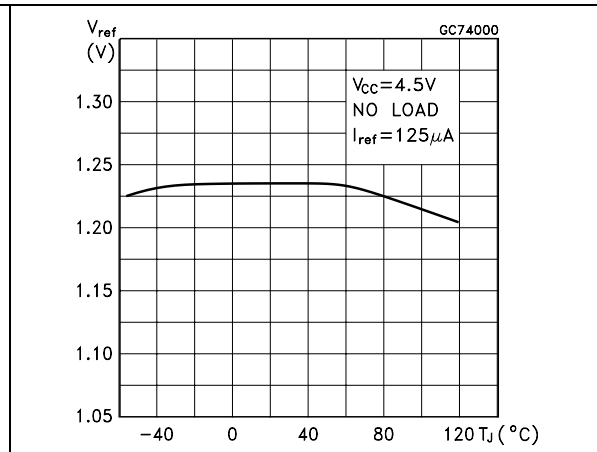
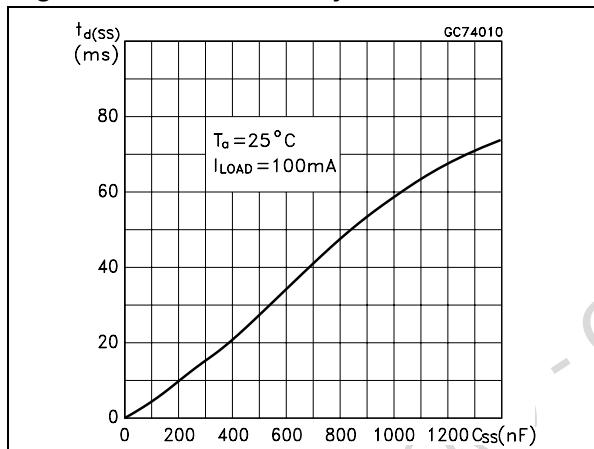


Figure 13. Soft start delay time



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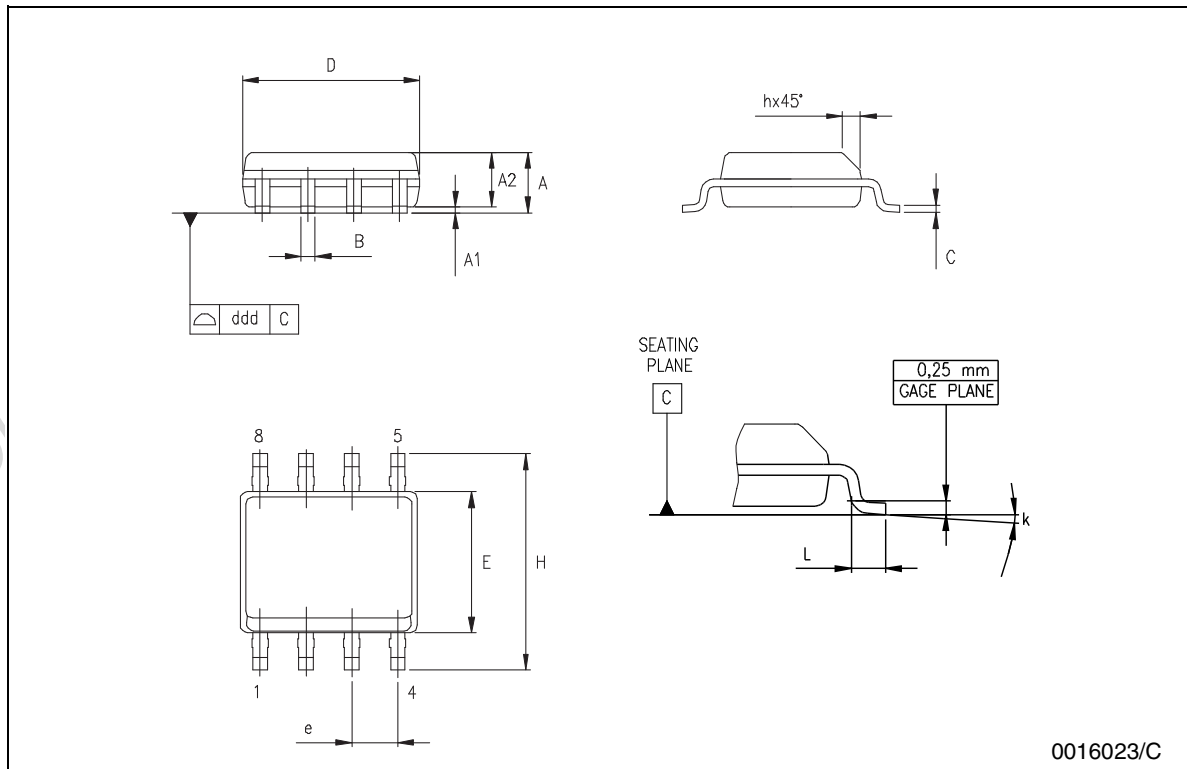
## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

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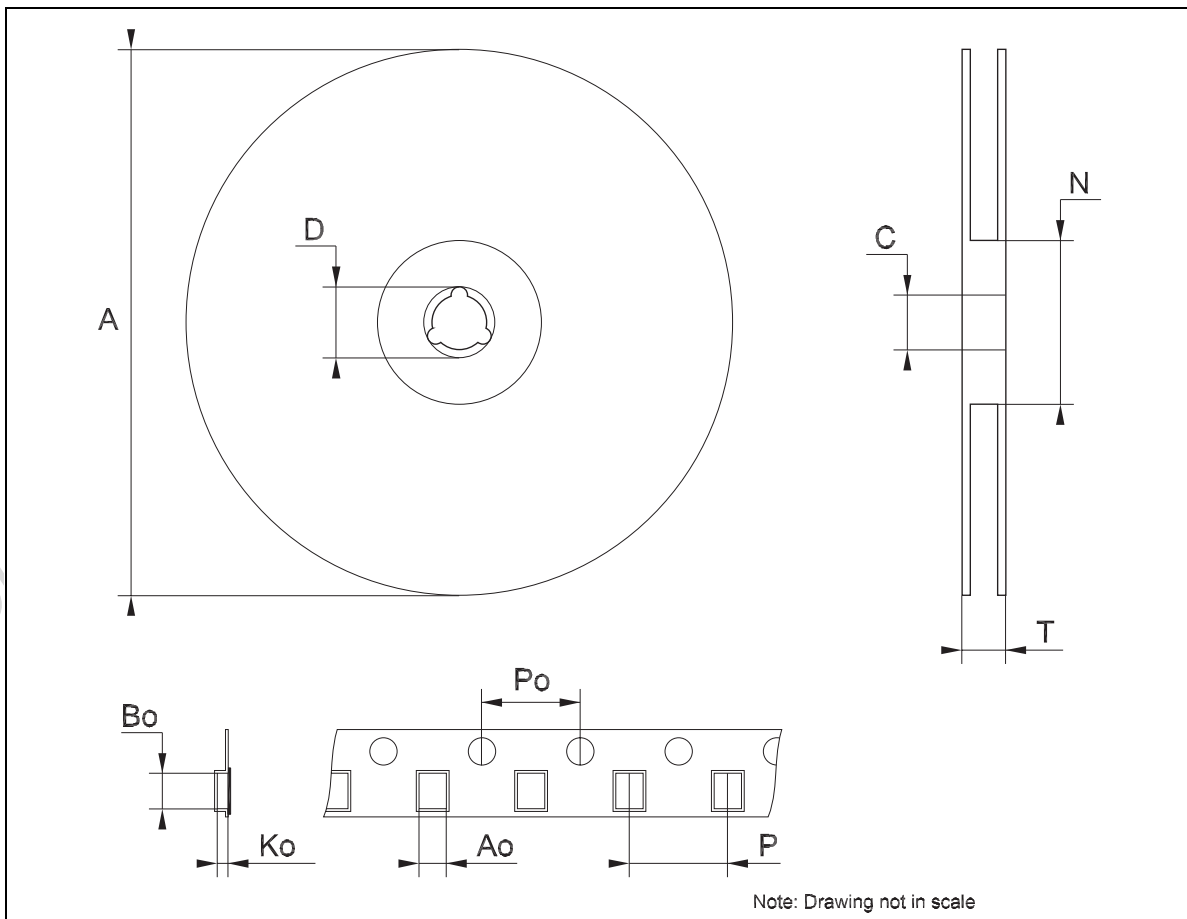
## SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



**Tape & Reel SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



## 9 Revision history

Table 7. Revision history

Date	Revision	Changes
06-Jul-2007	5	Device summary updated and the document has been reformatted.

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