FAIRCHILD SEMICONDUCTOR®

April 2007

FDMF8705
Driver plus FET Multi-chip Module

Benefits

- Fully optimized system efficiency. Higher efficiency levels are achievable compared with conventional discrete components.
- Space savings of up to 50% PCB versus discrete solutions.
- Higher frequency of operation.
- Simpler system design and board layout. Reduced time in component selection and optimization.

Features

- 12V typical Input Voltage
- Output current up to 18A
- 500KHz switching frequency capable
- Internal adaptive gate drive
- Integrated bootstrap diode
- Peak Efficiency >85%
- Under-voltage Lockout
- Output disable for lost phase shutdown
- Low profile SMD package
- RoHS Compliant

General Description

The FDMF8705 is a fully optimized integrated 12V Driver plus MOSFET power stage solution for high current synchronous buck DC-DC applications. The device integrates a driver IC and two Power MOSFETs into a space saving, 8mm x 8mm, 56-pin Power88™ package. Fairchild Semiconductor's integrated approach optimizes the complete switching power stage with regards to driver to FET dynamic performance, system inductance and overall solution ON resistance. Package parasitics and problematical layouts associated with conventional discrete solutions are greatly reduced. This integrated approach results in significant board space saving, therefore maximizing footprint power density. This solution is based on the Intel™ DrMOS specification.

Applications

- Desktop and server non V-core buck converters.
- CPU/GPU power train in game consoles and high end desktop systems.
- High-current DC-DC Point of Load (POL) converters
- Networking and telecom microprocessor voltage regulators
- Small form factor voltage regulator modules

Powertrain Application Circuit

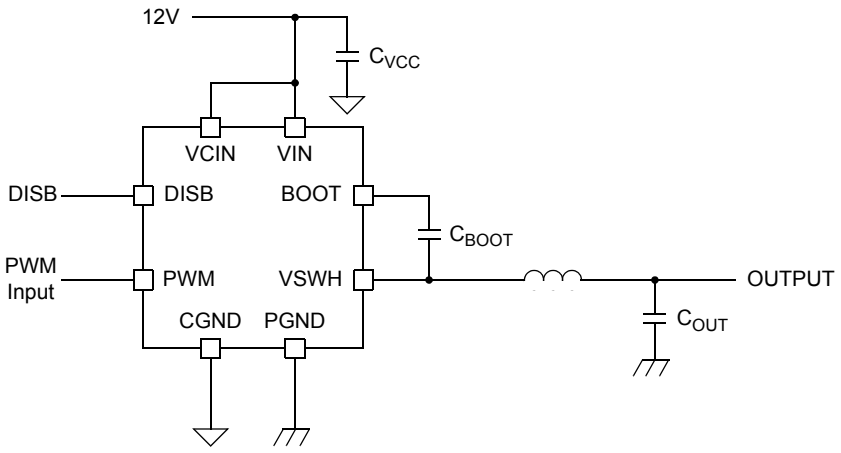

Figure 1. Powertrain Application Circuit

Ordering Information

Part	Current Rating Max [A]	Input Voltage Typical [V]	Frequency Max [KHz]	Device Marking
FDMF8705	18	12	500	FDMF8705

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Functional Block Diagram

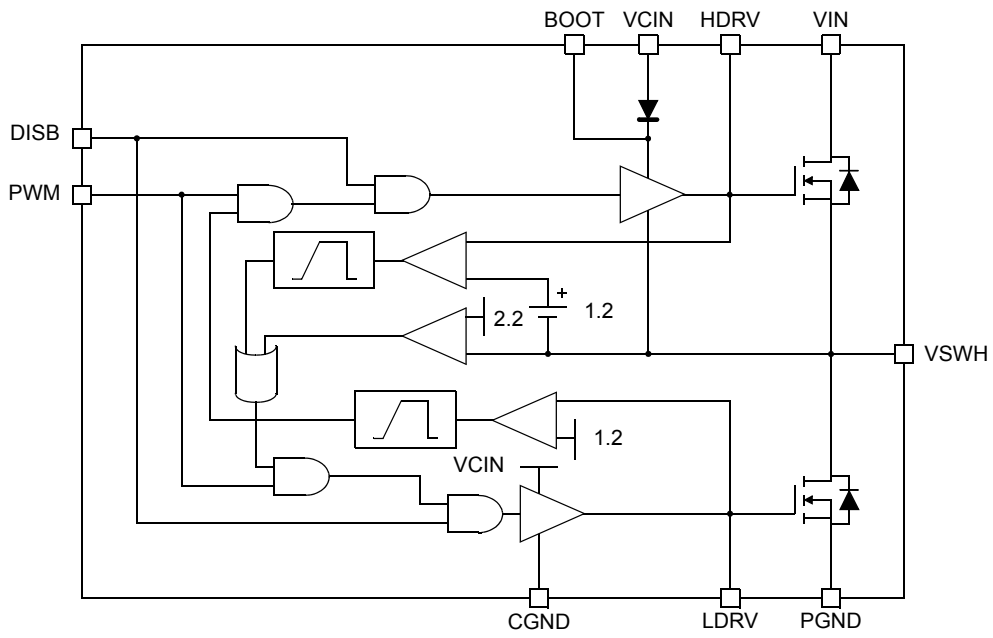

Figure 2. Functional Block Diagram

Pin Configuration

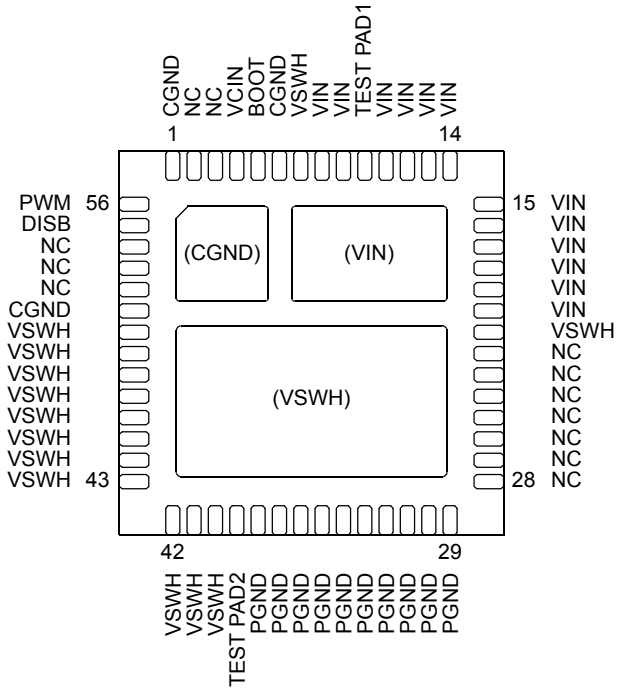

Figure 3. Power88 56L Bottom View

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Pin Description

Pin	Name	Function
1,6,51	CGND	IC Ground. Ground return for driver IC.
2,3,22-28,52-54	NC	No connect
4	VCIN	IC Supply. +12V chip bias power. Bypass with a 1µF ceramic capacitor.
5	BOOT	Bootstrap Supply Input. Provides voltage supply to high-side MOSFET driver. Connect bootstrap capacitor.
7,21,40-50	VSWH	Switch Node Input. SW Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection.
8,9,11-20	VIN	Power Input. Output stage supply voltage.
10	TEST PAD 1	For manufacturing test only. HDRV pin. This pin must be floated. Must not be connected to any pin.
29-38	PGND	Power ground. Output stage ground. Source pin of low side MOSFET(s).
39	TEST PAD 2	For manufacturing test only. LDRV pin. This pin must be floated. Must not be connected to any pin.
55	DISB	Output Disable. When low, this pin disable FET switching (HDRV and LDRV are held low).
56	PWM	PWM Signal Input. This pin accepts a logic-level PWM signal from the controller.

Absolute Maximum Rating

Parameter		Min.	Max.	Units
V_{CIN} to PGND		-0.5	15	V
V_{IN} to PGND		-0.5	15	V
PWM, DSIB to GND		-0.3	5.5	V
VSWH to PGND	Continuous	-1	15	V
	Transient (t = 100ns, f_{sw} = 500KHz)	-5	25	V
BOOT to VSWH		-0.3	15	V
BOOT to PGND	Continuous	-0.3	30	V
	Transient (t = 100ns, f_{sw} = 500KHz)	-0.3	33	V
$I_{O(AV)}$	V_{IN} = 12V, V_O = 1.3V, f_{sw} = 500KHz, T_{PCB} = 100°C		18	A
$I_{O(PK)}$	V_{IN} = 12V, t_{PULSE} = 10µs		65	A
R_{JPCB}	Junction to PCB Thermal Resistance (note 1)		8	°C/W
P_D	T_{PCB} = 100°C (note 1)		6.25	W
Operating and Storage Junction Temperature Range		-55	150	°C

Recommended Operating Range

Parameter		Min.	Typ.	Max.	Units
V_{CIN}	Control Circuit Supply Voltage	6.4	12	13.5	V
V_{IN}	Output Stage Supply Voltage	6.4	12	14	V

Electrical Characteristics

V_{IN} = 12V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Control Circuit Supply Current	I_{CIN}	f_{SW} = 0Hz, V_{DISB} = 0V		3.5	8	mA
		f_{SW} = 500KHz, V_{DISB} = 5V		18		
Undervoltage lockout threshold	$V_{TH(UVLO)}$(2)	Turn-on		6		V
		Turn-off		5.25		V
PWM Input High Voltage	$V_{IH(PWM)}$		3.5			V

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Electrical Characteristics

V_{IN} = 12V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
PWM Input Low Voltage	$V_{IL(PWM)}$				0.8	V
PWM Input Current	$I_{IL(PWM)}$		-1		1	µA
Output Disable Input High Voltage	$V_{IH(DISB)}$		2.5			V
Output Disable Input Low Voltage	$V_{IL(DISB)}$				0.8	V
Output Disable Input Current	I_{DISB}		-1		1	µA
Output Stage Leakage Current	$I_{IN_LEAKAGE}$	V_{DISB} = 0V		250		µA
Propagation Delay	$t_{PDL(LDRV)}$ (3)	V_{IN} = 12V, V_{OUT} = 1.3V, f_{sw} = 500KHz, I_O = 18A		51		ns
	$t_{PDL(HDRV)}$ (3)			39		ns
	$t_{PDH(LDRV)}$ (3)			47		ns
	$t_{PDH(HDRV)}$ (3)			46		ns

Note 1: Package power dissipation based on 4 layer, 2 square inch, 2 oz. copper pad. R_{JPCB} is the steady state junction to PCB thermal resistance with PCB temperature referenced at VSWH pin.

Note 2: When combined with controller, driver UVLO must be less than that of controller.

Note 3: $t_{PDL(LDRV/HRDV)}$ refers to HIGH-to-LOW transition, $t_{PDH(LDRV/HDRV)}$ refers to LOW-to-HIGH transition.

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Typical Characteristics

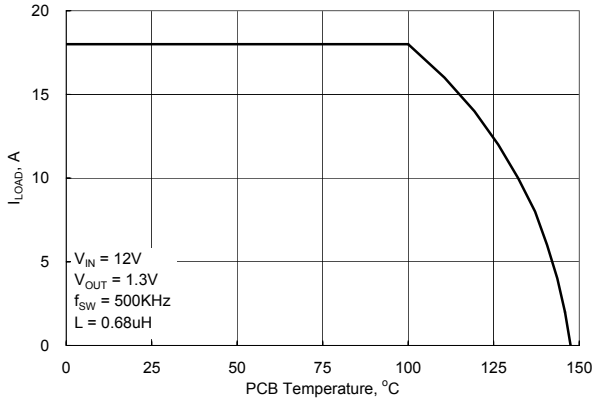

Figure 4. Safe Operating Area vs. PCB Temperature

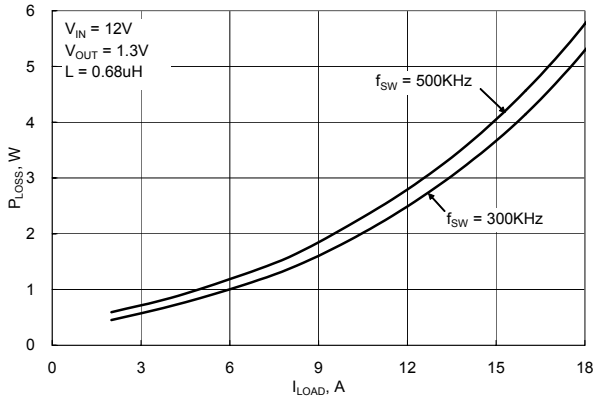

Figure 5. Module Power Loss vs. Output Current
(V_O measured at VSWH pin)

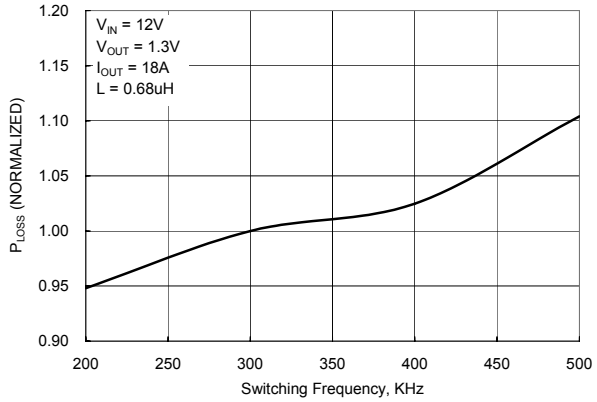

Figure 6. Power Loss vs. Switching Frequency

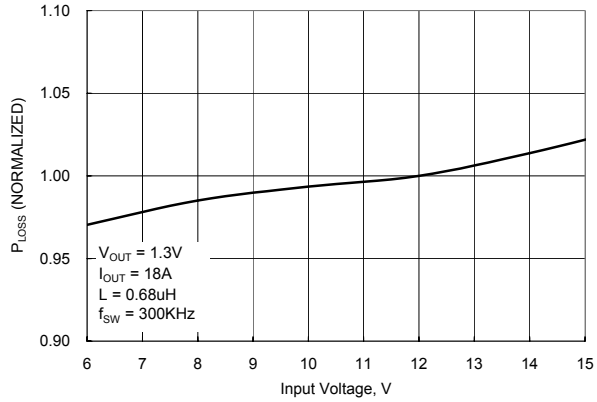

Figure 7. Power Loss vs. Input Voltage

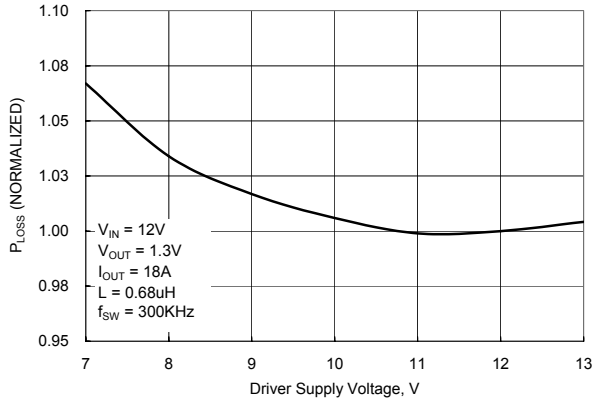

Figure 8. Power Loss vs. Driver Supply Voltage

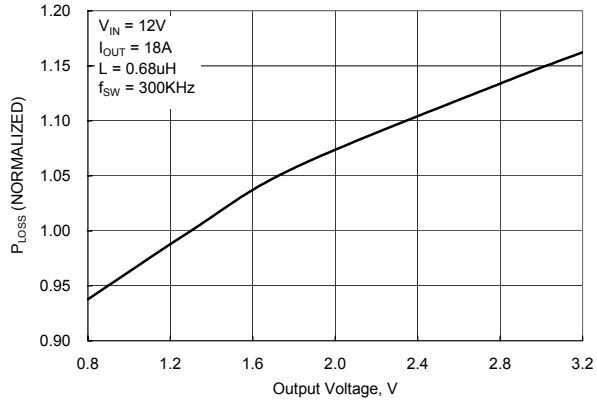

Figure 9. Power Loss vs. Output Voltage

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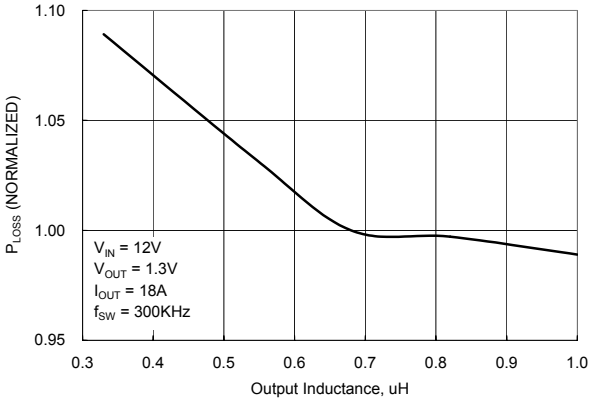

Figure 10. Power Loss vs. Output Inductance

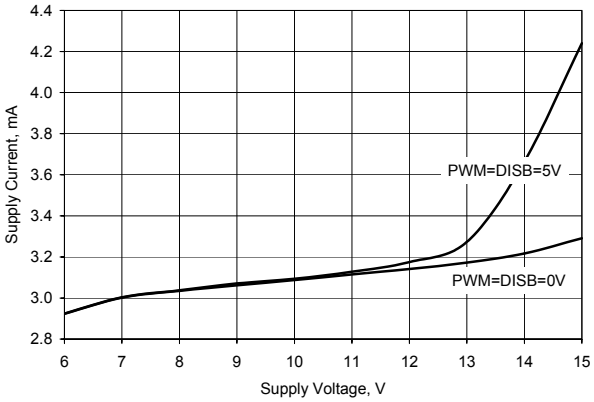

Figure 11. Supply Current vs. Supply Voltage

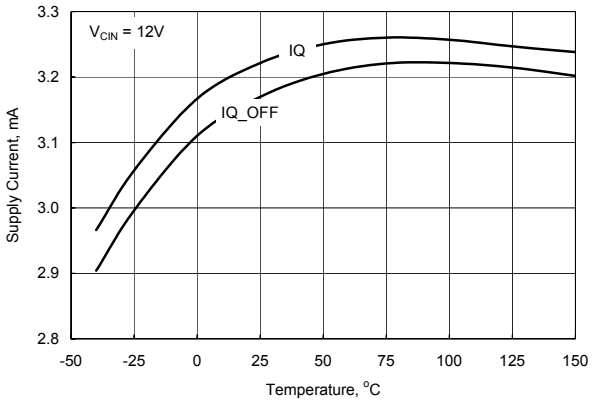

Figure 12. Supply Current vs. Temperature

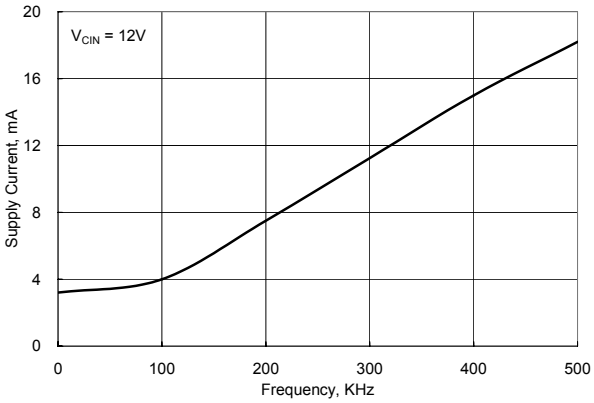

Figure 13. Supply Current vs. Frequency

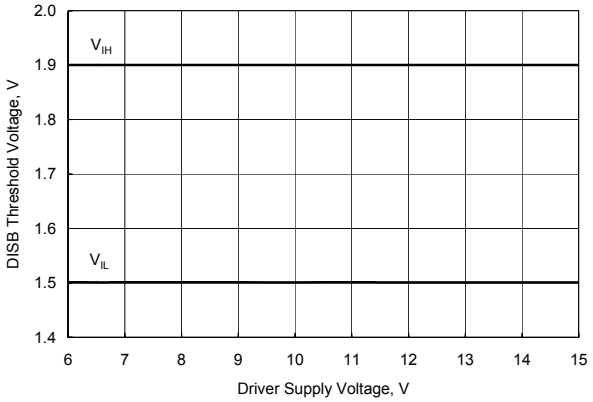

Figure 14. DISB Threshold Voltage vs. Driver Supply Voltage

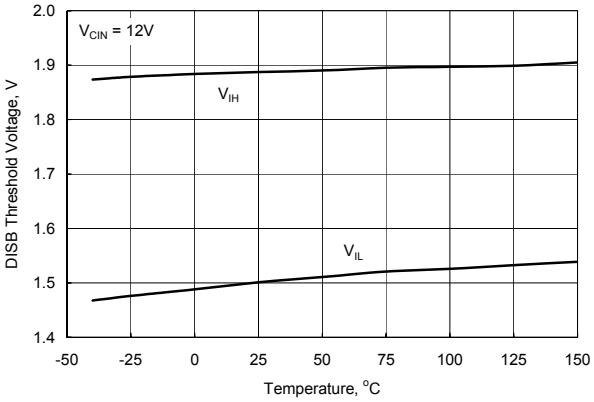

Figure 15. DISB Threshold Voltage vs. Temperature

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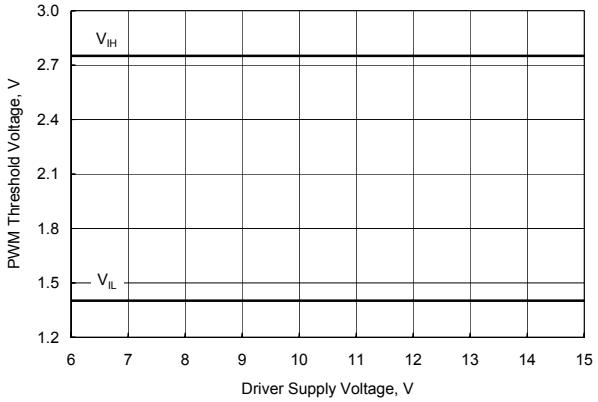

Figure 16. PWM Threshold Voltage vs. Driver Supply Voltage

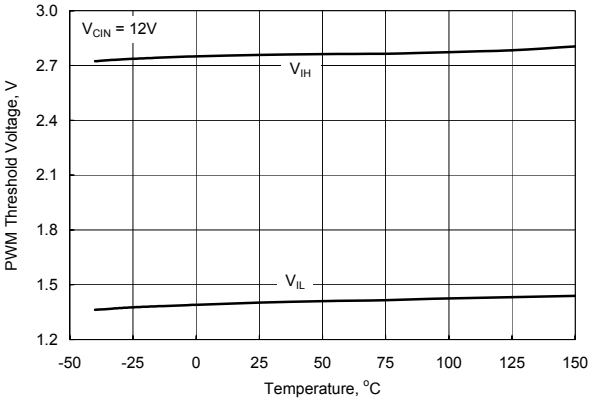

Figure 17. PWM Threshold Voltage vs. Temperature

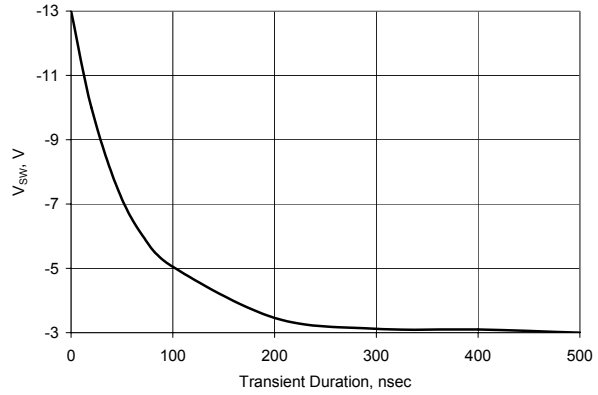

Figure 18. VSWH vs. Transient Duration

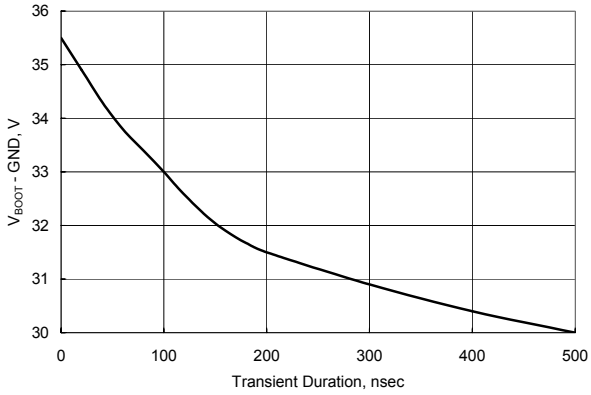

Figure 19. Boot to Ground Voltage vs. Transient Duration

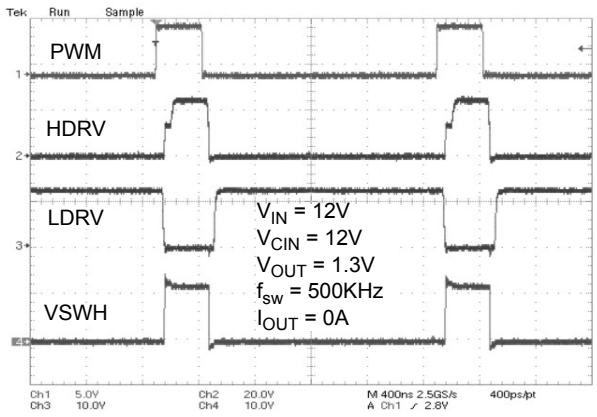

Figure 20. Switching Waveform at Iout = 0A

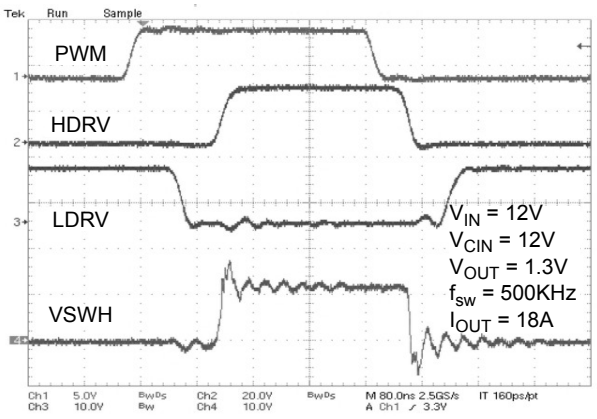

Figure 21. Switching Waveform at Iout = 18A

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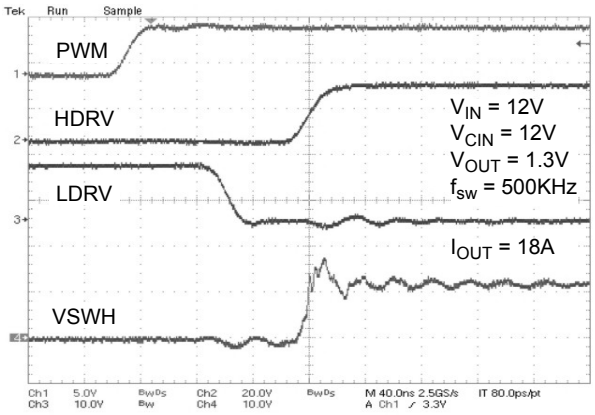

Figure 22. Switching Waveform (Rising edge)

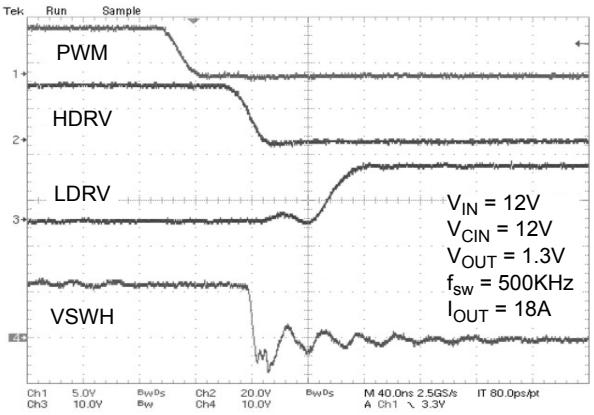

Figure 23. Switching Waveform (Falling Edge)

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Description of Operation

Circuit Description

The FDMF8705 is a driver plus FET module optimized for synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each part is capable of driving speeds up to 500KHz.

Low-Side Driver

The low-side driver (LDRV) is designed to drive a ground referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for LDRV is internally connected between VCIN and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB = 0V), LDRV is held low.

High-Side Driver

The high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of the internal diode and external bootstrap capacitor (C_{BOOT}). During start-up, VSWH is held at PGND, allowing C_{BOOT} to charge to VCIN through the internal diode. When the PWM input goes high, HDRV will begin to charge the high-side MOSFET's gate (Q1). During this transition, charge is removed from C_{BOOT} and delivered to Q1's gate. As Q1 turns on, VSWH rises to V_{IN}, forcing the BOOT pin to V_{IN} +$V_{C(BOOT)}$, which provides sufficient VGS enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to VSWH. C_{BOOT} is then recharged to VCIN when VSWH falls to PGND. HDRV output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Adaptive Gate Drive Circuit

The driver IC embodies an advanced design that ensures minimum MOSFET dead-time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to Figure 24 and 25 for the relevant timing waveforms.

To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, Q2 will begin to turn OFF after some propagation delay ($t_{PDL(LDRV)}$). Once the LDRV pin is discharged below ~1.2V, Q1 begins to turn ON after adaptive delay $t_{PDH(HDRV)}$.

To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, Q1 will begin to turn OFF after some propagation delay ($t_{PDL(HDRV)}$). Once the VSWH pin falls below ~2.2V, Q2 begins to turn ON after adaptive delay $t_{pdh(LDRV)}$.

Additionally, V_{GS} of Q1 is monitored. When $V_{GS(Q1)}$ is discharged below ~1.2V, a secondary adaptive delay is initiated, which results in Q2 being driven ON after $t_{PDH(LDRV)}$, regardless of SW state. This function is implemented to ensure C_{BOOT} is recharged each switching cycle, particularly for cases where the power convertor is sinking current and SW voltage does not fall below the 2.2V adaptive threshold. Secondary delay $t_{PDH(HDRV)}$ is longer than $t_{PDH(LDRV)}$.

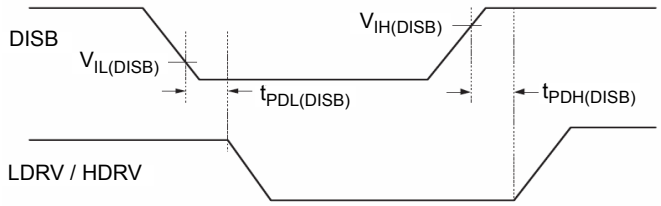

Figure 24. Output Disable Timing

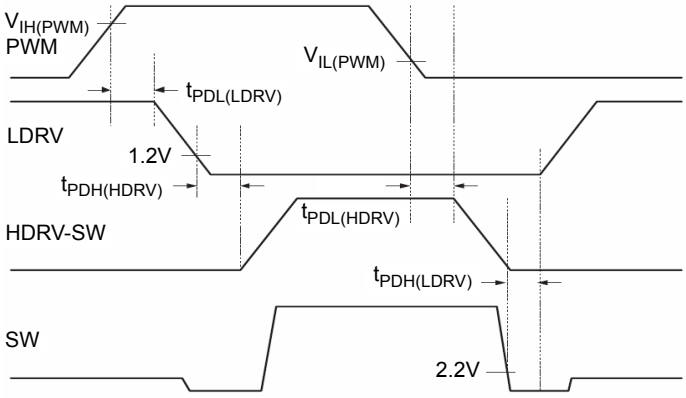

Figure 25. Adaptive Gate Drive Timing

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Typical Application

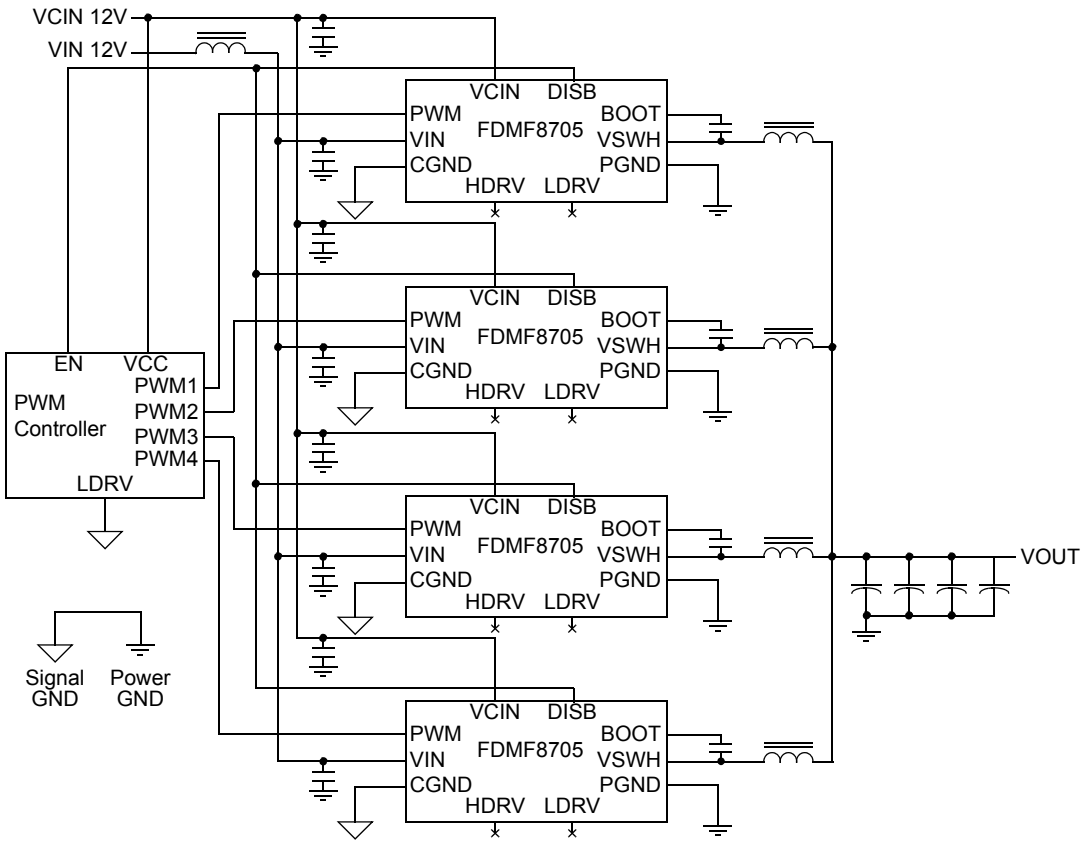

Figure 26. Typical Application

Application Information
Supply Capacitor Selection

For the supply input (VCIN) of the FDMF8705, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FDMF8705 VCIN and CGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and the internal diode, as shown in Figure 26. Selection of these components should be done after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} >= \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where Q_G is the total gate charge of the high-side MOSFET, and ΔV_{BOOT} is the voltage droop allowed on the high-side MOSFET drive. For example, the Q_G of the internal high-side MOSFET is about 21nC @ $12V_{GS}$. For an allowed droop of ~300mV, the required bootstrap capacitance is > 100nF. A good quality ceramic capacitor must be used.

The average diode forward current, $I_{F(AVG)}$, can be estimated by:

$$I_{F(AVG)} = Q_G \times f_{SW} \quad (2)$$

where f_{SW} is the switching frequency of the controller. The peak surge current rating of the internal diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces. For applications requiring higher I_F, an external diode may be used in parallel to the internal diode.

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Module Power Loss Measurement and Calculation

Refer to Figure 27 for module power loss testing method. Power loss calculation are as follows:

(a) P_{IN} = $(V_{IN} \times I_{IN}) + (V_{CIN} \times I_{CIN})$ (W)

(b) P_{OUT} = $V_O \times I_{OUT}$ (W)

(c) P_{LOSS} = $P_{IN} - P_{OUT}$ (W)

PCB Layout Guideline

Figure 28. shows a proper layout example of FDMF8705 and critical parts. All of high current flow path, such as V_{IN}, VSWH, V_{OUT} and GND copper, should be short and wide for better and stable current flow, heat radiation and system performance.

Following is a guideline which the PCB designer should consider:

1. Input bypass capacitors should be close to V_{IN} and GND pin of FDMF8705 to help reduce input current ripple component induced by switching operation.

2. It is critical that the VSWH copper has minimum area for lower switching noise emission. VSWH copper trace should also be wide enough for high current flow. Other signal routing path, such as PWM IN and BOOT signal, should be considered with care to avoid noise pickup from VSWH copper area.

3. Output inductor location should be as close as possible to the FDMF8705 for lower power loss due to copper trace.

4. Place ceramic bypass capacitor and boot capacitor as close to VCIN and BOOT pin of FDMF8705 in order to supply stable power. Routing width and length should also be considered.

5. Use multiple Vias on each copper area to interconnect each top, inner and bottom layer to help smooth current flow and heat conduction. Vias should be relatively large and of reasonable inductance.

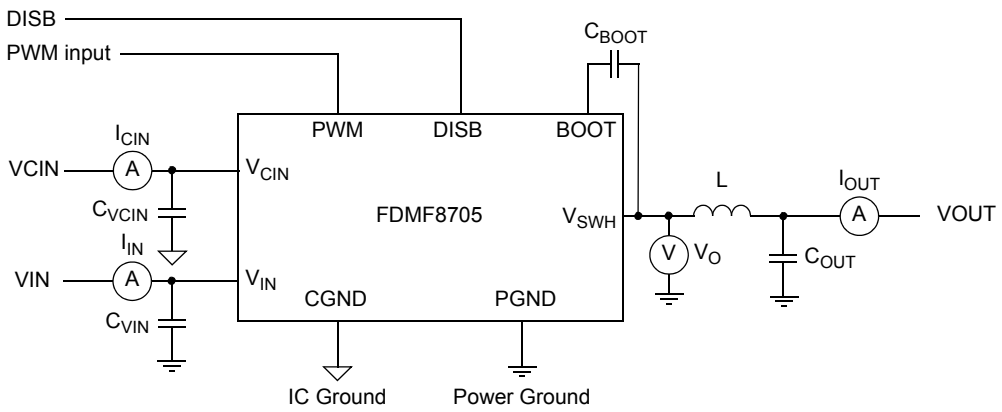

Figure 27. Power Loss Measurement Block Diagram

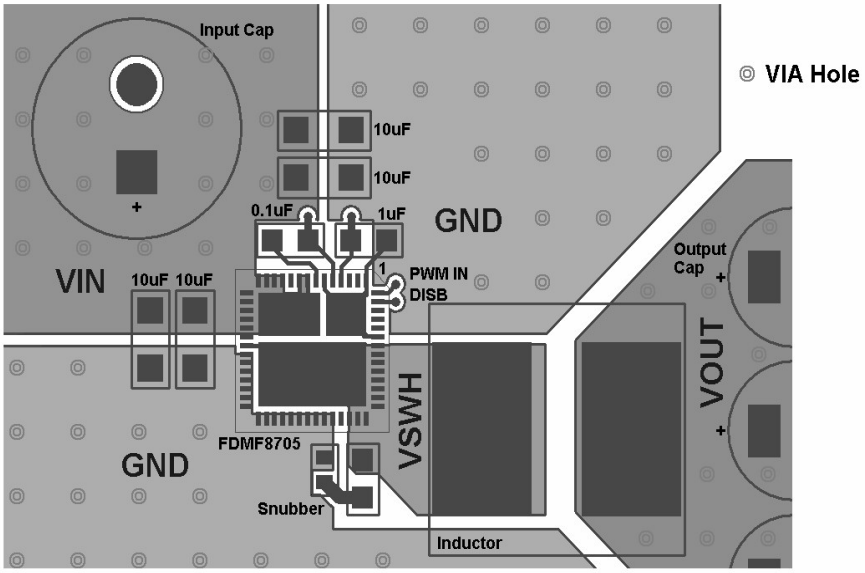

Figure 28. Typical PCB Layout Example (Top View)

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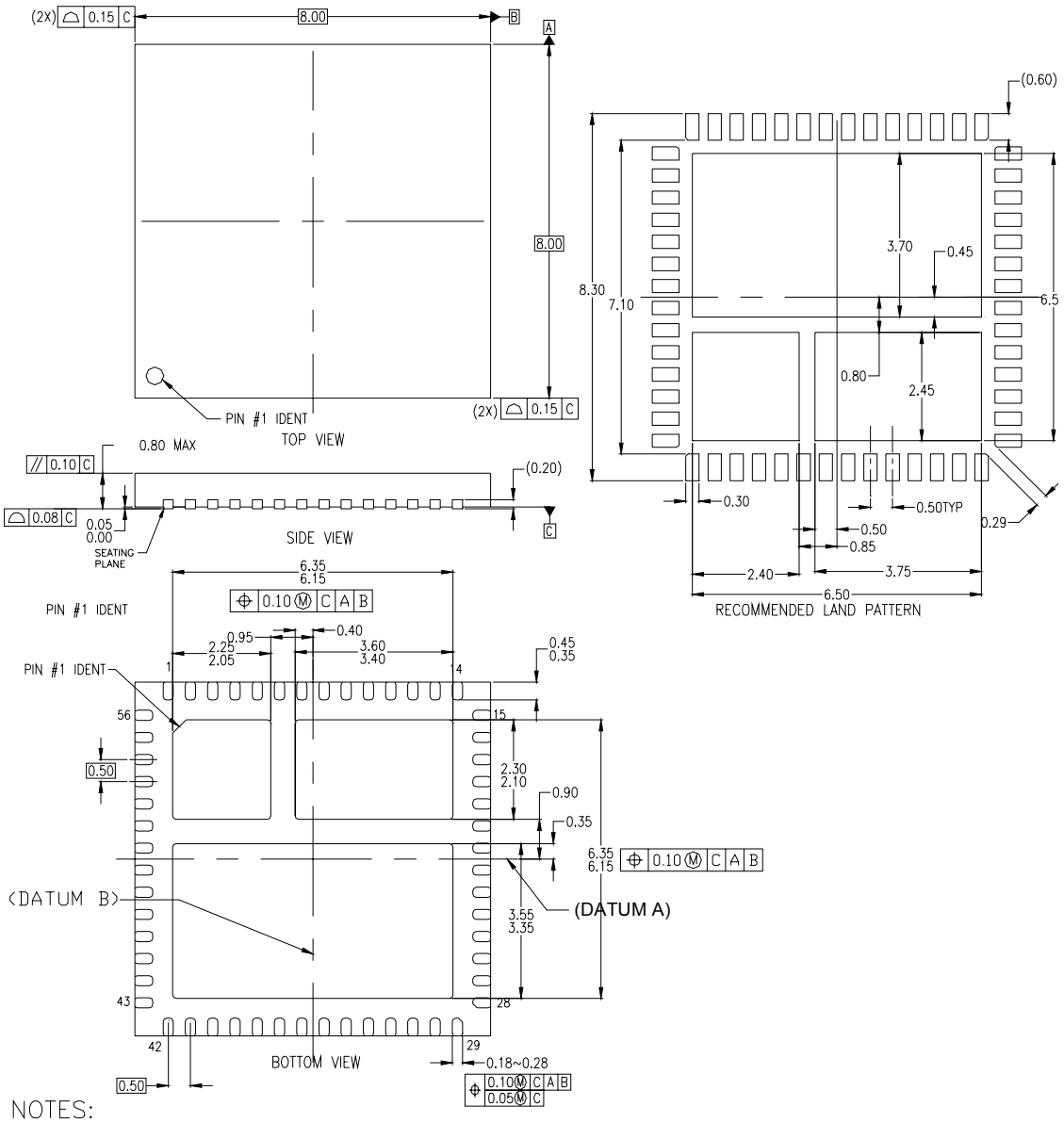
Dimensional Outline and Pad layout



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WLLD-5,6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, NOR TIE BAR PROTRUSIONS.

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Definition of Terms

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