19-2837; Rev 1; 11/04

EVALUATION KIT AVAILABLE

800mA, 2MHz, PWM DC-to-DC Step-Down Converter with RESET

MAX1572

General Description

The MAX1572 is a fixed-frequency, synchronous step-down DC-to-DC converter to power low-voltage microprocessor/DSP cores in portable equipment requiring high efficiency in a limited PC board area. The features are optimized for high efficiency over a wide load range, small external component size, low output ripple, and excellent transient response. The input supply voltage range is from 2.6V to 5.5V, while the output is internally fixed from 0.75V to 2.5V in 50mV increments with a guaranteed output current of 800mA. The high 2MHz switching allows tiny low-cost capacitors and a low-profile inductor, while the power-saving pulse-group mode reduces quiescent current to 48µA (typ) with light loads. To reduce noise and RF interference, the converter can be configured to provide forced-PWM operation.

The MAX1572 includes a low on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency and minimize external component count. No external diode is needed. Other features include soft-start to eliminate inrush current at startup and a 170ms (min) $\overline{\text{RESET}}$ output to provide power-on/undervoltage reset. The MAX1572 is available in a 12-pin, 4mm x 4mm thin QFN package with exposed paddle.

Applications

Cell Phones and Smart Phones
PDAs, Palmtops, and Notebook Computers
MP3 and DVD Players
Digital Cameras and Camcorders
PCMCIA Cards
Hand-Held Instruments

Selector Guide appears at end of data sheet.

Features

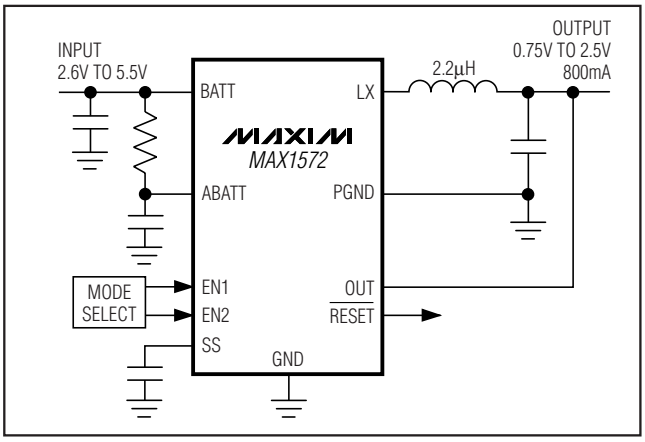
- ♦ **Up to 97% Efficiency**
- ♦ **2MHz PWM Switching**
- ♦ **800mA Guaranteed Output Current**
- ♦ **Low 48µA Quiescent Current**
- ♦ **Power-Saving Modes: Pulse-Group, Pulse-Skip, Forced-PWM Mode**
- ♦ **0.75V to 2.5V Preset Output Range (in 50mV Increments)**
- ♦ **Voltage-Positioning Load Transients**
- ♦ **5mV$_{P-P}$ Output Ripple**
- ♦ **Tiny 2.2µH Inductor**
- ♦ **10µF Ceramic Output Capacitor**
- ♦ **Low 0.1µA Shutdown Current**
- ♦ **No External Schottky Diode Required**
- ♦ **Soft-Start with Zero Inrush Current**
- ♦ **170ms (min) $\overline{\text{RESET}}$ Output**
- ♦ **Small 12-Pin, 4mm x 4mm Thin QFN Package**

Ordering Information

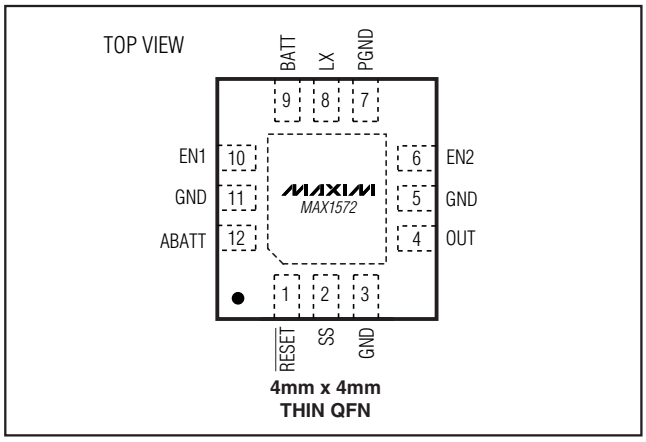
PART	TEMP RANGE	PIN-PACKAGE
MAX1572ETC075	-40°C to +85°C	12 Thin QFN-EP**
MAX1572ETC130	-40°C to +85°C	12 Thin QFN-EP**
MAX1572ETC150	-40°C to +85°C	12 Thin QFN-EP**
MAX1572ETC180	-40°C to +85°C	12 Thin QFN-EP**
MAX1572ETC250	-40°C to +85°C	12 Thin QFN-EP**
MAX1572ETCxyz*	-40°C to +85°C	12 Thin QFN-EP**

**xyz is for the output voltage (e.g., MAX1572ETC165 has a 1.65V output). Minimum order quantity is 2500.*
***EP = Exposed paddle.*

Typical Operating Circuit



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

800mA, 2MHz, PWM DC-to-DC Step-Down Converter with RESET

ABSOLUTE MAXIMUM RATINGS

ABATT, BATT, EN1, EN2, RESET, OUT, SS to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
LX Current (Note 1) .....±2.1A
Output Short-Circuit Duration .....Infinite
Continuous Power Dissipation (T_A = +70°C)
12-Pin Thin QFN (derate 16.9mW/°C above +70°C)...1349mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND and BATT. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 3.6V, **T_A = +0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Input Voltage			2.6		5.5	V
Undervoltage Lockout Threshold	V_{BATT} rising and falling, 1% hysteresis		2.20	2.35	2.55	V
Quiescent Supply Current	EN1 = GND, EN2 = BATT, no switching			48	80	µA
	EN1 = BATT, EN2 = GND, no switching			700		
Shutdown Supply Current	EN1 = EN2 = GND, T_A = +25°C			0.1	1	µA
Maximum Output Current			800			mA
OUT Bias Current				6	9	µA
Output-Voltage Accuracy (Voltage Positioning)	No load, EN1 = EN2 = BATT			1.2	2.7	%
	100mA load		-0.4	+0.8	+2.0	
	300mA load			0		
	550mA load			-1		
	800mA load			-2		
Line Regulation				0.3		%/V
P-Channel On-Resistance	I_{LX} = 180mA	V_{BATT} = 3.6V		0.28	0.45	Ω
		V_{BATT} = 2.6V		0.33		
N-Channel On-Resistance	I_{LX} = 180mA	V_{BATT} = 3.6V		0.18	0.30	Ω
		V_{BATT} = 2.6V		0.20		
P-Channel Current-Limit Threshold			1.00	1.25	1.65	A
N-Channel Current-Limit Threshold	EN1 = EN2 = BATT		-0.68	-0.52	-0.37	A
N-Channel Zero-Crossing Threshold	EN1 = BATT, EN2 = GND		15	40	65	mA
LX Output Current	(Note 2)				1.4	A_{RMS}
LX Leakage Current	EN1 = EN2 = GND			0.1	10	µA
Maximum Duty Cycle			100			%
Minimum Duty Cycle	EN1 = BATT, EN2 = GND or EN1 = GND, EN2 = BATT			0		%
	EN1 = EN2 = BATT			16.7	17.3	
Switching Frequency			1.8	2	2.2	MHz
SS Output Impedance			65	100	150	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 3.6V, **T_A = +0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SS Discharge Resistance	EN1 = EN2 = GND		100	200	Ω
EN_ Logic Input High	V_{ABATT} > 4.2V	1.6			V
	V_{ABATT} ≤ 4.2V	1.4			
EN_ Logic Input Low				0.4	V
EN_ Logic Input Current			0.1	1	µA
$\overline{RESET}$ Threshold	Percent of nominal, measured at OUT	87	90	93	%
$\overline{RESET}$ Timer Delay Time	From V_{OUT} > 90% to $\overline{RESET}$ = HI	170	200	230	ms
$\overline{RESET}$ Output Low Level	I_{SINK} = 1mA		0.015	0.075	V
$\overline{RESET}$ Internal Pullup Resistance to OUT		9	14	20	kΩ
Thermal-Shutdown Threshold	T_J rising		160		°C
Thermal-Shutdown Hysteresis			20		°C

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Input Voltage		2.6		5.5	V
Undervoltage Lockout Threshold	V_{BATT} rising and falling, 1% hysteresis	2.20		2.55	V
Quiescent Supply Current	EN1 = GND, EN2 = BATT, no switching			80	µA
Shutdown Supply Current	EN1 = EN2 = GND			3	µA
Maximum Output Current		800			mA
OUT Bias Current				9	µA
Output-Voltage Accuracy (Voltage Positioning)	No load, EN1 = EN2 = BATT			3.2	%
	100mA load	-1.2		+2.8	
P-Channel On-Resistance	I_{LX} = 180mA			0.45	Ω
N-Channel On-Resistance	I_{LX} = 180mA			0.3	Ω
N-Channel Current-Limit Threshold	EN1 = EN2 = BATT	-0.68		-0.22	A
N-Channel Zero-Crossing Threshold	EN1 = BATT, EN2 = GND	10		65	mA
LX Output Current	(Note 2)			1.4	A_{RMS}
LX Leakage Current	EN1 = EN2 = GND			10	µA
Maximum Duty Cycle		100			%
Minimum Duty Cycle	EN1 = EN2 = BATT			17.3	%
Switching Frequency		1.8		2.2	MHz
SS Output Impedance		65		150	kΩ
SS Discharge Resistance	EN1 = EN2 = GND			200	Ω
EN_ Logic Input High	V_{ABATT} > 4.2V	1.6			V
	V_{ABATT} ≤ 4.2V	1.4			

800mA, 2MHz, PWM DC-to-DC Step-Down Converter with RESET

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

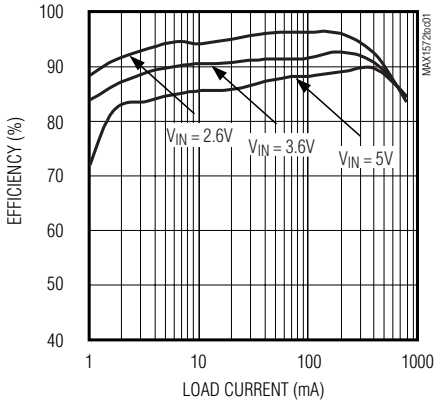
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN_ Logic Input Low				0.4	V
EN_ Logic Input Current				1	µA
$\overline{RESET}$ Threshold	Percent of nominal, measured at OUT	87		93	%
$\overline{RESET}$ Timer Delay Time	From V_{OUT} > 90% to $\overline{RESET}$ = HI	170		230	ms
$\overline{RESET}$ Output Low Level	I_{SINK} = 1mA			0.2	V
$\overline{RESET}$ Internal Pullup Resistance to OUT		9		20	kΩ

Note 2: Guaranteed by design, not production tested.
Note 3: Specifications to -40°C are guaranteed by design and not production tested.

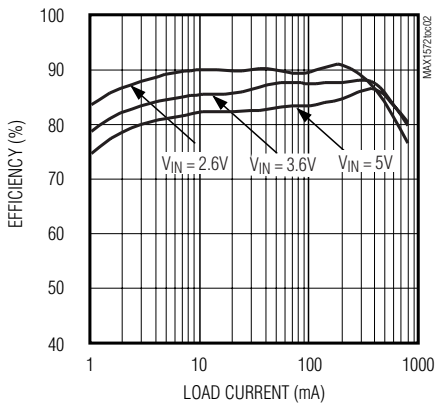
Typical Operating Characteristics

(V_{BATT} = 3.6V, V_{OUT} = 1.5V, EN1 = GND, EN2 = BATT, T_A = +25°C, unless otherwise noted.)

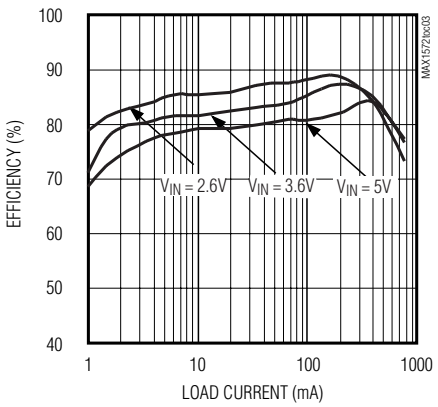
EFFICIENCY vs. LOAD CURRENT WITH 2.5V OUTPUT



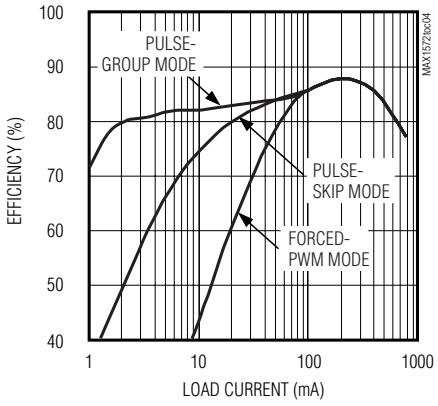
EFFICIENCY vs. LOAD CURRENT WITH 1.8V OUTPUT



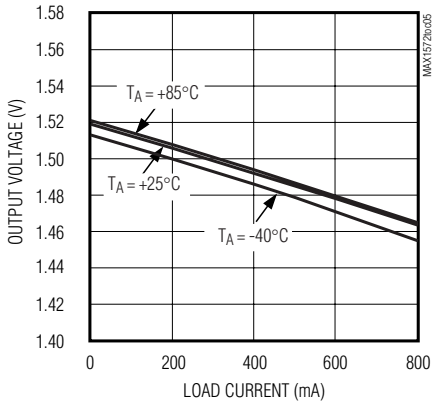
EFFICIENCY vs. LOAD CURRENT WITH 1.5V OUTPUT



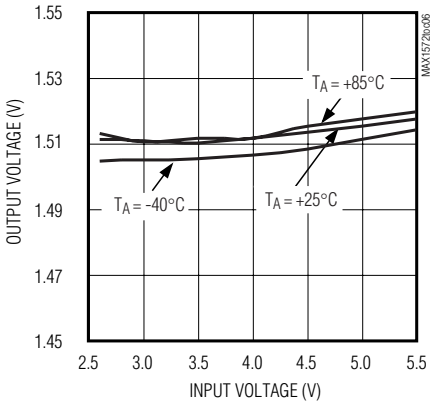
EFFICIENCY vs. LOAD CURRENT vs. MODE



OUTPUT VOLTAGE vs. LOAD CURRENT



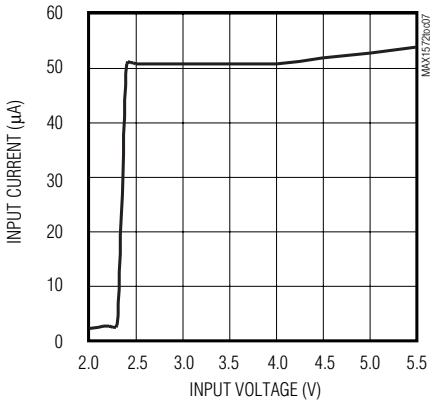
OUTPUT VOLTAGE vs. INPUT VOLTAGE WITH 100mA LOAD



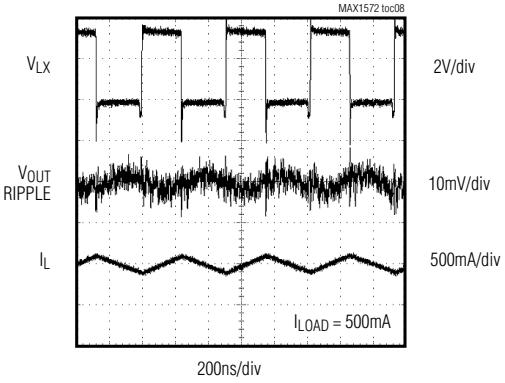
Typical Operating Characteristics (continued)

(V_{BATT} = 3.6V, V_{OUT} = 1.5V, EN1 = GND, EN2 = BATT, T_A = +25°C, unless otherwise noted.)

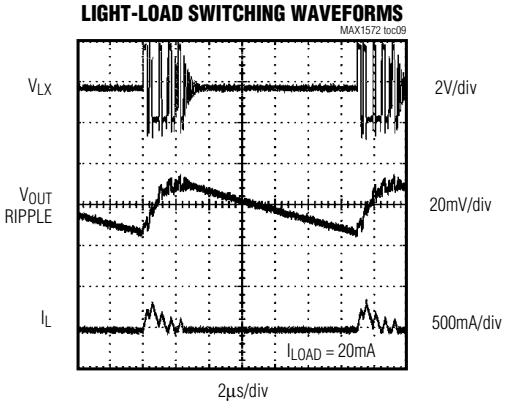
INPUT CURRENT vs. INPUT VOLTAGE WITH NO LOAD



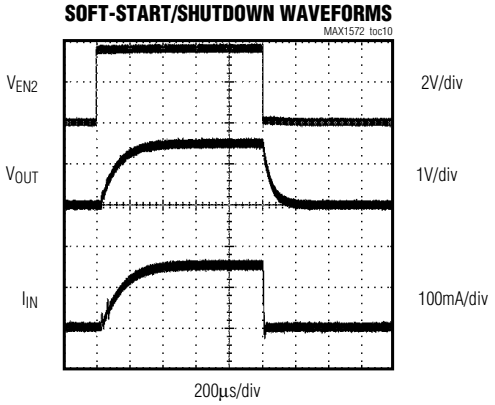
HEAVY-LOAD SWITCHING WAVEFORMS



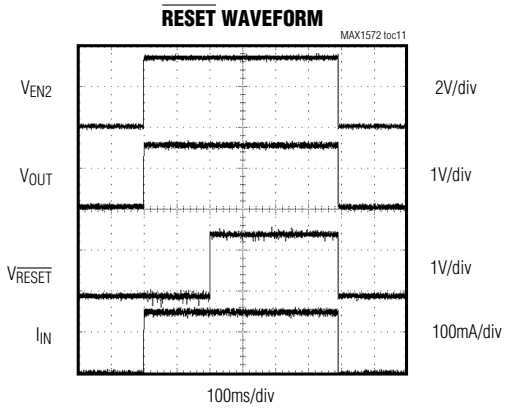
LIGHT-LOAD SWITCHING WAVEFORMS



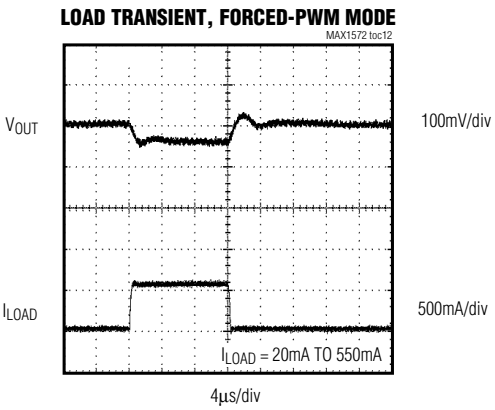
SOFT-START/SHUTDOWN WAVEFORMS



$\overline{\text{RESET}}$ WAVEFORM



LOAD TRANSIENT, FORCED-PWM MODE

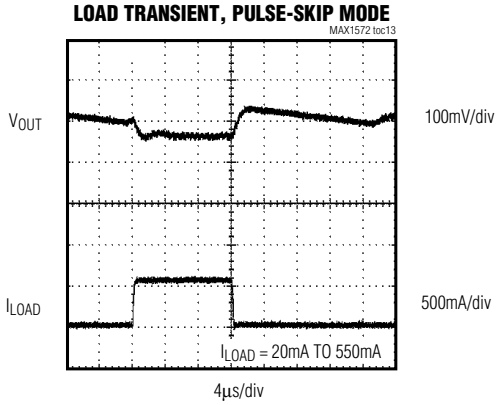


800mA, 2MHz, PWM DC-to-DC Step-Down Converter with RESET

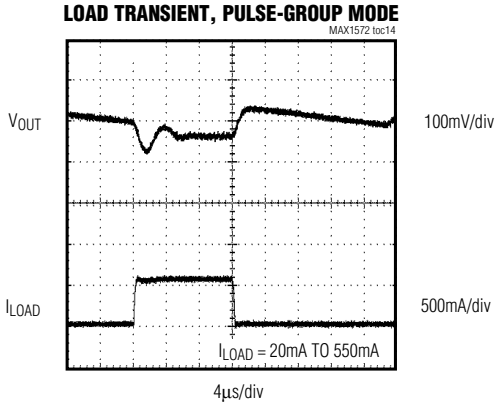
Typical Operating Characteristics (continued)

(V_{BATT} = 3.6V, V_{OUT} = 1.5V, EN1 = GND, EN2 = BATT, T_A = +25°C, unless otherwise noted.)

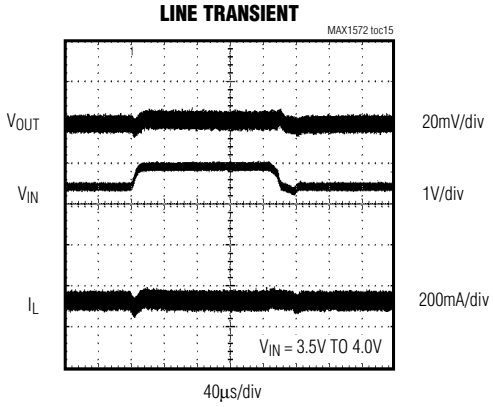
LOAD TRANSIENT, PULSE-SKIP MODE



LOAD TRANSIENT, PULSE-GROUP MODE



LINE TRANSIENT



Pin Description

PIN	NAME	FUNCTION
1	$\overline{RESET}$	Active-Low $\overline{RESET}$ Output. Open-drain output with internal 14kΩ pullup to OUT. $\overline{RESET}$ is driven LOW in shutdown.
2	SS	Soft-Start Control. Connect a capacitor from SS to GND to set the soft-start time. Use a 1000pF or larger capacitor to eliminate inrush current during startup. With greater than 10µF total output capacitance, increase C_{SS} to C_{OUT}/10,000 for soft-start. In shutdown, SS is discharged internally with 100Ω to GND.
3, 5, 11	GND	Ground. Connect all ground pins to the exposed paddle.
4	OUT	Output Sense Input. Connect to the output of the regulator. In shutdown, OUT is discharged internally with 14kΩ to GND.
6	EN2	Enable/Mode Control Input 2. See Table 1.
7	PGND	Power Ground. Connect to exposed paddle.
8	LX	Inductor Connection. LX is high impedance in shutdown.
9	BATT	Supply Voltage Input. Connect to a 2.6V to 5.5V source. Connect a 10µF ceramic capacitor from BATT to GND.
10	EN1	Enable/Mode Control Input 1. See Table 1.
12	ABATT	Analog Supply Input. Connect to BATT through a 10Ω resistor. Connect a 0.1µF capacitor from ABATT to GND.
—	Exposed Paddle	Exposed Paddle. Connect to GND and PGND.

Table 1. Mode Select Truth Table

MODE	EN1	EN2
Shutdown	0	0
Pulse group	0	1
Pulse skip	1	0
Forced PWM	1	1

A zero represents EN_ being driven low or connected to GND.
A 1 represents EN_ being driven high or connected to BATT.

Detailed Description

Figure 1 is the functional diagram.

PWM Control Scheme

The MAX1572 uses a 2MHz fixed-frequency, pulse-width-modulated (PWM), current-mode control scheme. The heart of the current-mode PWM controller is an open-loop comparator that compares the error amp voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side P-channel MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the

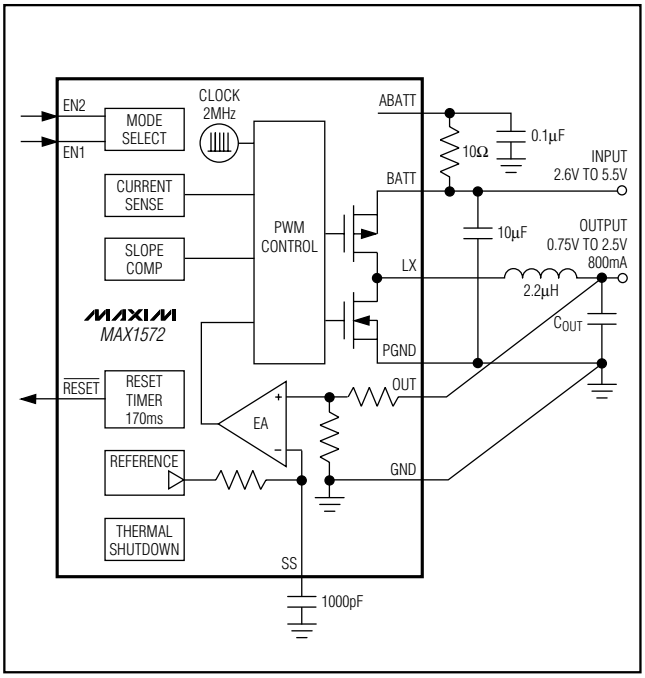


Figure 1. Functional Diagram

output and storing energy in the inductor's magnetic field. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (assuming that the inductor value is relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. This pushes the output LC filter pole, normally found in a voltage-mode PWM, to a higher frequency. To preserve inner-loop stability and eliminate inductor staircasing, an internal slope-compensation ramp is summed into the main PWM comparator. During the second half of the switching cycle (off-time), the internal high-side P-channel MOSFET turns off and the internal low-side N-channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit, the high-side MOSFET is turned off and the low-side MOSFET remains on for the remainder of the cycle to let the inductor current ramp down.

Pulse-Group Mode

Pulse-group mode is used to minimize the supply current with a light load. In pulse-group mode, the IC shuts off most internal circuitry when V_{OUT} is +0.8% above nominal regulation. When V_{OUT} drops below +0.8% of the nominal regulation voltage, the IC powers up its circuits and resumes switching.

Pulse-Skip Mode

Pulse-skip mode is also used to minimize the supply current with a light load. The difference between pulse-group and pulse-skip modes is that when V_{OUT} rises above the +0.8% regulation point, pulse-group mode stops switching and completely turns off a number of circuits. Under the same conditions, pulse-skip mode stops switching but leaves all circuits on. The delay coming out of pulse-skip mode is shorter than with pulse-group mode. In pulse-skip mode, the output voltage ripple is lower, and the load-transient response faster. However, the quiescent current is higher than in pulse-group mode.

Forced-PWM Mode

In forced-PWM mode, the MAX1572 operates at a constant 2MHz switching frequency without pulse skipping. This is desirable in noise-sensitive applications, since the output ripple is minimized and has a predictable noise spectrum. Forced-PWM mode requires higher supply current with light loads due to constant switching.

100% Duty-Cycle Operation

The MAX1572 can operate at 100% duty cycle. In this state, the high-side P-channel MOSFET is turned on (not switching). This occurs when the input voltage is close to the output voltage. The dropout voltage is the voltage drop due to the output current across the on-resistance of the internal P-channel MOSFET ($R_{DS(ON)P}$) and the inductor resistance (R_L):

$$V_{DROPOUT} = I_{OUT} \times (R_{DS(ON)P} + R_L)$$

$R_{DS(ON)P}$ is given in the *Electrical Characteristics* section. R_L, for a few recommended inductors, is given in Table 2.

Load-Transient Response/ Voltage Positioning

The MAX1572 uses voltage positioning that matches the load regulation to the voltage droop seen during load transients. In this way, the output voltage does not overshoot when the load is removed, which results in the total output-voltage variation being half as wide as in a conventional design. Figure 2 shows an example of a voltage-positioned and a nonvoltage-positioned load transient. Additionally, the MAX1572 uses a wide-bandwidth feedback loop to respond more quickly to a load transient than regulators using conventional integrating feedback loops.

The load line used to achieve voltage positioning is shown in Figure 3. This assumes a nominal operating point of 3.6V input at 300mA load.

Table 2. Recommended Inductors

MANUFACTURER	PART	VALUE (µH)	R_L (mΩ)	I_{SAT} (mA)	SIZE (mm)	SHIELDED
Murata	LQH32CN	2.2	97	790	2.5 x 3.2 x 2.0	No
Sumida	CDRH3D16	2.2	50	1200	3.8 x 3.8 x 1.8	Yes
	CDRH2D11	2.2	78	780	3.2 x 3.2 x 1.2	Yes
TOKO	D312F	2.2	170	1200	3.6 x 3.6 x 1.2	No
	D412F	2.2	140	1330	4.8 x 4.8 x 1.2	No

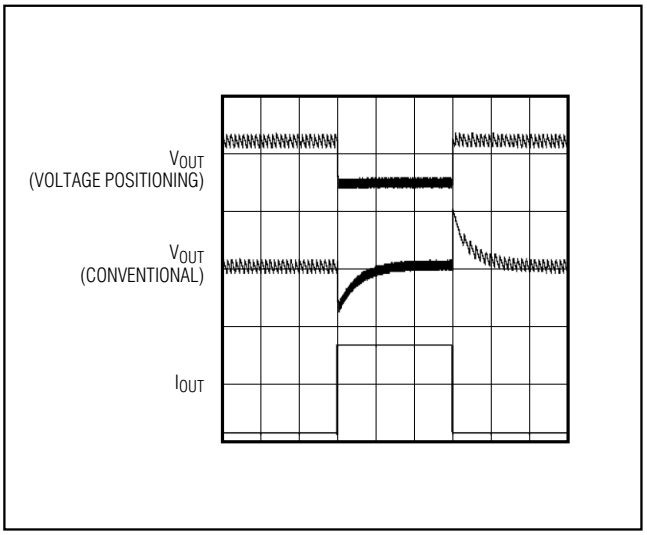


Figure 2. Load Transient Response, With and Without Voltage Positioning

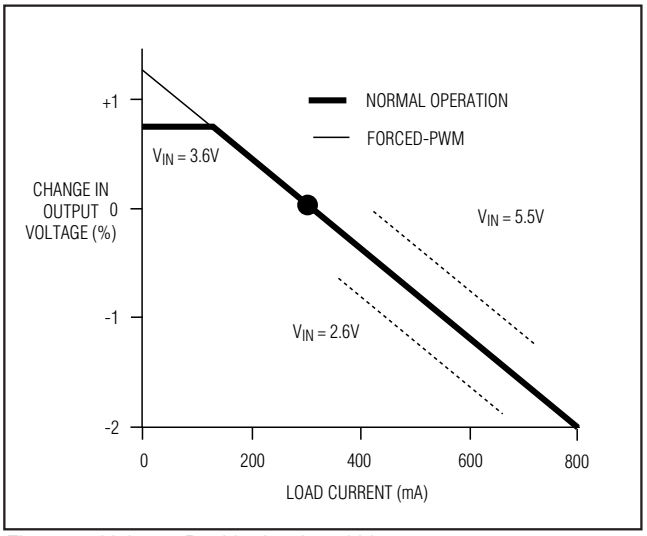


Figure 3. Voltage-Positioning Load Line

Soft-Start

Soft-start is used to prevent input-current overshoot during startup. For most applications using a 10µF output capacitor, connect a 1000pF capacitor from SS to GND. If a larger output capacitor is used, then use the following formula to find the value of the soft-start capacitor needed to prevent input-current overshoot:

$$C_{SS} = C_{OUT} / 10^4$$

During soft-start, the output voltage rises from 0 to $V_{OUT(nom)}$ with a time constant equal to C_{SS} times 100kΩ (see the *Typical Operating Characteristics*).

170ms RESET

RESET is an open-drain output with an internal 14kΩ pullup resistor to OUT. During startup, RESET is held low until 200ms (typ) after the output voltage reaches 90% of its nominal regulation voltage. When the output voltage drops below 90% of its nominal regulation voltage, RESET pulls low again. See the *Typical Operating Characteristics* section for RESET waveforms during startup and shutdown.

Applications Information

Inductor Selection

A 2.2µH inductor with a saturation current of at least 1A is recommended for full-load (800mA) applications. For lower load currents, the inductor current rating may be reduced. For most applications, use an inductor with a current rating 1.25 times the maximum required output current. For maximum efficiency, the inductor's DC resistance should be as low as possible. See Table 2 for recommended inductors and manufacturers.

Capacitor Selection

Ceramic 10µF input and output capacitors are recommended for most applications. For output voltages below 1.5V, output capacitance should be increased to 22µF. For best stability over a wide temperature range, use capacitors with an X5R or better dielectric.

ABATT Input Filter

In normal applications, an RC filter on ABATT keeps power-supply noise from entering the IC. Connect a 10Ω resistor between BATT and ABATT and connect a 0.1µF capacitor from ABATT to GND.

PC Board Layout and Routing

Due to fast-switching waveforms and high-current paths, careful PC board layout is required. An evaluation kit (MAX1572EVKIT) is available to speed design.

When laying out a board, minimize trace lengths between the IC, the inductor, the input capacitor, and the output capacitor. Keep these traces short, direct, and wide. Keep noisy traces, such as the LX node trace, away from OUT. The input bypass capacitors should be placed as close to the IC as possible. Connect PGND and GND directly to the exposed paddle underneath the IC. The ground connections of the input and output capacitors should be as close together as possible.

800mA, 2MHz, PWM DC-to-DC Step-Down Converter with RESET

Selector Guide

PART	V_{OUT} (V)	TOP MARK
MAX1572ETC075	0.75	AABW
MAX1572ETC130	1.30	AACW
MAX1572ETC150	1.50	AABX
MAX1572ETC180	1.80	AABY
MAX1572ETC250	2.50	AABZ
MAX1572ETCxyz	*	—

**xyz is for output voltage (e.g., MAX1572ETC165 has a 1.65V output).*

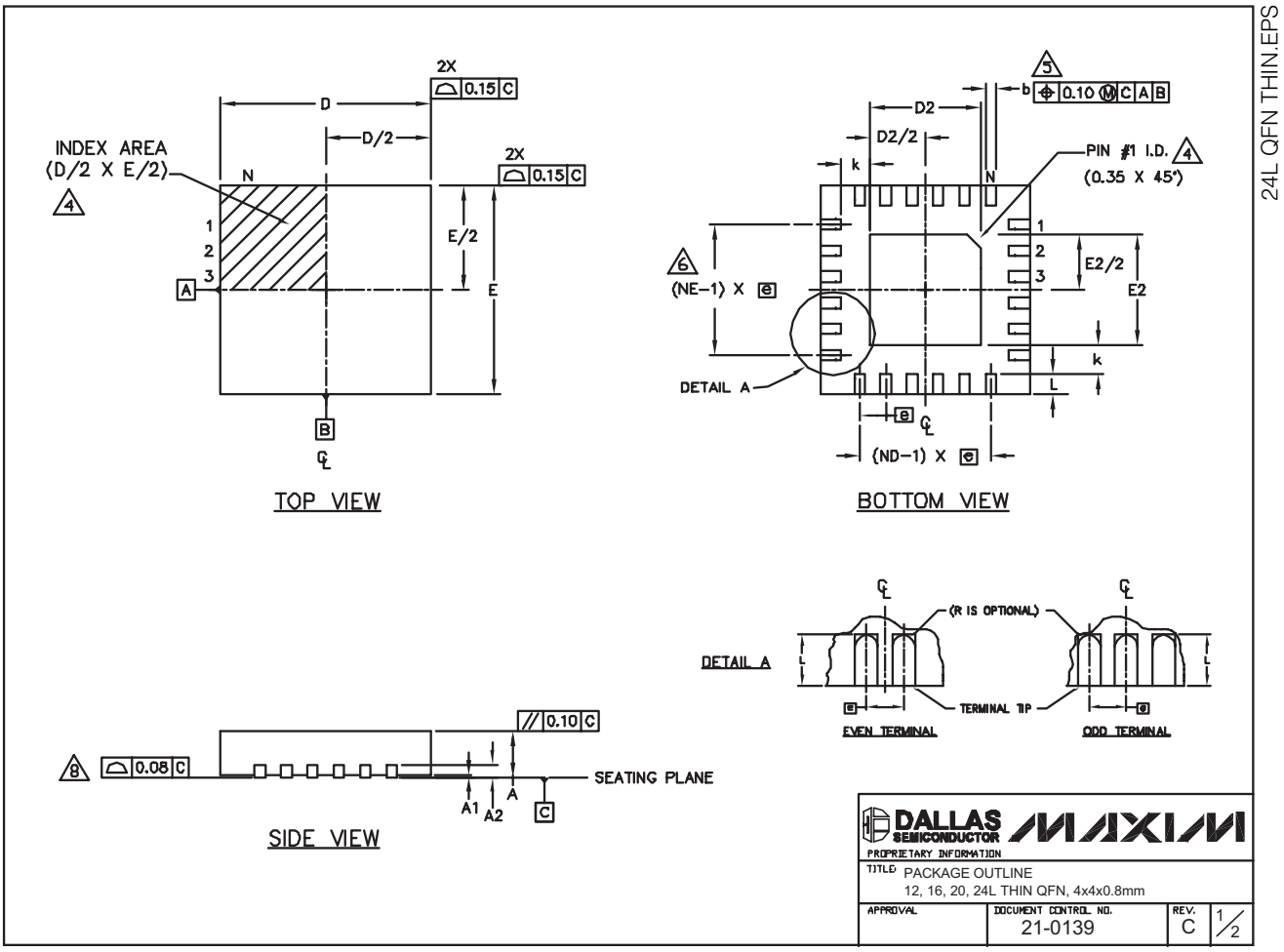
Chip Information

TRANSISTOR COUNT: 3697

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	C	2/2