

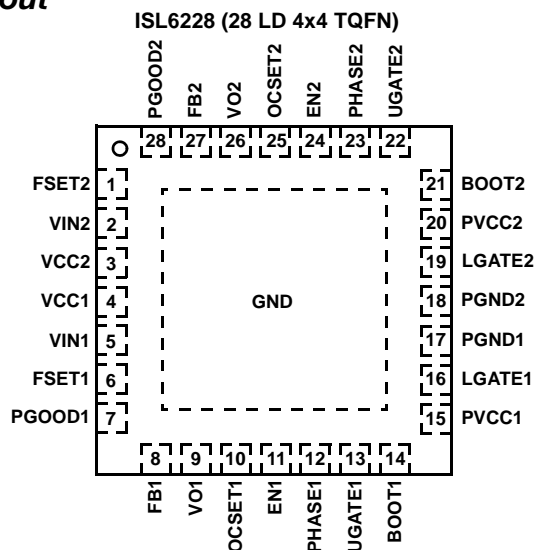
## High-Performance Dual-Output Buck Controller for Notebook Applications

The ISL6228 IC is a dual channel synchronous-buck PWM controller featuring Intersil's Robust Ripple Regulator (R<sup>3</sup>) technology that delivers truly superior dynamic response to input voltage and output load transients. Integrated MOSFET drivers and bootstrap diodes result in fewer components and smaller implementation area.

Intersil's R<sup>3</sup> technology combines the best features of fixed-frequency and hysteretic PWMs while eliminating many of their shortcomings. R<sup>3</sup> technology employs an innovative modulator that synthesizes an AC ripple voltage signal  $V_R$ , analogous to the output inductor ripple current. The AC signal  $V_R$  enters a window comparator where the lower threshold is the error amplifier output  $V_{COMP}$ , and the upper threshold is a programmable voltage reference  $V_W$ , resulting in generation of the PWM signal. The voltage reference  $V_W$  sets the steady-state PWM frequency. Both edges of the PWM can be modulated in response to input voltage transients and output load transients, much faster than conventional fixed-frequency PWM controllers. Unlike a conventional hysteretic converter, each channel of the ISL6228 has an error amplifier that provides  $\pm 1\%$  voltage regulation at the FB pin.

The ISL6228 has a 1.5ms digital soft-start and can be started into a pre-biased output voltage. A resistor divider is used to program the output voltage setpoint. The ISL6228 operates in continuous-conduction-mode (CCM) in heavy load, and in diode-emulation-mode (DEM) in light load to improve light-load efficiency. In CCM, the controller always operates as a synchronous rectifier. In DEM, the low-side MOSFET is permitted to stay off, blocking negative current flow into the low-side MOSFET from the output inductor.

### Pinout



### Features

- High performance R<sup>3</sup> technology
- Fast transient response
- $\pm 1\%$  regulation accuracy:  $-40^\circ\text{C}$  to  $+100^\circ\text{C}$
- Individual power stage input rail for each channel
- Wide input voltage range:  $+3.3\text{V}$  to  $+25\text{V}$
- Output voltage range:  $+0.6\text{V}$  to  $+5\text{V}$
- Diode emulation mode for increased light load efficiency
- Programmable PWM frequency: 200kHz to 600kHz
- Pre-biased output start-up capability
- Integrated MOSFET drivers and bootstrap diode
- Internal digital soft-start
- Power good monitor
  - Undervoltage protection
  - Soft crowbar overvoltage protection
  - Inductor DCR overcurrent protection
  - Over-temperature protection
  - Fault identification by PGOOD pull-down resistance
- Pb-free (RoHS compliant)

### Applications

- General purpose switching buck regulators
- PCI express graphical processing unit
- Auxiliary power rail
- VRM
- Network adaptor

### Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6228HRTZ	6228HRTZ	-10 to +100	28 Ld 4x4 TQFN	L28.4x4A
ISL6228HRTZ-T*	6228HRTZ	-10 to +100	28 Ld 4x4 TQFN Tape and Reel	L28.4x4A
ISL6228IRTZ	6228IRTZ	-40 to +100	28 Ld 4x4 TQFN	L28.4x4A
ISL6228IRTZ-T*	6228IRTZ	-40 to +100	28 Ld 4x4 TQFN Tape and Reel	L28.4x4A

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram

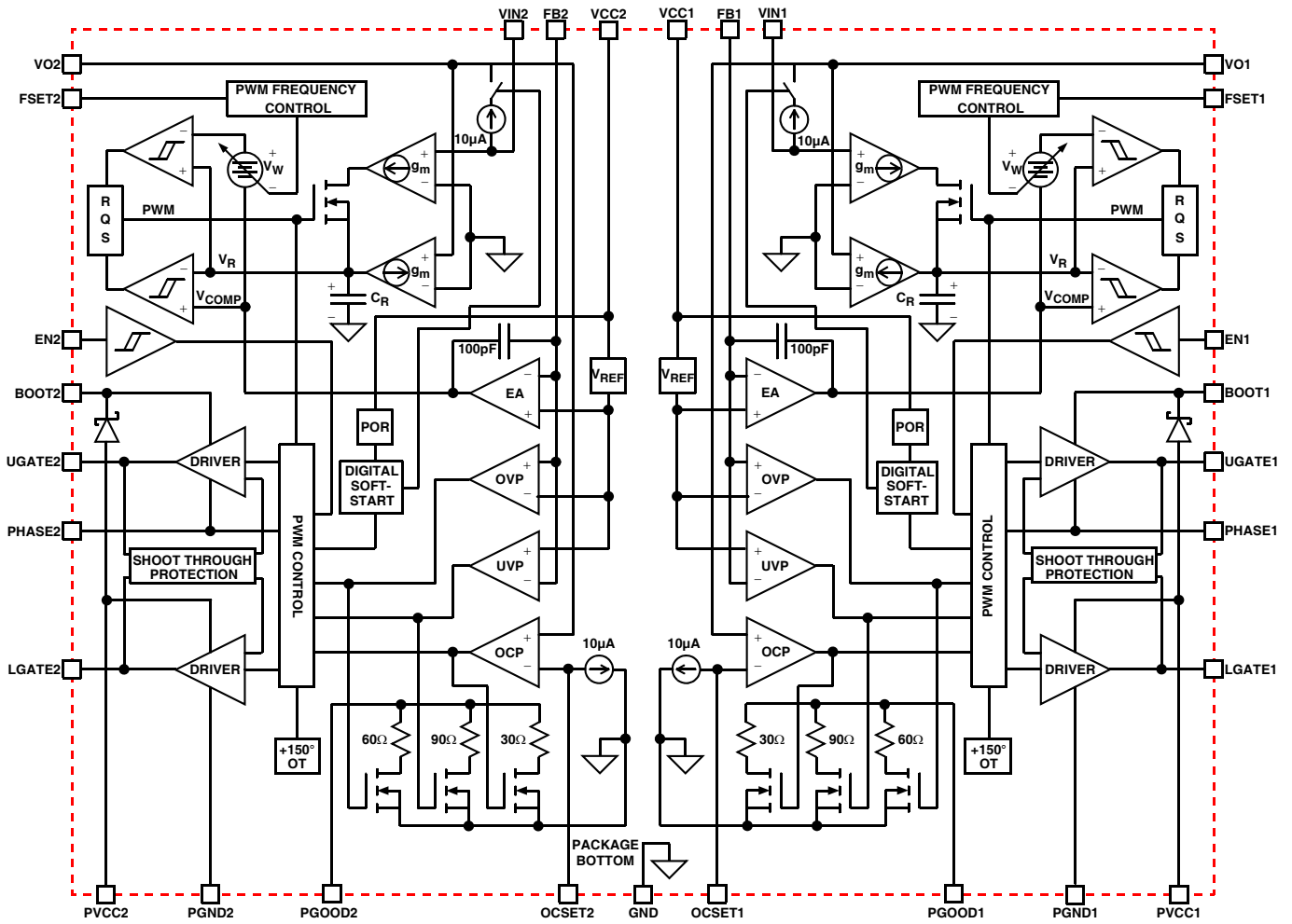
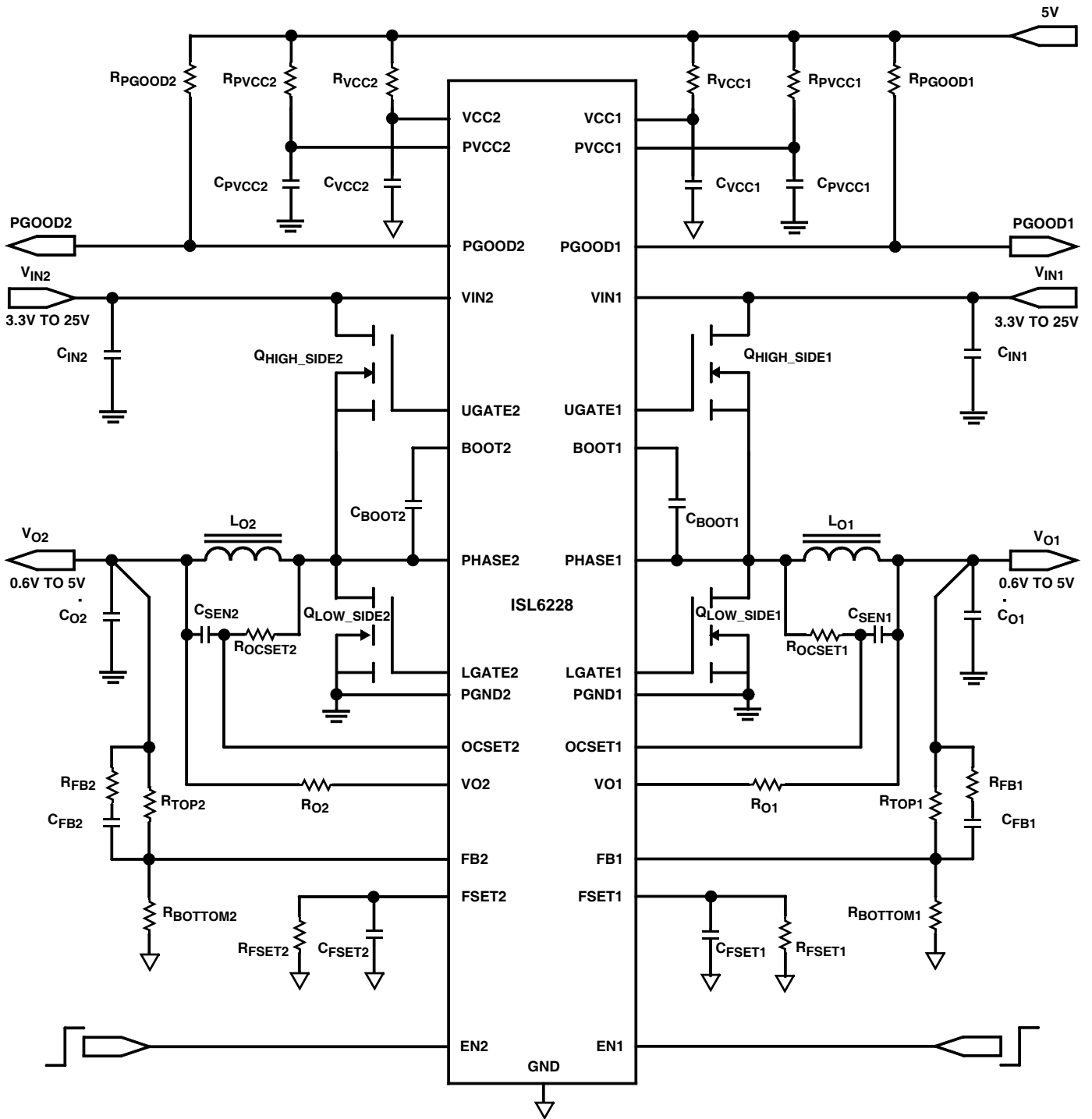


FIGURE 1. SCHEMATIC BLOCK DIAGRAM

Typical Application



**Absolute Voltage Ratings**

VIN <sub>1,2</sub> to GND	-0.3V to +28V
VCC, PGOOD <sub>1,2</sub> to GND	-0.3V to +7.0V
PVCC to GND	-0.3V to +7.0V
EN <sub>1,2</sub>	-0.3V to GND, VCC +3.3V
VO <sub>1,2</sub> , FB <sub>1,2</sub> , FSET <sub>1,2</sub>	-0.3V to GND, VCC +0.3V
PHASE <sub>1,2</sub> to GND	(DC) -0.3V to +28V
(<100ns Pulse Width, 10μJ)	-5.0V
BOOT <sub>1,2</sub> to GND	-0.3V to +33V
BOOT <sub>1,2</sub> to PHASE <sub>1,2</sub>	-0.3V to +7V
UGATE <sub>1,2</sub>	(DC) -0.3V to PHASE <sub>1,2</sub> , BOOT <sub>1,2</sub> +0.3V
(<200ns Pulse Width, 20μJ)	-4.0V
LGATE <sub>1,2</sub>	(DC) -0.3V to GND, PVCC +0.3V
(<100ns Pulse Width, 4μJ)	-2.0V

**Thermal Information**

Thermal Resistance (Typical, Notes 1, 2)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
TQFN Package	40	3
Junction Temperature Range	-55°C to +150°C	
Operating Temperature Range	-40°C to +100°C	
Storage Temperature	-65°C to +150°C	
Pb-free reflow profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

**Recommended Operating Conditions**

Ambient Temperature Range	-10°C to +100°C
Supply Voltage (VIN to GND)	3.3V to 25V
VCC to GND	.5V ±5%
PVCC to GND	.5V ±5%

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

1.  $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.
3. Limits established by characterization and are not production tested.

**Electrical Specifications**

These specifications apply for  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ; All typical specifications  $T_A = +25^\circ\text{C}$ , VCC = 5V, PVCC = 5V; Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN</b>						
VIN Input Bias Current	$I_{VIN}$	EN = 5V, VIN = 15V	-	16	-	μA
VIN Shutdown Current	$I_{VIN\_SHDN}$	EN = GND, VIN = 25V	-	0.1	1.0	μA
<b>VCC and PVCC</b>						
VCC Input Bias Current in Single-Channel	$I_{VCC\_S}$	EN <sub>1</sub> = 5V, FB <sub>1</sub> = 0.65V, VIN <sub>1</sub> = 3.3V to 25V, EN <sub>2</sub> = GND, FB <sub>2</sub> = GND, VIN <sub>2</sub> = GND	-	1	-	mA
VCC Input Bias Current in Dual Channel	$I_{VCC\_D}$	EN <sub>1</sub> = 5V, FB <sub>1</sub> = 0.65V, VIN <sub>1</sub> = 3.3V to 25V, EN <sub>2</sub> = 5V, FB <sub>2</sub> = 0.65V, VIN <sub>2</sub> = 3.3V to 25V	-	2	-	mA
VCC Shutdown Current	$I_{VCC\_SHDN}$	EN <sub>1</sub> = GND, EN <sub>2</sub> = GND, VCC = 5V	-	0.1	1.0	μA
PVCC Shutdown Current	$I_{PVCC\_SHDN}$	EN <sub>1</sub> = GND, EN <sub>2</sub> = GND, PVCC = 5V	-	0.1	1.0	μA
<b>VCC POR THRESHOLD</b>						
Rising VCC POR Threshold Voltage	$V_{VCC\_THR}$		4.33	4.45	4.55	V
		$T_A = -10^\circ\text{C}$ to $+100^\circ\text{C}$	4.35	4.45	4.55	V
Falling VCC POR Threshold Voltage	$V_{VCC\_THF}$		4.08	4.20	4.30	V
		$T_A = -10^\circ\text{C}$ to $+100^\circ\text{C}$	4.10	4.20	4.30	V
<b>REGULATION</b>						
Reference Voltage	$V_{REF}$		-	0.6	-	V
Regulation Accuracy		Close loop	-1	-	+1	%
<b>PWM</b>						
Frequency Range	$f_{SW}$		200	-	600	kHz
Frequency-Set Accuracy		$f_{SW} = 300\text{kHz}$	-12	-	+12	%
VO Range	$V_{VO}$		0.60	-	5	V
VO Input Leakage	$I_{VO}$	EN = 5V, VO = 0.60V	-	1	-	μA
		EN = 5V, VO = 5V	-	7.0	-	μA
		EN = 0V, VO = 5V	-	0.1	-	μA

**Electrical Specifications**

These specifications apply for  $T_A = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ ; All typical specifications  $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $PV_{CC} = 5\text{V}$ ; Parameters with MIN and/or MAX limits are 100% tested at  $+25^{\circ}\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ERROR AMPLIFIER</b>						
FB Input Bias Current	$I_{FB}$	FB = 0.60V	-33	-	15	nA
		FB = 0.60V $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	-35	-	15	nA
<b>POWER GOOD</b>						
PGOOD Pull-Down Impedance	$R_{PG\_SS}$	PGOOD = 5mA Sink	70	95	125	$\Omega$
	$R_{PG\_SS}$	PGOOD = 5mA Sink $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	75	95	125	$\Omega$
	$R_{PG\_UV}$	PGOOD = 5mA Sink	70	95	125	$\Omega$
	$R_{PG\_UV}$	PGOOD = 5mA Sink $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	75	95	125	$\Omega$
	$R_{PG\_OV}$	PGOOD = 5mA Sink	45	63	85	$\Omega$
	$R_{PG\_OV}$	PGOOD = 5mA Sink $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	50	63	85	$\Omega$
	$R_{PG\_OC}$	PGOOD = 5mA Sink	22	32	45	$\Omega$
	$R_{PG\_OC}$	PGOOD = 5mA Sink $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	25	32	45	$\Omega$
PGOOD Leakage Current	$I_{PGOOD}$	PGOOD = 5V	-	0.1	1.0	$\mu\text{A}$
PGOOD Maximum Sink Current (Note 3)			-	5.0	-	mA
PGOOD Soft-Start Delay	$t_{SS}$	EN High to PGOOD High	2.20	2.75	3.50	ms
<b>GATE DRIVER</b>						
UGATE Pull-Up Resistance (Note 3)	$R_{UGPU}$	200mA Source Current	-	1.0	1.5	$\Omega$
UGATE Source Current (Note 3)	$I_{UGSRC}$	UGATE - PHASE = 2.5V	-	2.0	-	A
UGATE Sink Resistance (Note 3)	$R_{UGPD}$	250mA Sink Current	-	1.0	1.5	$\Omega$
UGATE Sink Current (Note 3)	$I_{UGSNK}$	UGATE - PHASE = 2.5V	-	2.0	-	A
LGATE Pull-Up Resistance (Note 3)	$R_{LGPU}$	250mA Source Current	-	1.0	1.5	$\Omega$
LGATE Source Current (Note 3)	$I_{LGSRC}$	LGATE - PGND = 2.5V	-	2.0	-	A
LGATE Sink Resistance (Note 3)	$R_{LGPD}$	250mA Sink Current	-	0.5	0.9	$\Omega$
LGATE Sink Current (Note 3)	$I_{LGSNK}$	LGATE - PGND = 2.5V	-	4.0	-	A
UGATE to LGATE Deadtime	$t_{UGFLGR}$	UGATE falling to LGATE rising, no load	-	21	-	ns
LGATE to UGATE Deadtime	$t_{LGFUGR}$	LGATE falling to UGATE rising, no load	-	21	-	ns
<b>BOOTSTRAP DIODE</b>						
Forward Voltage	$V_F$	$PV_{CC} = 5\text{V}$ , $I_F = 2\text{mA}$	-	0.58	-	V
Reverse Leakage	$I_R$	$V_R = 25\text{V}$	-	0.2	-	$\mu\text{A}$
<b>CONTROL INPUTS</b>						
EN High Threshold	$V_{ENTHR}$		2.0	-	-	V
EN Low Threshold	$V_{ENTHF}$		-	-	1.0	V
EN Leakage	$I_{ENL}$	EN = 0V	-	0.1	1.0	$\mu\text{A}$
		EN = 5.0V	1.4	2	2.5	$\mu\text{A}$
		EN = 5.0V $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	1.5	2	2.5	$\mu\text{A}$
<b>PROTECTION</b>						
OCSET-VO Threshold	$V_{OCSETTHR}$		-1.75	0	1.75	mV
OCSET 10 $\mu\text{A}$ Current Source	$I_{OCSET}$	EN = 5V	8.8	10	10.5	$\mu\text{A}$
		EN = 5V $T_A = -10^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	9	10	10.5	$\mu\text{A}$
		EN = 0V	-	0	-	$\mu\text{A}$
OCSET 10 $\mu\text{A}$ Current Source Impedance	$R_{OCSETIMP}$	EN = 5V, OCSET = 1.2V	-	600	-	k $\Omega$
UVP Threshold	$V_{UV}$		81	86	87	%
OVP Rising Threshold	$V_{OVR}$		113	116	120	%
OVP Falling Threshold	$V_{OVF}$		100	102	106	%

**Electrical Specifications** These specifications apply for  $T_A = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ ; All typical specifications  $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $PV_{CC} = 5\text{V}$ ; Parameters with MIN and/or MAX limits are 100% tested at  $+25^{\circ}\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTP Rising Threshold (Note 3)	$T_{OTR}$		-	150	-	$^{\circ}\text{C}$
OTP Hysteresis (Note 3)	$T_{OTHYS}$		-	25	-	$^{\circ}\text{C}$

## Functional Pin Descriptions

### GND (Bottom Pad)

Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

### FSET2 (Pin 1)

The FSET2 pin programs the PWM switching frequency of Channel 2. Program the desired PWM frequency with a resistor and a capacitor connected across the FSET2 and GND pins.

### VIN2 (Pin 2)

The VIN2 pin measures the input voltage of the Channel 2 converter. It is a required input to the Channel 2  $R^3$  PWM modulator. Connect the VIN2 pin to the drain of the Channel 2 high-side MOSFET.

### VCC2 (Pin 3)

The VCC2 pin is the input bias voltage for Channel 2. Connect +5V to the VCC2 pin. Decouple with at least  $1\mu\text{F}$  of a MLCC capacitor from the VCC2 pin to the GND pin.

### VCC1 (Pin 4)

The VCC1 pin is the input bias voltage for Channel 1. Connect +5V to the VCC1 pin. Decouple with at least  $1\mu\text{F}$  of a MLCC capacitor from the VCC1 pin to the GND pin.

### VIN1 (Pin 5)

The VIN1 pin measures the input voltage of the Channel 1 converter. It is a required input to the Channel 1  $R^3$  PWM modulator. Connect the VIN1 pin to the drain of the Channel 1 high-side MOSFET.

### FSET1 (Pin 6)

The FSET1 pin programs the PWM switching frequency of Channel 1. Program the desired PWM frequency with a resistor and a capacitor connected across the FSET1 and GND pins.

### PGOOD1 (Pin 7)

The PGOOD1 pin is an open-drain output that indicates when the Channel 1 converter is able to supply regulated voltage. Connect the PGOOD1 pin to +5V through a pull-up resistor.

### FB1 (Pin 8)

The FB1 pin is the inverting input of the control-loop error amplifier for Channel 1. The Channel 1 converter output voltage regulates to 600mV from the FB1 pin to the GND pin. Program the desired output voltage with a resistor network

connected across the VO1, FB1, and GND pins. Select the resistor values such that FB1 to GND is 600mV when the converter output voltage is at the programmed regulation value.

### VO1 (Pin 9)

The VO1 pin measures the Channel 1 converter output voltage and is used as an input to the Channel 1  $R^3$  PWM modulator. It also serves as part of Channel 1 inductor current sensing and the OCP overcurrent fault protection circuit.

### OCSET1 (Pin 10)

The OCSET1 pin measures the Channel 1 inductor current and programs the threshold of the OCP overcurrent fault protection.

### EN1 (Pin 11)

The EN1 pin is the on/off switch of Channel 1. The soft-start sequence begins when the EN1 pin is pulled above the rising threshold voltage  $V_{ENTHR}$  and VCC1 is above the power-on reset (POR) rising threshold voltage  $V_{VCC\_THR}$ . When the EN1 pin is pulled below the falling threshold voltage  $V_{ENTHF}$  PWM1 immediately stops.

### PHASE1 (Pin 12)

The PHASE1 pin is the current return path for the Channel 1 high-side MOSFET gate driver. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of the Channel 1 converter.

### UGATE1 (Pin 13)

The UGATE1 pin is the output of the Channel 1 high-side MOSFET gate driver. Connect the UGATE1 pin to the gate of the Channel 1 converter high-side MOSFET.

### BOOT1 (Pin 14)

The BOOT1 pin stores the input voltage for the Channel 1 high-side MOSFET gate driver. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the PVCC1 pin to the BOOT1 pin, each time the PHASE1 pin drops below PVCC1 minus the voltage dropped across the internal boot diode.

### PVCC1 (Pin 15)

The PVCC1 pin is the input voltage bias for the Channel 1 low-side MOSFET gate drivers. Connect +5V to the PVCC1

pin. Decouple with at least 1  $\mu\text{F}$  of an MLCC capacitor across the PVCC1 and PGND1 pin.

#### **LGATE1 (Pin 16)**

The LGATE1 pin is the output of the Channel 1 converter low-side MOSFET gate driver. Connect the LGATE1 pin to the gate of the Channel 1 converter low-side MOSFET.

#### **PGND1 (Pin 17)**

The PGND1 pin is the current return path for the Channel 1 converter low-side MOSFET gate driver. Connect the PGND1 pin to the source of the Channel 1 converter low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE1 pin to the gate of the Channel 1 converter low-side MOSFET.

#### **PGND2 (Pin 18)**

The PGND2 pin is the current return path for the Channel 2 converter low-side MOSFET gate driver. Connect the PGND2 pin to the source of the Channel 2 converter low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE2 pin to the gate of the Channel 2 converter low-side MOSFET.

#### **LGATE2 (Pin 19)**

The LGATE2 pin is the output of the Channel 2 converter low-side MOSFET gate driver. Connect to the gate of the Channel 2 converter low-side MOSFET.

#### **PVCC2 (Pin 20)**

The PVCC2 pin is the input voltage bias for the Channel 2 low-side MOSFET gate drivers. Connect +5V to the PVCC2 pin. Decouple with at least 1  $\mu\text{F}$  of an MLCC capacitor across the PVCC2 and PGND2 pin.

#### **BOOT2 (Pin 21)**

The BOOT2 pin stores the input voltage for the Channel 2 high-side MOSFET gate driver. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the PVCC2 pin to the BOOT2 pin, each time the PHASE2 pin drops below PVCC2 minus the voltage dropped across the internal boot diode.

#### **UGATE2 (Pin 22)**

The UGATE2 pin is the output of the Channel 2 high-side MOSFET gate driver. Connect to the gate of the Channel 2 converter high-side MOSFET.

#### **PHASE2 (Pin 23)**

The PHASE2 pin is the current return path for the Channel 2 high-side MOSFET gate driver. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of the Channel 2 converter.

#### **EN2 (Pin 24)**

The EN2 pin is the on/off switch of Channel 2. The soft-start sequence begins when the EN2 pin is pulled above the rising threshold voltage  $V_{ENTHR}$  and VCC2 is above the power-on reset (POR) rising threshold voltage  $V_{VCC\_THR}$ . When the EN2 pin is pulled below the falling threshold voltage  $V_{ENTHF}$ , PWM2 immediately stops.

#### **OCSET2 (Pin 25)**

The OCSET2 pin measures the Channel 2 inductor current and programs the threshold of the OCP overcurrent fault protection.

#### **VO2 (Pin 26)**

The VO2 pin measures the Channel 2 converter output voltage and is used as an input to the Channel 2  $R^3$  PWM modulator. It also serves as part of Channel 2 inductor current sensing and the OCP overcurrent fault protection circuit.

#### **FB2 (Pin 27)**

The FB2 pin is the inverting input of the control-loop error amplifier for Channel 2. The Channel 2 converter output voltage regulates to 600mV from the FB2 pin to the GND pin. Program the desired output voltage with a resistor network connected across the VO2, FB2, and GND pins. Select the resistor values such that FB2 to GND is 600mV when the converter output voltage is at the programmed regulation value.

#### **PGOOD2 (Pin 28)**

The PGOOD2 pin is an open-drain output that indicates when the Channel 2 converter is able to supply regulated voltage. Connect the PGOOD2 pin to +5V through a pull-up resistor.

## **Theory of Operation**

### **Two Separate Channels**

The ISL6228 is a dual channel controller. Pins 4~17 are dedicated to Channel 1, and pins 1~3 and pins 18~28 are dedicated to Channel 2. The two channels are identical and almost entirely independent, with the exception of sharing the GND pin. Unless otherwise stated, only an individual channel is discussed, and the conclusion applies to both channels.

### **Modulator**

The ISL6228 modulator features Intersil's  $R^3$  technology, a hybrid of fixed frequency PWM control and variable frequency hysteretic control. Intersil's  $R^3$  technology can simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients. The  $R^3$  modulator synthesizes an AC signal  $V_R$ , which is an analog representation of the output inductor ripple current. The duty-cycle of  $V_R$  is the result of charge and discharge current through a ripple capacitor  $C_R$ . The

current through  $C_R$  is provided by a transconductance amplifier  $g_m$  that measures the  $V_{IN}$  and  $V_O$  pin voltages. The positive slope of  $V_R$  can be written as Equation 1:

$$V_{RPOS} = (g_m) \cdot (V_{IN} - V_{OUT}) / C_R \quad (\text{EQ. 1})$$

The negative slope of  $V_R$  can be written as Equation 2:

$$V_{RNEG} = g_m \cdot V_{OUT} / C_R \quad (\text{EQ. 2})$$

Where  $g_m$  is the gain of the transconductance amplifier.

A window voltage  $V_W$  is referenced with respect to the error amplifier output voltage  $V_{COMP}$ , creating an envelope into which the ripple voltage  $V_R$  is compared. The amplitude of  $V_W$  is set by a resistor connected across the FSET and GND pins. The  $V_R$ ,  $V_{COMP}$ , and  $V_W$  signals feed into a window comparator in which  $V_{COMP}$  is the lower threshold voltage and  $V_W$  is the higher threshold voltage. Figure 2 shows PWM pulses being generated as  $V_R$  traverses the  $V_W$  and  $V_{COMP}$  thresholds. The PWM switching frequency is proportional to the slow rates of the positive and negative slopes of  $V_R$ ; it is inversely proportional to the voltage between  $V_W$  and  $V_{COMP}$ .

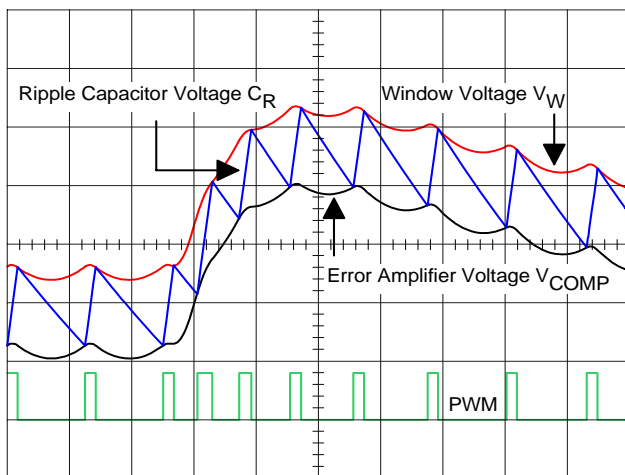


FIGURE 2. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

### Power-On Reset

The ISL6228 is disabled until the voltage at the VCC pin has increased above the rising power-on reset (POR)  $V_{CCR}$  threshold voltage. The controller will be disabled when the voltage at the VCC pin decreases below the falling POR  $V_{CCF}$  threshold voltage.

### EN, Soft-Start and PGOOD

The ISL6228 uses a digital soft-start circuit to ramp the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of the soft-start sequence has been selected to limit the in-rush current through the output capacitors as they charge to the desired regulation voltage. When the EN pin is pulled above the rising EN threshold voltage  $V_{ENTHR}$ , the PGOOD

Soft-Start Delay  $t_{SS}$  begins and the output voltage begins to rise. The FB pin ramps to 0.6V in approximately 1.5ms and the PGOOD pin goes to high impedance approximately 1.25ms after the FB pin voltage reaches 0.6V.

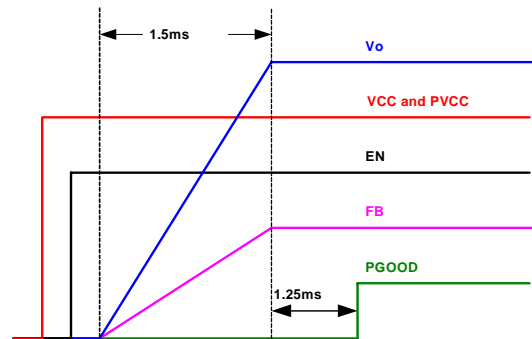


FIGURE 3. SOFT-START SEQUENCE

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. The PGOOD pin is an undefined impedance if  $V_{CC}$  has not reached the rising POR threshold  $V_{CCR}$ , or if  $V_{CC}$  is below the falling POR threshold  $V_{CCF}$ . The ISL6228 features a unique fault-identification capability that can drastically reduce trouble-shooting time and effort. The pull-down resistance of the PGOOD pin corresponds to the fault status of the controller. The PGOOD pull-down resistance is  $95\Omega$  during soft-start or if an UVP occurs,  $30\Omega$  for an OCP, or  $60\Omega$  for OVP.

TABLE 1. PGOOD PULL-DOWN RESISTANCE

CONDITION	PGOOD RESISTANCE
VCC Below POR	Undefined
Soft-start or Undervoltage	$90\Omega$
Overshoot	$60\Omega$
Overcurrent	$30\Omega$

### MOSFET Gate-Drive Outputs LGATE and UGATE

The ISL6228 has internal gate-drivers for the high-side and low-side N-Channel MOSFETs. The low-side gate-drivers are optimized for low duty-cycle applications where the low-side MOSFET conduction losses are dominant, requiring a low  $r_{DS(ON)}$  MOSFET. The LGATE pull-down resistance is small in order to clamp the gate of the MOSFET below the  $V_{GS(th)}$  at turnoff. The current transient through the gate at turn-off can be considerable because the gate charge of a low  $r_{DS(ON)}$  MOSFET can be large. Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 4 is extended by the additional period that the falling gate voltage stays above the 1V threshold. The typical dead-time is 21ns. The high-side gate-driver output voltage is measured across the UGATE and PHASE pins while the low-side gate-driver output voltage is measured across the LGATE and PGND



pins. The power for the LGATE gate-driver is sourced directly from the PVCC pin. The power for the UGATE gate-driver is sourced from a “boot” capacitor connected across the BOOT and PHASE pins. The boot capacitor is charged from a 5V bias supply through a “boot diode” each time the low-side MOSFET turns on, pulling the PHASE pin low. The ISL6228 has an integrated boot diode connected from the PVCC pin to the BOOT pin.

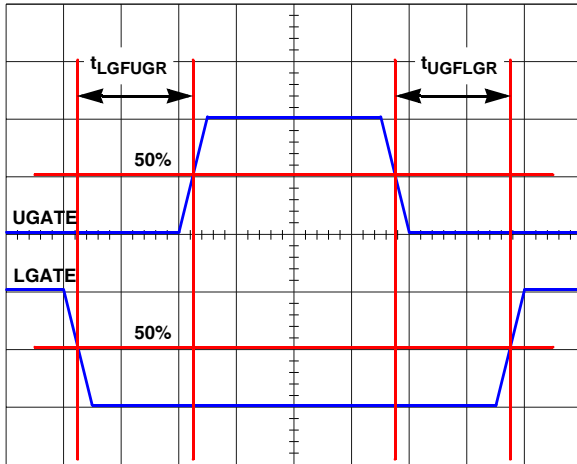


FIGURE 4. LGATE AND UGATE DEAD-TIME

**Diode Emulation**

The ISL6228 implements forced continuous-conduction-mode (CCM) at heavy load and diode-emulation-mode (DEM) at light load, to optimize efficiency in the entire load range. The transition is automatically achieved by detecting the output load current.

Positive-going inductor current flows from either the source of the high-side MOSFET, or the drain of the low-side MOSFET. Negative-going inductor current flows into the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the GND and PGND pins. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the GND and PGND pins. The ISL6228 monitors the phase voltage, when the low-side MOSFET is conducting inductor current, to determine the direction of the inductor current.

When the output load current is greater than or equal to ½ the inductor ripple current, the inductor current is always positive, and the converter is always in CCM. The ISL6228 minimizes the conduction loss in this condition by forcing the low-side MOSFET to operate as a synchronous rectifier.

When the output load current is less than ½ the inductor ripple current, negative inductor current occurs. Sinking negative inductor through the low-side MOSFET lowers efficiency through unnecessary conduction losses. The ISL6228 automatically enters DEM after the PHASE pin has

detected positive voltage and LGATE was allowed to go high for eight consecutive PWM switching cycles. The ISL6228 will turn off the low-side MOSFET once the phase voltage turns positive, indicating negative inductor current. The ISL6228 will return to CCM on the following cycle after the PHASE pin detects negative voltage, indicating that the body diode of the low-side MOSFET is conducting positive inductor current.

Efficiency can be further improved with a reduction of unnecessary switching losses by reducing the PWM frequency. It is characteristic of the R<sup>3</sup> architecture for the PWM frequency to decrease while in diode emulation. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency makes an initial step-reduction because of a 33% step-increase of the window voltage V<sub>W</sub>.

**Overcurrent Protection**

The overcurrent protection (OCP) setpoint is programmed with resistor R<sub>OCSET</sub> that is connected across the OCSET and PHASE pins.

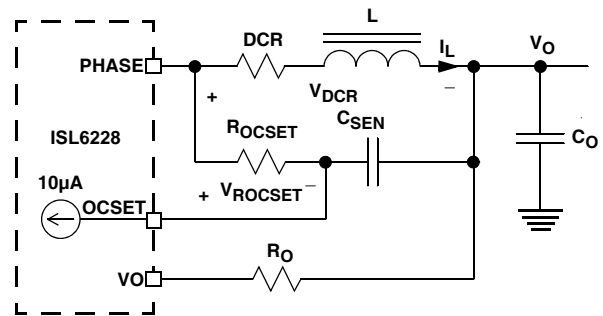


FIGURE 5. OVERCURRENT-SET CIRCUIT

Figure 5 shows the overcurrent-set circuit. The inductor consists of inductance L and the DC resistance DCR. The inductor DC current I<sub>L</sub> creates a voltage drop across DCR, given by Equation 3:

$$V_{DCR} = I_L \cdot DCR \tag{EQ. 3}$$

The ISL6228 sinks 10µA current into the OCSET pin, creating a DC voltage drop across the resistor R<sub>OCSET</sub>, given by Equation 4:

$$V_{ROCSET} = 10\mu A \cdot R_{OCSET} \tag{EQ. 4}$$

Resistor R<sub>O</sub> is connected between the VO pin and the actual output voltage of the converter. During normal operation, the VO pin is a high impedance path, therefore there is no voltage drop across R<sub>O</sub>. The DC voltage difference between the OCSET pin and the VO pin can be established using Equation 5:

$$V_{OCSET} - V_{VO} = V_{DCR} - V_{ROCSET} = I_L \cdot DCR - 10\mu A \cdot R_{OCSET} \tag{EQ. 5}$$

The ISL6228 monitors the OCSET pin and the VO pin voltages. Once the OCSET pin voltage is higher than the VO pin voltage for more than 10µs, the ISL6228 declares an OCP fault. The value of  $R_{OCSET}$  is then written as Equation 6:

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{10\mu A} \quad (\text{EQ. 6})$$

Where:

- $R_{OCSET}$  ( $\Omega$ ) is the resistor used to program the overcurrent setpoint
- $I_{OC}$  is the output current threshold that will activate the OCP circuit
- DCR is the inductor DC resistance

For example, if  $I_{OC}$  is 20A and DCR is 4.5m $\Omega$ , the choice of  $R_{OCSET}$  is  $R_{OCSET} = 20A \times 4.5m\Omega / 10\mu A = 9k\Omega$ .

Resistor  $R_{OCSET}$  and capacitor  $C_{SEN}$  form an R-C network to sense the inductor current. To sense the inductor current correctly not only in DC operation, but also during dynamic operation, the R-C network time constant  $R_{OCSET}C_{SEN}$  needs to match the inductor time constant  $L/DCR$ . The value of  $C_{SEN}$  is then written as Equation 7:

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR} \quad (\text{EQ. 7})$$

For example, if L is 1.5µH, DCR is 4.5m $\Omega$ , and  $R_{OCSET}$  is 9k $\Omega$ , the choice of  $C_{SEN} = 1.5\mu H / (9k\Omega \times 4.5m\Omega) = 0.037\mu F$ .

Upon converter startup, capacitor  $C_{SEN}$  initial voltage is 0V. To prevent false OCP, a 10µA current source flows out of the VO pin during start up, generating a voltage drop on resistor  $R_O$ , which has the same resistance as  $R_{OCSET}$ . When PGOOD pin goes high, the VO pin current source will terminate.

When an OCP fault is declared, the PGOOD pin will pull down to 30 $\Omega$  and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage  $V_{ENTHF}$  or if  $V_{CC}$  has decayed below the falling POR threshold voltage  $V_{VCC\_THF}$ .

### Overvoltage Protection

The OVP fault detection circuit triggers after the FB pin voltage is above the rising overvoltage threshold  $V_{OVR}$  for more than 2µs. The FB pin voltage is 0.6V in normal operation. The rising overvoltage threshold  $V_{OVR}$  is typically 116%. That means if the FB pin voltage is above 116%  $\times$  0.6V = 0.696V, for more than 2µs, an OVP fault is declared.

When an OVP fault is declared, the PGOOD pin will pull down to 60 $\Omega$  and latch-off the converter. The OVP fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage  $V_{ENTHF}$  or if  $V_{CC}$  has decayed below the falling POR threshold voltage  $V_{VCC\_THF}$ .

Although the converter has latched-off in response to an OVP fault, the LGATE gate-driver output will retain the ability to toggle the low-side MOSFET on and off, in response to

the output voltage transverse the  $V_{OVR}$  and  $V_{OVF}$  thresholds. The LGATE gate-driver will turn on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE gate-driver will turn off the low-side MOSFET once the FB pin voltage is lower than the falling overvoltage threshold  $V_{OVF}$  for more than 2µs. The falling overvoltage threshold  $V_{OVF}$  is typically 106%. That means if the FB pin voltage falls below 106%  $\times$  0.6V = 0.636V, for more than 2µs, the LGATE gate-driver will turn off the low-side MOSFET. If the output voltage rises again, the LGATE driver will again turn on the low-side MOSFET when the FB pin voltage is above the rising overvoltage threshold  $V_{OVR}$  for more than 2µs. By doing so, the ISL6228 protects the load when there is a consistent overvoltage condition.

### Undervoltage Protection

The UVP fault detection circuit triggers after the FB pin voltage is below the undervoltage threshold  $V_{UV}$  for more than 2µs. The FB pin voltage is 0.6V in normal operation. The undervoltage threshold  $V_{UV}$  is typically 86%. That means if the FB pin voltage is below 86%  $\times$  0.6V = 0.516V, for more than 2µs, an UVP fault is declared, and the PGOOD pin will pull down to 95 $\Omega$  and latch-off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage  $V_{ENTHF}$  or if  $V_{CC}$  has decayed below the falling POR threshold voltage  $V_{VCC\_THF}$ .

### Programming the Output Voltage

When the converter is in regulation there will be 0.6V from the FB pin to the GND pin. Connect a two-resistor voltage divider across the VO pin and the GND pin with the output node connected to the FB pin. Scale the voltage-divider network such that the FB pin is 0.6V with respect to the GND pin when the converter is regulating at the desired output voltage. The output voltage can be programmed from 0.6V to 5V.

Programming the output voltage is written as Equation 8:

$$V_{REF} = V_O \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad (\text{EQ. 8})$$

Where:

- $V_O$  is the desired output voltage of the converter
- The voltage to which the converter regulates the FB pin is the  $V_{REF}$
- $R_{TOP}$  is the voltage-programming resistor that connects from the FB pin to the converter output. In addition to setting the output voltage, this resistor is part of the loop compensation network
- $R_{BOTTOM}$  is the voltage-programming resistor that connects from the FB pin to the GND pin

Choose  $R_{TOP}$  value first, and calculate  $R_{BOTTOM}$  according to Equation 9:

$$R_{BOTTOM} = \frac{V_{REF} \cdot R_{TOP}}{V_O - V_{REF}} \quad (\text{EQ. 9})$$

### Programming the PWM Switching Frequency

The ISL6228 does not use a clock signal to produce PWMs. The PWM switching frequency  $f_{SW}$  is programmed by the resistor  $R_{FSET}$  that is connected from the FSET pin to the GND pin. The approximate PWM switching frequency is written as Equation 10:

$$f_{SW} = \frac{1}{K \cdot R_{FSET}} \quad (\text{EQ. 10})$$

Estimating the value of  $R_{FSET}$  is written as Equation 11:

$$R_{FSET} = \frac{1}{K \cdot f_{SW}} \quad (\text{EQ. 11})$$

Where:

- $f_{SW}$  is the PWM switching frequency
- $R_{FSET}$  is the  $f_{SW}$  programming resistor
- $K = 1.5 \times 10^{-10}$

It is recommended that whenever the control loop compensation network is modified,  $f_{SW}$  should be checked for the correct frequency and if necessary, adjust  $R_{FSET}$ .

### Compensation Design

Figure 6 shows the recommended Type-II compensation circuit. The FB pin is the inverting input of the error amplifier. The COMP signal, the output of the error amplifier, is inside the chip and unavailable to users.  $C_{INT}$  is a 100pF capacitor integrated inside the IC, connecting across the FB pin and the COMP signal.  $R_{TOP}$ ,  $R_{FB}$ ,  $C_{FB}$  and  $C_{INT}$  form the Type-II compensator. The frequency domain transfer function is given by Equation 12:

$$G_{COMP}(s) = \frac{1 + s \cdot (R_{TOP} + R_{FB}) \cdot C_{FB}}{s \cdot R_{TOP} \cdot C_{INT} \cdot (1 + s \cdot R_{FB} \cdot C_{FB})} \quad (\text{EQ. 12})$$

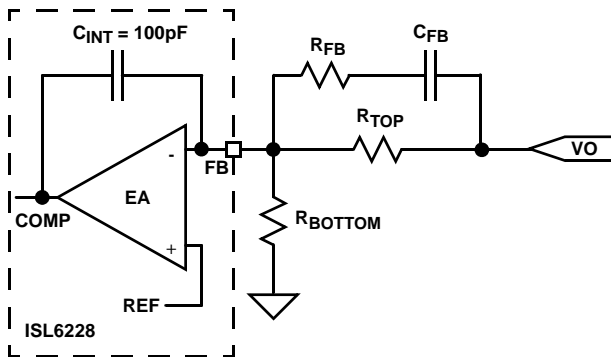


FIGURE 6. COMPENSATION REFERENCE CIRCUIT

The LC output filter has a double pole at its resonant frequency that causes rapid phase change. The  $R^3$  modulator used in the ISL6228 makes the LC output filter resemble a first order system in which the closed loop stability can be achieved with the recommended Type-II compensation network. Intersil provides a PC-based tool (example page is shown later) that can be used to calculate compensation network component values and help simulate the loop frequency response.

### General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

#### Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is written as Equation 13:

$$D = \frac{V_O}{V_{IN}} \quad (\text{EQ. 13})$$

The output inductor peak-to-peak ripple current is written as Equation 14:

$$I_{PP} = \frac{V_O \cdot (1 - D)}{f_{SW} \cdot L} \quad (\text{EQ. 14})$$

A typical step-down DC/DC converter will have an  $I_{P-P}$  of 20% to 40% of the maximum DC output load current. The value of  $I_{PP}$  is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated by Equation 15:

$$P_{COPPER} = I_{LOAD}^2 \cdot DCR \quad (\text{EQ. 15})$$

Where  $I_{LOAD}$  is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance  $C_O$  into which ripple current  $I_{P-P}$  can flow. Current  $I_{PP}$  develops a corresponding ripple voltage  $V_{P-P}$  across  $C_O$ , which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written as Equation 16:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad (\text{EQ. 16})$$

and Equation 17:

$$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}} \quad (\text{EQ. 17})$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required  $V_{P-P}$  is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered. A capacitor

dissipates heat as a function of RMS current and frequency. Be sure that  $I_{p-p}$  is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at  $f_{SW}$ . Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

### Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 7 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as Equation 18:

$$I_{IN\_RMS,NORMALIZED} = \frac{\sqrt{(I_{MAX}^2 \cdot (D - D^2)) + (x \cdot I_{MAX}^2 \cdot \frac{D}{12})}}{I_{MAX}} \quad (\text{EQ. 18})$$

Where:

- $I_{MAX}$  is the maximum continuous  $I_{LOAD}$  of the converter
- $x$  is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of  $I_{MAX}$  (0% to 100%)
- $D$  is the duty cycle that is adjusted to take into account the efficiency of the converter which is written as:

$$D = \frac{V_O}{V_{IN} \cdot \text{EFF}} \quad (\text{EQ. 19})$$

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

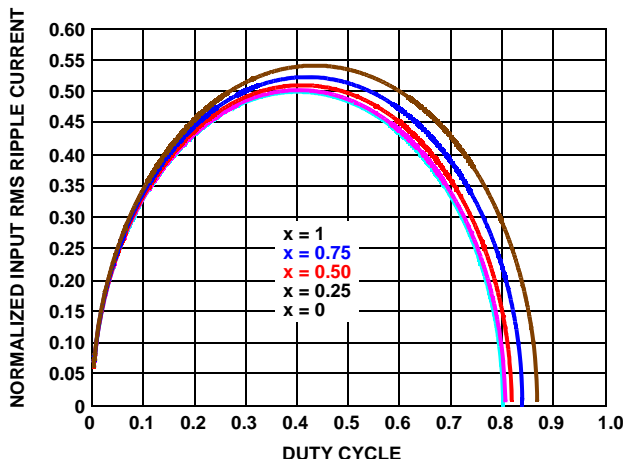


FIGURE 7. NORMALIZED RMS INPUT CURRENT

### MOSFET Selection and Considerations

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum  $V_{DS}$  rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with  $V_{IN} - V_{OUT}$ , plus the spike, across it. The preferred low-side MOSFET emphasizes low  $r_{DS(ON)}$  when fully saturated to minimize conduction loss.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 20:

$$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)\_LS} \cdot (1 - D) \quad (\text{EQ. 20})$$

For the high-side (HS) MOSFET, the its conduction loss is written as Equation 21:

$$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(ON)\_HS} \cdot D \quad (\text{EQ. 21})$$

For the high-side MOSFET, the switching loss is written as Equation 22:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2} \quad (\text{EQ. 22})$$

Where:

- $I_{VALLEY}$  is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- $I_{PEAK}$  is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{ON}$  is the time required to drive the device into saturation
- $t_{OFF}$  is the time required to drive the device into cut-off

### Selecting The Bootstrap Capacitor

The selection of the bootstrap capacitor is written as Equation 23:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad (\text{EQ. 23})$$

Where:

- $Q_g$  is the total gate charge required to turn on the high-side MOSFET
- $\Delta V_{BOOT}$ , is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate charge  $Q_g$ , of 25nC at  $V_{GS} = 5V$ , and a  $\Delta V_{BOOT}$  of 200mV. The calculated bootstrap capacitance is 0.125 $\mu$ F; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22 $\mu$ F will suffice. Use an X7R or X5R ceramic capacitor.

### Layout Considerations

As a general rule, power should be on the bottom layer of the PCB and weak analog or logic signals are on the top layer of the PCB. The ground-plane layer should be adjacent to the top layer to provide shielding. The ground plane layer should have an island located under the IC, the compensation components, and the FSET components. The island should be connected to the rest of the ground plane layer at one point.

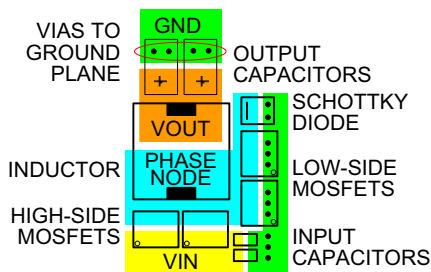


FIGURE 8. TYPICAL POWER COMPONENT PLACEMENT

### Signal Ground and Power Ground

The bottom of the ISL6228 TQFN package is the signal ground (GND) terminal for analog and logic signals of the IC. Connect the GND pad of the ISL6228 to the island of ground plane under the top layer using several vias, for a robust thermal and electrical conduction path. Connect the input capacitors, the output capacitors, and the source of the lower MOSFETs to the power ground plane.

### PGND (Pins 17 and 18)

This is the return path for the pull-down of the LGATE low-side MOSFET gate driver. Ideally, PGND should be connected to the source of the low-side MOSFET with a low-resistance, low-inductance path.

### VIN (Pins 2 and 5)

The VIN pin should be connected close to the drain of the high-side MOSFET, using a low resistance and low inductance path.

### VCC (Pins 3 and 4)

For best performance, place the decoupling capacitor very close to the VCC and GND pins.

### PVCC (Pins 15 and 20)

For best performance, place the decoupling capacitor very close to the PVCC and respective PGND pins, preferably on the same side of the PCB as the ISL6228 IC.

### EN (Pins 11 and 24), and PGOOD (Pins 7 and 28)

These are logic signals that are referenced to the GND pin. Treat as a typical logic signal.

### OCSET (Pins 10 and 25)

The current-sensing network consisting of  $R_{OCSET}$  and  $C_{SEN}$  needs to be connected to the inductor pads for accurate measurement. Connect  $R_{OCSET}$  to the phase-node side pad of the inductor, and connect  $C_{SEN}$  to the output side pad of the inductor. Connect the OCSET pin to the common node of node of  $R_{OCSET}$  and  $C_{SEN}$ .

### FB (Pins 8 and 27), and VO (Pins 9 and 26)

The VO pin is used to sense the inductor current for OCP. Connect the VO pin to the output-side of  $C_{SEN}$  through resistor  $R_O$ . The input impedance of the FB pin is high, so place the voltage programming and loop compensation components close to the VO, FB, and GND pins keeping the high impedance trace short.

### FSET (Pins 1 and 6)

This pin requires a quiet environment. The resistor  $R_{FSET}$  and capacitor  $C_{FSET}$  should be placed directly adjacent to this pin. Keep fast moving nodes away from this pin.

### LGATE (Pins 16 and 19)

The signal going through this trace is both high  $dv/dt$  and high  $di/dt$ , with high peak charging and discharging current. Route this trace in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in proximity with these traces on any layer.

### BOOT (Pins 14 and 21), UGATE (Pins 13 and 22), and PHASE (Pins 12 and 23)

The signals going through these traces are both high  $dv/dt$  and high  $di/dt$ , with high peak charging and discharging current. Route the UGATE and PHASE pins in parallel with short and wide traces. There should be no other weak signal traces in proximity with these traces on any layer.

### Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the upper MOSFET and the source of the lower MOSFET to suppress the turn-off voltage spike.

Typical Performance

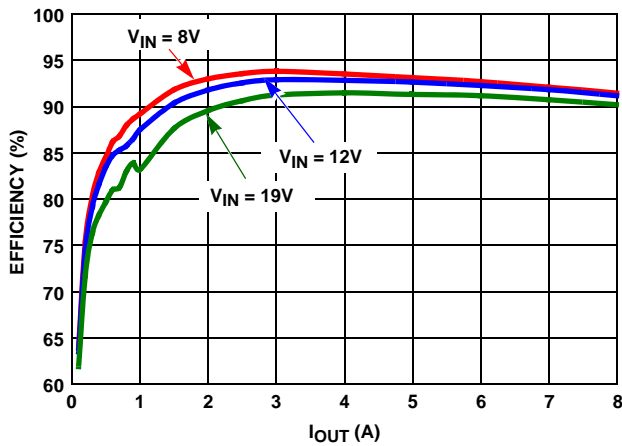


FIGURE 9. CHANNEL 1 EFFICIENCY AT  $V_O = 1.5V$

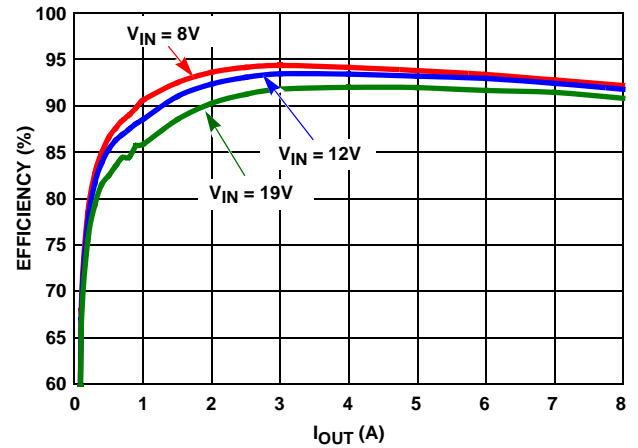


FIGURE 10. CHANNEL 2 EFFICIENCY AT  $V_O = 1.8V$

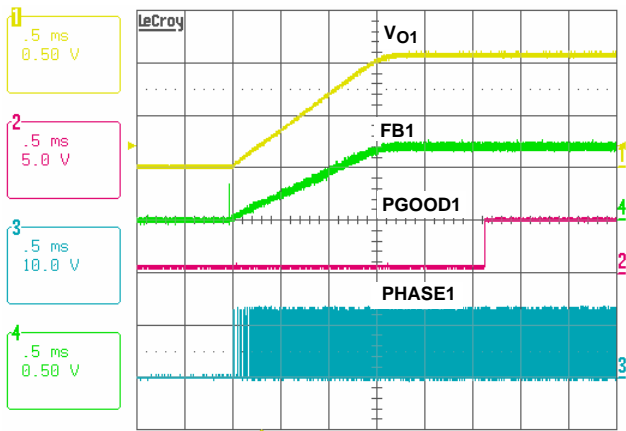


FIGURE 11. START-UP,  $V_{IN} = 12V$ ,  $I_{LOAD} = 0.25A$ ,  $V_O = 1.05V$

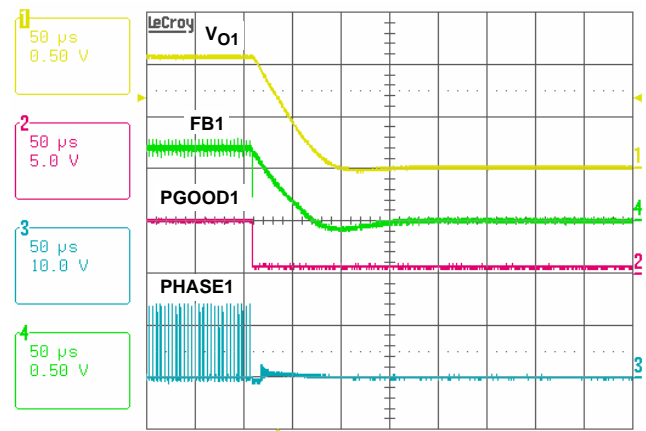


FIGURE 12. SHUT-DOWN,  $V_{IN} = 12V$ ,  $I_O = 10A$ ,  $V_O = 1.05V$

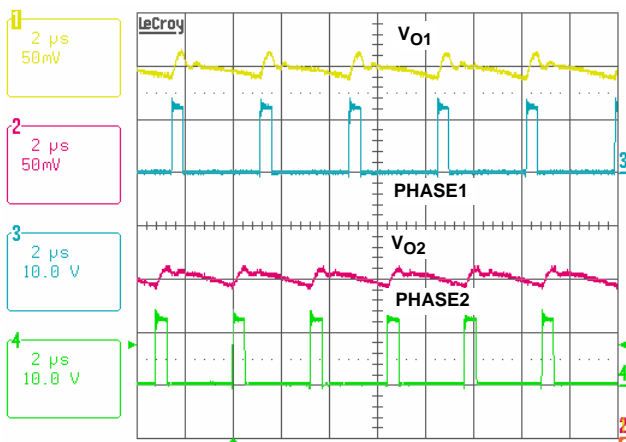


FIGURE 13. CCM STEADY-STATE OPERATION,  $V_{IN} = 12V$ ,  $V_{O1} = 1.5V$ ,  $I_{O1} = 3A$ ,  $V_{O2} = 1.8A$ ,  $I_{O2} = 4A$

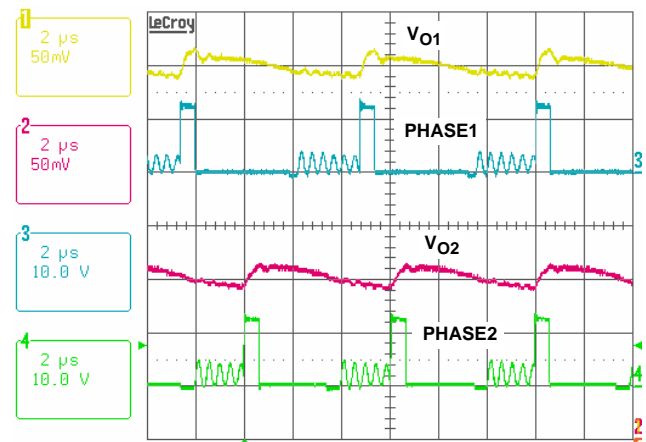


FIGURE 14. DCM STEADY-STATE OPERATION,  $V_{IN} = 12V$ ,  $V_{O1} = 1.5V$ ,  $I_{O1} = 1A$ ,  $V_{O2} = 1.8V$ ,  $I_{O2} = 1A$

Typical Performance (Continued)

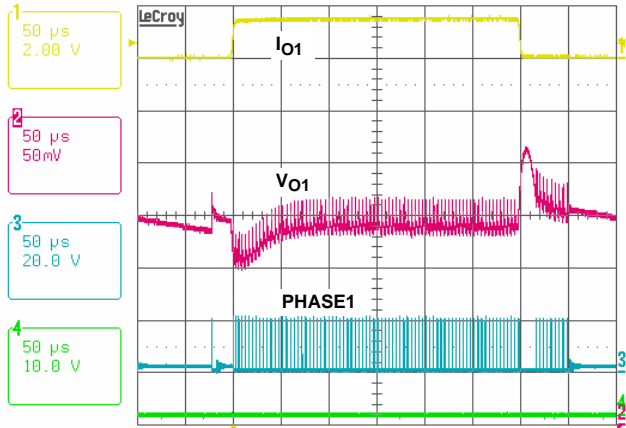


FIGURE 15. TRANSIENT RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.5V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

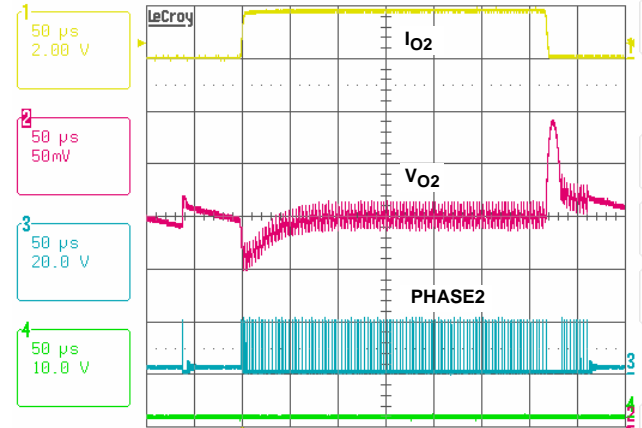


FIGURE 16. TRANSIENT RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.8V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

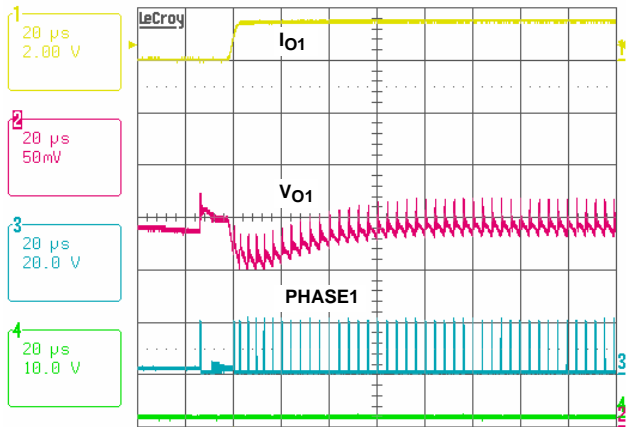


FIGURE 17. LOAD INSERTION RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.5V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

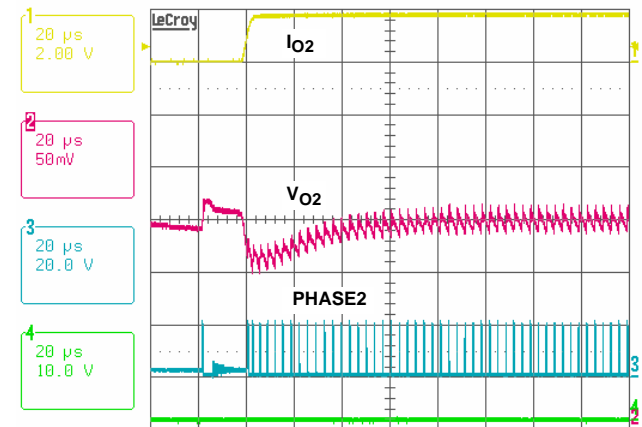


FIGURE 18. LOAD INSERTION RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.8V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

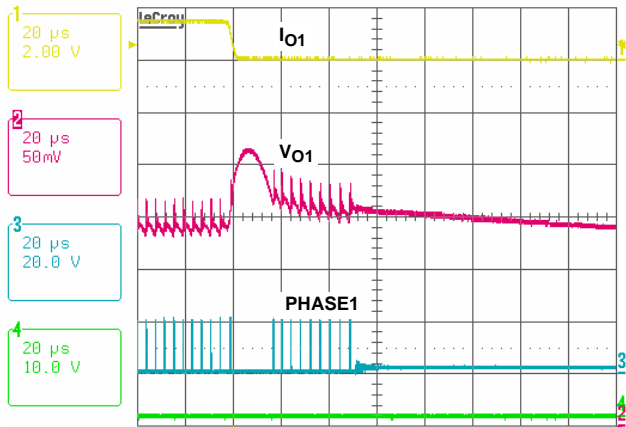


FIGURE 19. LOAD RELEASE RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.5V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

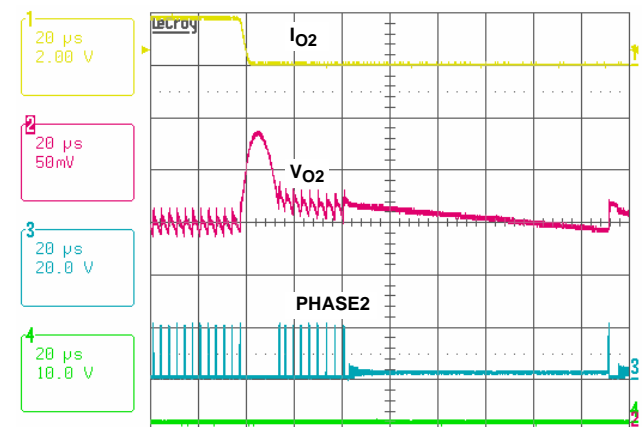


FIGURE 20. LOAD RELEASE RESPONSE,  $V_{IN} = 12V$ ,  $V_O = 1.8V$ ,  $I_O = 0.1A/8.1A @ 2.55A/\mu s$

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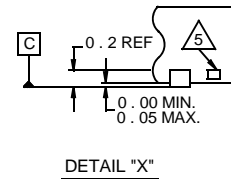
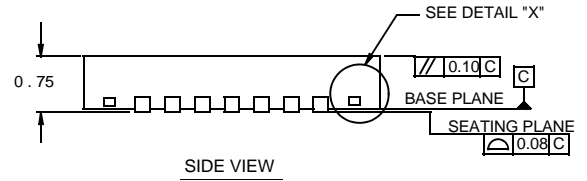
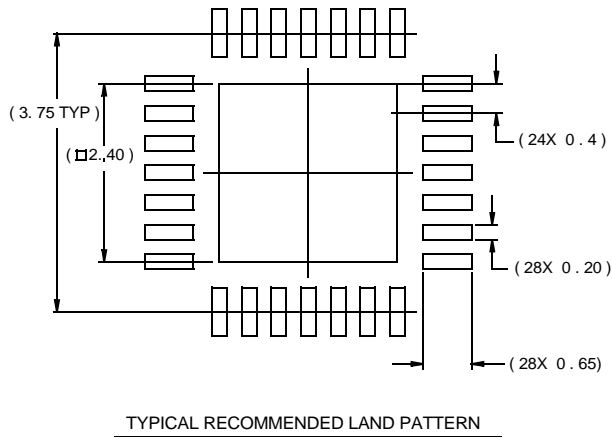
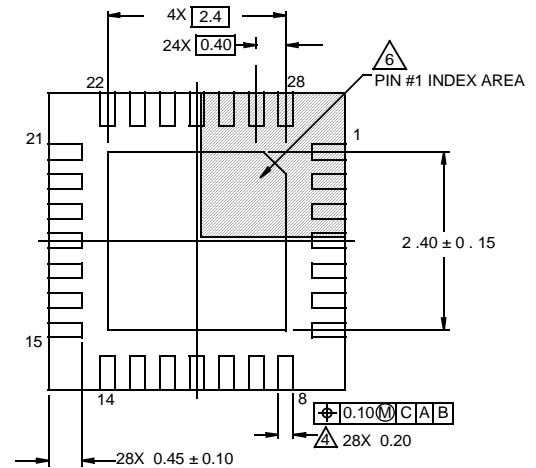
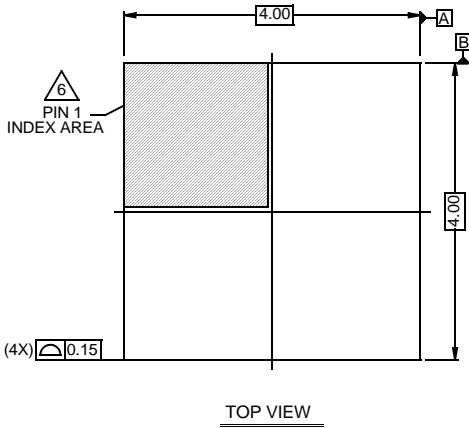
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## Package Outline Drawing

### L28.4x4A

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 3/07



#### NOTES:

- Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
- Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
- Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.