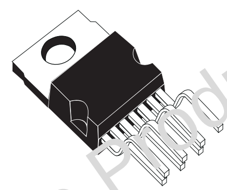
L4901A

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS : I_{01} = 400mA
  $I_{0\,2}$ = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1µA AT OUTPUT 1
- LOW QUIESCENT CURRENT (Input 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SO A PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION



HEPTAWATT (Vertical)
(Plastic Package)

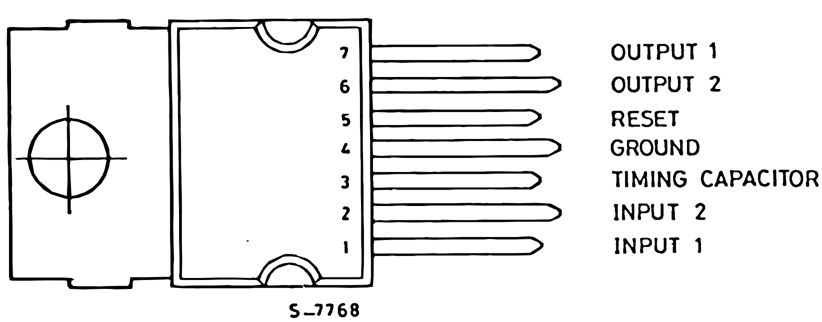
ORDERING NUMBER : L4901A

DESCRIPTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

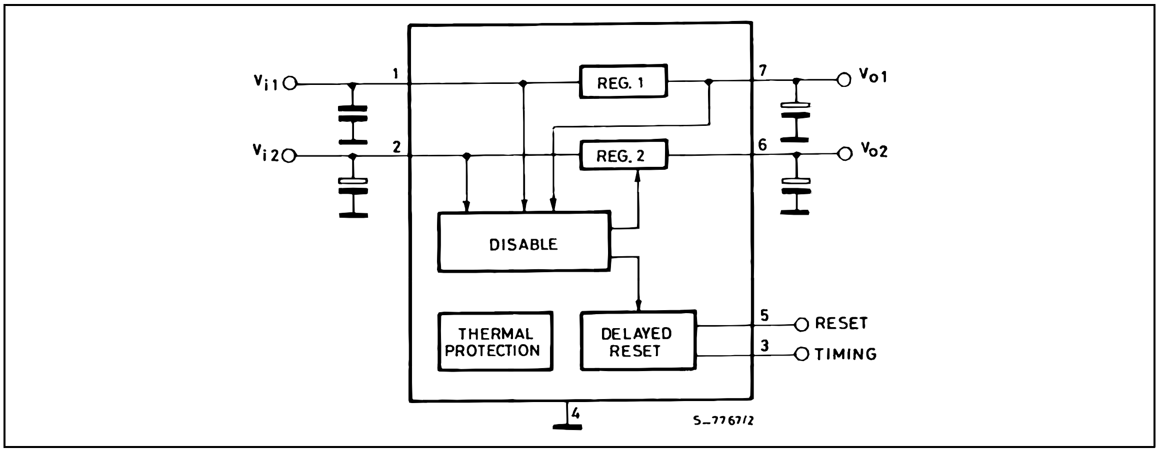
PIN CONNECTION



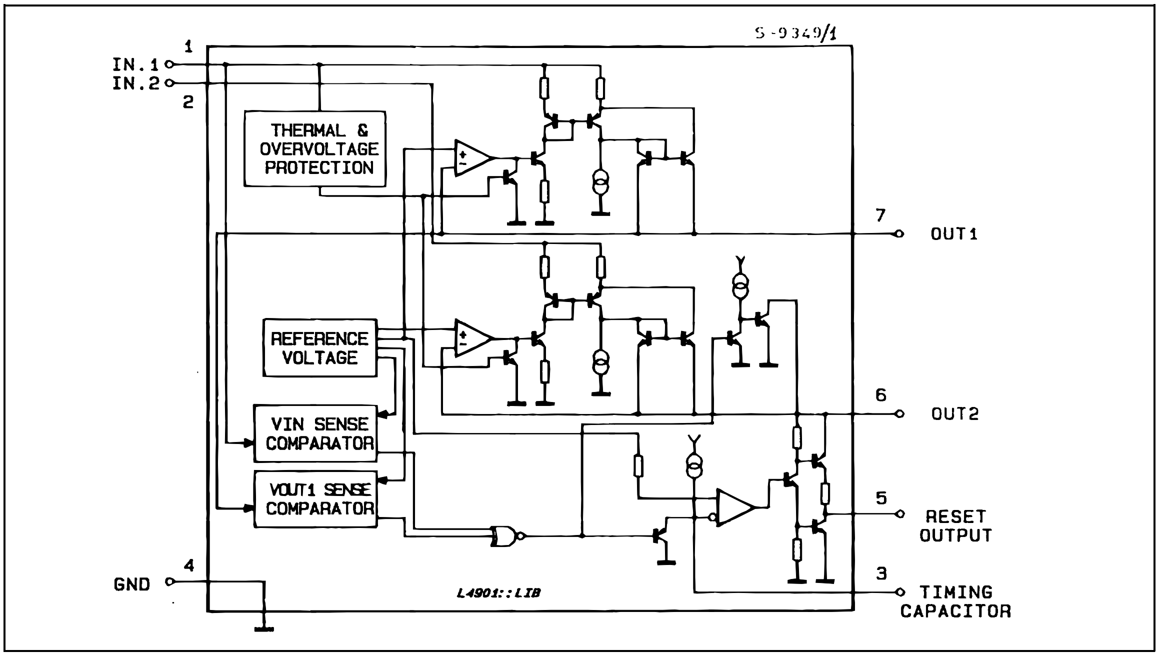
PIN DESCRIPTION

N°	Name	Function
1	Input 1	Low Quiescent Current 400mA Regulator Input.
2	Input 2	400mA regulator input.
3	Timing Capacitor	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is decharged.
4	GND	Common Ground.
5	Reset Output	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t\,(\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF)
6	Output 2	5V – 400mA Regulator Output. Enabled if V_o 1 > V_{RT} and $V_{IN\,2}$ > V_{IT}. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	Output 1	5V – 400mA regulator output with Low leakage (in switch-OFF condition).

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Transient Input Overvoltage (t = 40ms)	24 60	V V
I_o	Output Current	Internally Limited	
T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

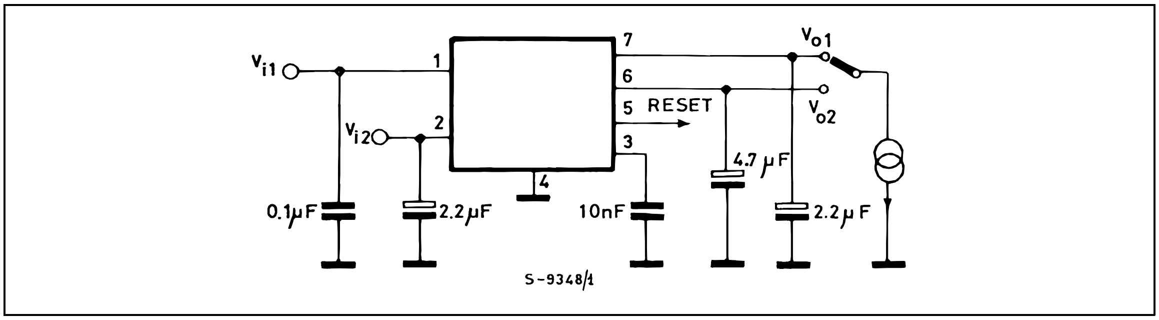
Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}c)}$	Thermal Resistance Junction-case Max.	4	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 14, 4V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC Operating Input Voltage				20	V
V_{01}	Output Voltage 1	R Load 1kΩ	4.95	5.05	5.15	V
$V_{02\ H}$	Output Voltage 2 HIGH	R Load 1kΩ	V_{01} –0.1	5	V_{01}	V
$V_{02\ L}$	Output Voltage 2 LOW	I_{02} = – 5mA		0.1		V
I_{01}	Output Current 1	ΔV_{01} = – 100mV	400			mA
I_{L01}	Leakage Output 1 Current	V_{IN} = 0, $V_{01} \leq$ 3V			1	µA
I_{02}	Output Current 2	ΔV_{02} = – 100mV	400			mA
V_{I01}	Output 1 Dropout Voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input Threshold Voltage		V_{01} + 1.2	6.4	V_{01} + 1.7	V
V_{ITH}	Input Threshold Voltage Hyst.			250		mV
ΔV_{01}	Line Regulation 1	7V < V_{IN} < 18V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line Regulation 2	7V < V_{IN} < 18V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load Regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load Regulation 2	5mA < I_{01} < 400mA		50	100	mV
I_Q	Quiescent Current	I_{02} = $I_{01} \leq$ 5mA 0 < V_{IN} < 13V 7V < V_{IN} < 13V		4.5 1.6	6.5 3.5	mA
I_{Q1}	Quiescent Current 1	$I_{01} \leq$ 5mA, I_{02} = 0, V_{IN2} = 0 6.3V < V_{IN} < 13V		0.6	0.9	mA
V_{RT}	Reset Threshold Voltage		V_{02} – 0.15	4.9	V_{02} –0.05	V
V_{RTH}	Reset Threshold Hysteresis		30	50	80	mV
V_{RH}	Reset Output Voltage HIGH	I_R = 500µA	V_{02} – 1	4.12	V_{02}	V
V_{RL}	Reset Output Voltage LOW	I_R = –<0>5mA		0.25	0.4	V
t_{RD}	Reset Pulse Delay	C_t = 10nF	3	5	11	ms
t_d	Timing Capacitor Discharge Time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
SVR1	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V Io = 100mA	50	84		dB
SVR2	Supply Voltage Rejection		50	80		dB

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

TEST CIRCUIT



APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments ; it provides two voltage regulators (both 5 V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Figure 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs :
- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$) ;
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$) ;

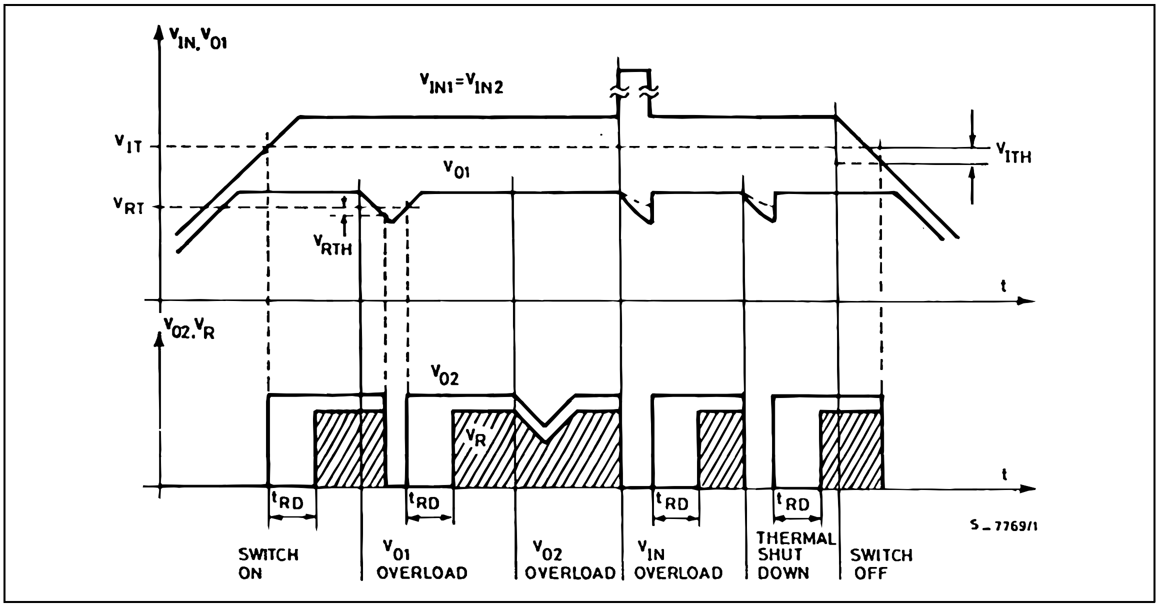
and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features :
- 5 V internal reference without voltage divider between the output and the error comparator ;
- very low drop series regulator element utilizing current mirrors ;

permit high output impedance and then very low leakage current error even in power down condi-

Figure 1



tion.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6 mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

APPLICATIONS SUGGESTIONS

Figure 2 shows an application circuit for a µP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is

Figure 2

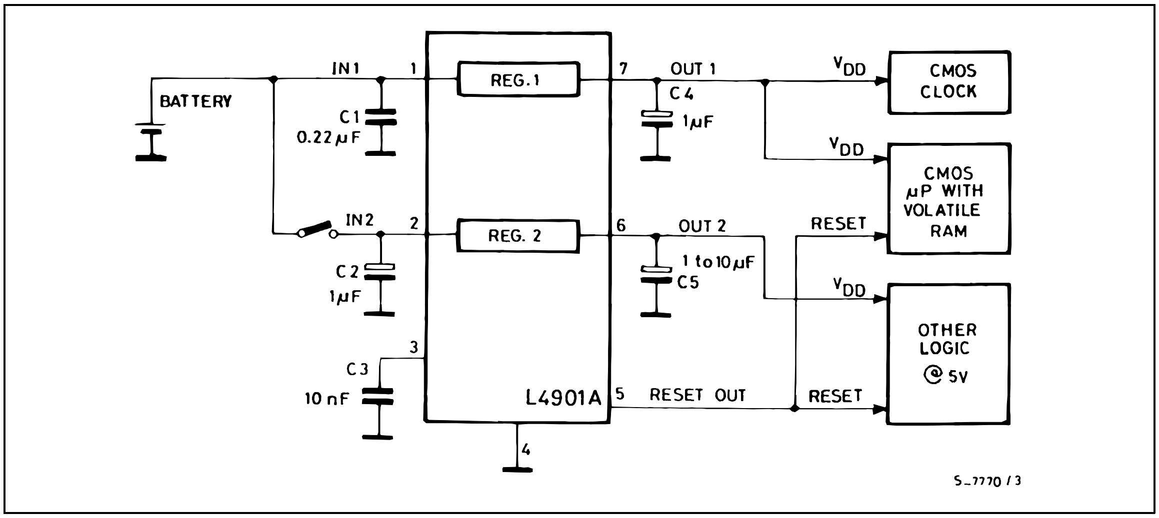
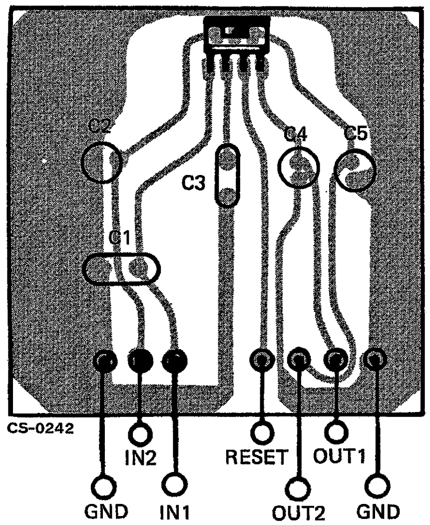


Figure 3 : P.C. Board Component Layout of Figure 2.



inactive.

Figure 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in Figure 5 the reset output is used both to

Figure 4

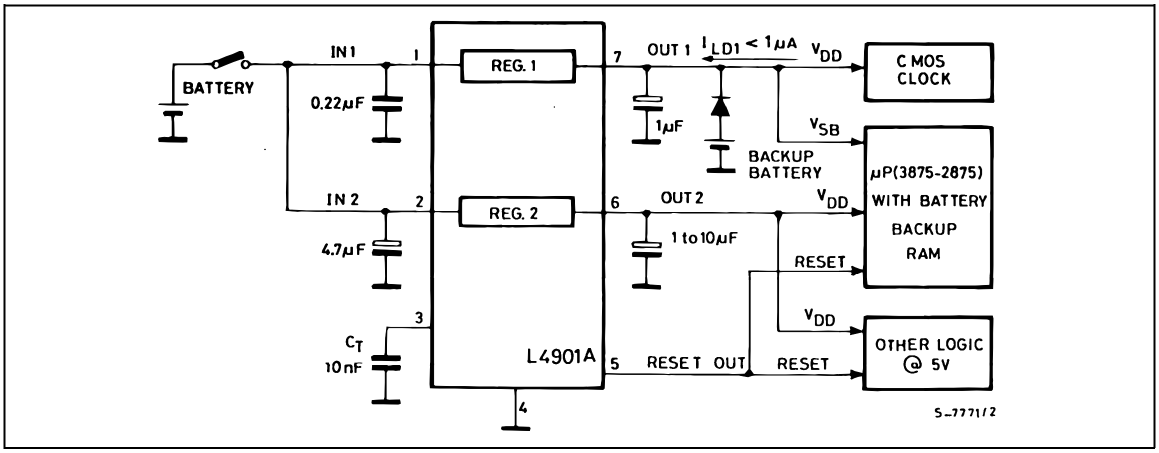
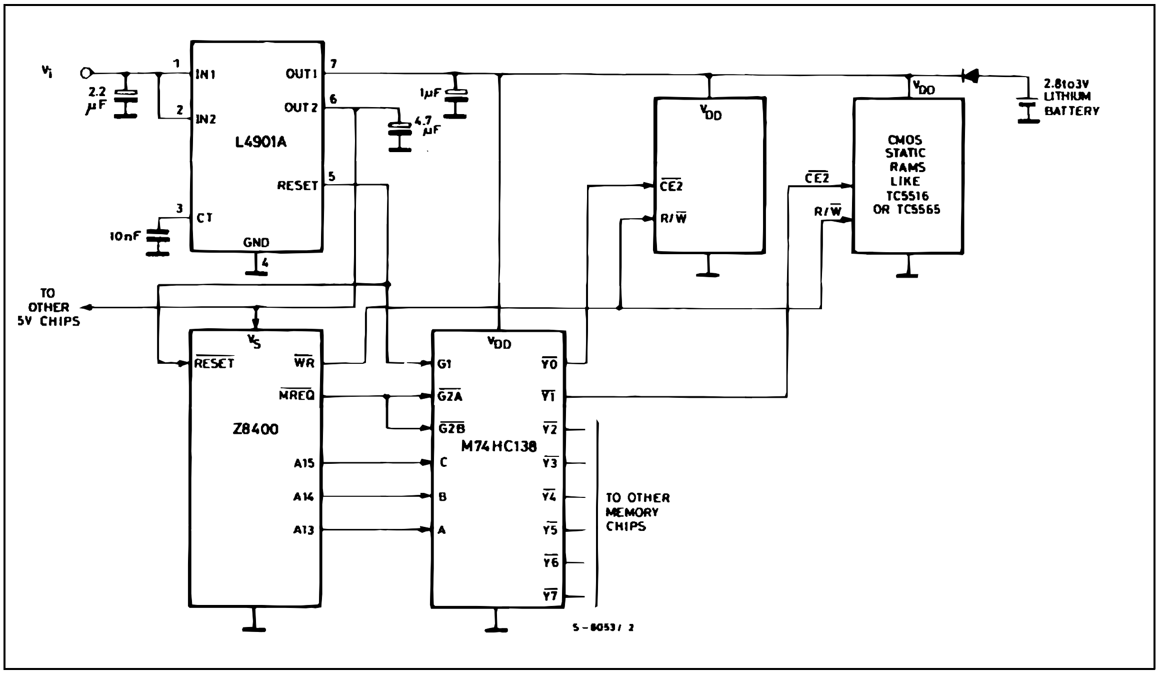


Figure 5



disable the µP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in µP system with shadow memories (see Figure 6).

When the input voltage goes below V_{IT}, the reset ouput enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a

Figure 6

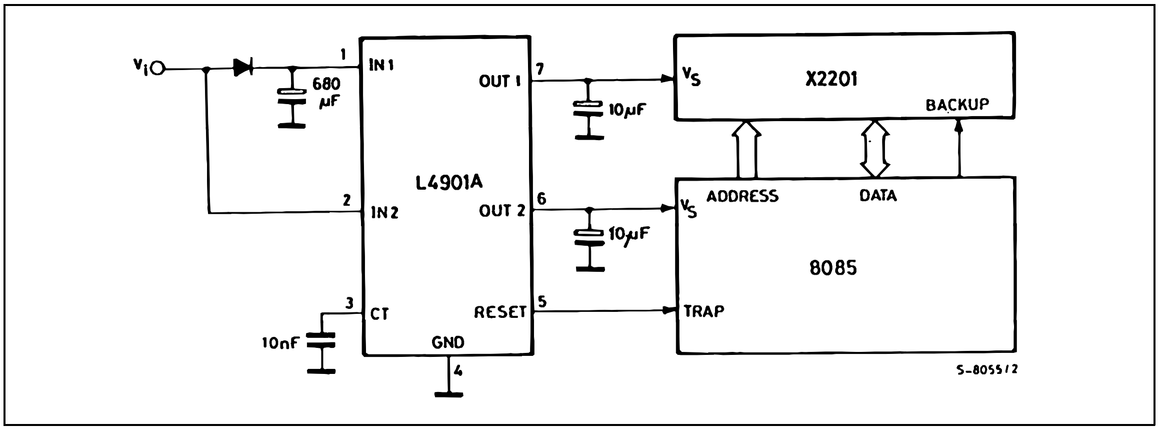


Figure 7 : Quiescent Current (reg.1) versus Output Current

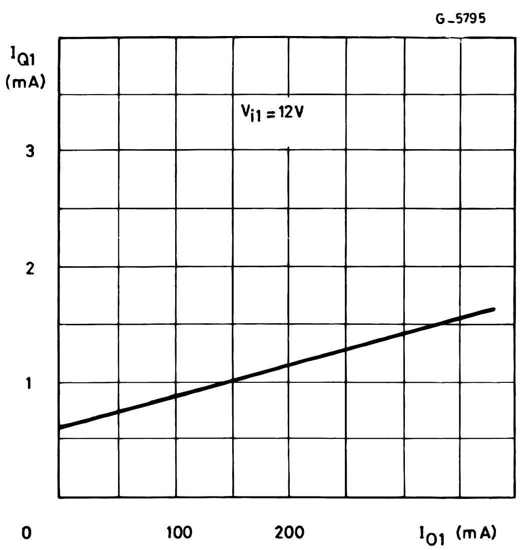


Figure 8 : Quiescent Current (reg.1) versus Input Voltage

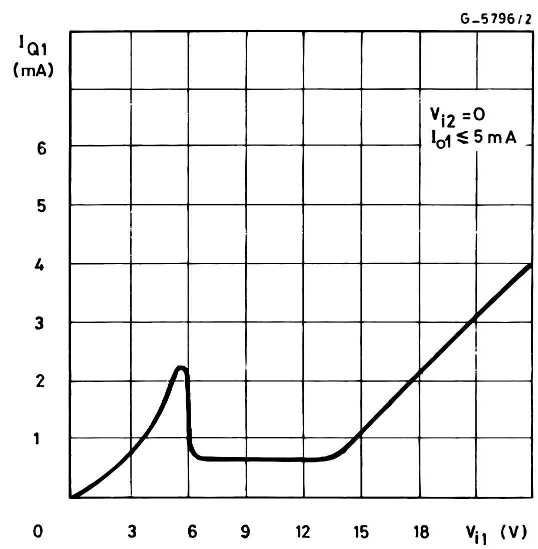


Figure 9 : Total Quiescent Current versus Input Voltage

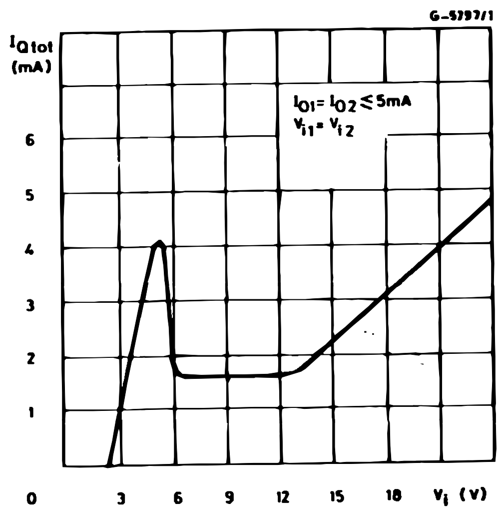


Figure 10 : Regulator 1 Output Current and Short Circuit Current versus Input Voltage

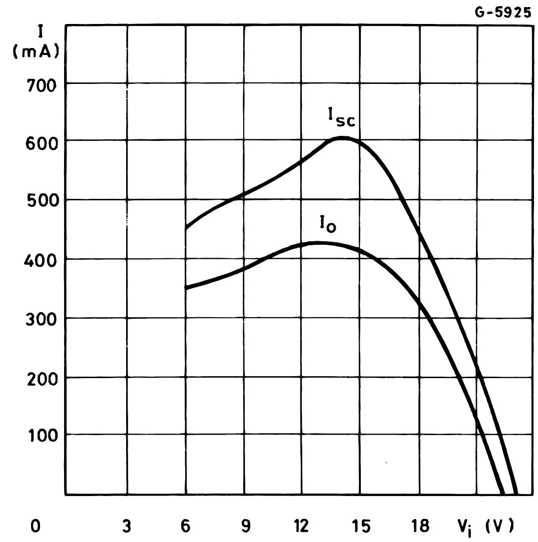


Figure 11 : Regulator 1 Output Current and Short Circuit Current versus Input Voltage

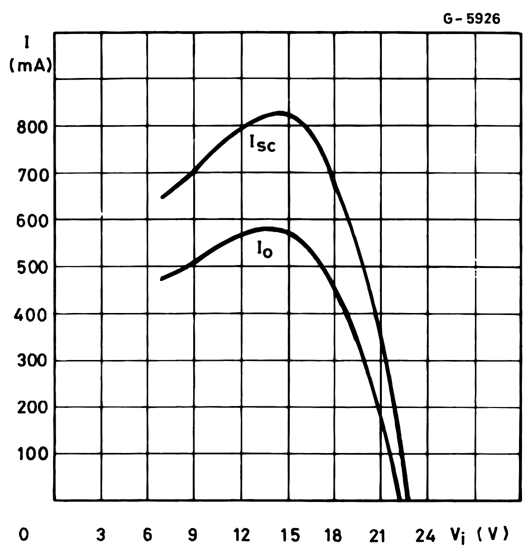
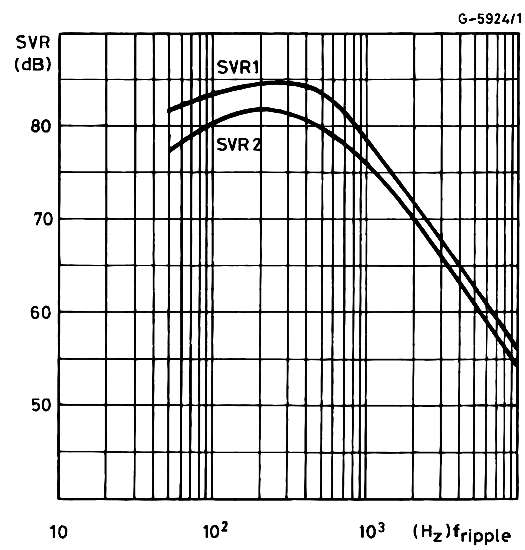
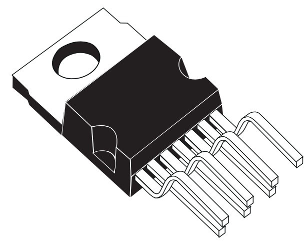


Figure 12 : Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequence



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.7		0.97	0.028		0.038
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.34	2.54	2.74	0.095	0.100	0.105
G1	4.88	5.08	5.28	0.193	0.200	0.205
G2	7.42	7.62	7.82	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L	16.7	16.9	17.1	0.657	0.668	0.673
L1		14.92			0.587	
L2	21.24	21.54	21.84	0.386	0.848	0.860
L3	22.27	22.52	22.77	0.877	0.891	0.896
L4			1.29			0.051
L5	2.6	2.8	3	0.102	0.110	0.118
L6	15.1	15.5	15.8	0.594	0.610	0.622
L7	6	6.35	6.6	0.236	0.250	0.260
L9		0.2			0.008	
M	2.55	2.8	3.05	0.100	0.110	0.120
M1	4.83	5.08	5.33	0.190	0.200	0.210
V4	40° (typ.)					
Dia	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Heptawatt V