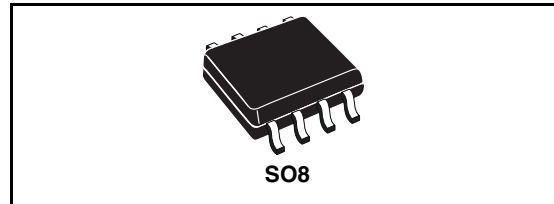


Up to 1A step down switching regulator

Features

- Up to 1A output current
- Operating input voltage from 4.4V to 36V
- 3.3V / ($\pm 2\%$) reference voltage
- Output voltage adjustable from 1.2V to 35V
- Low dropout operation: 100% duty cycle
- 250KHz Internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown



Description

The L5970D is a step down monolithic power switching regulator capable to deliver up to 1A at output voltages from 1.2V to 35V.

The device uses an internal P-Channel D-MOS transistor (with a typical R_{dson} of 250m Ω) as switching element to minimize the size of the external components.

An internal oscillator fixes the switching frequency at 250KHz.

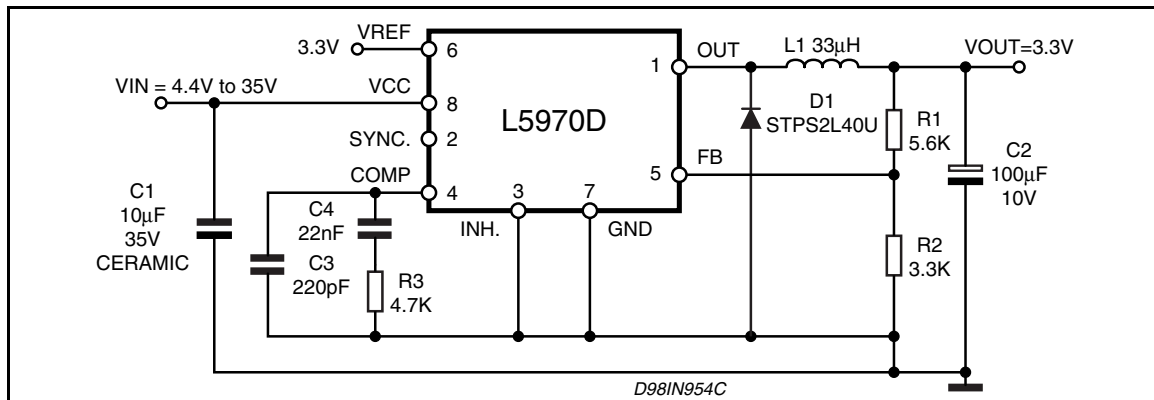
Having a minimum input voltage of 4.4V only, it is particularly suitable for 5V bus, available in all computer related applications.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

Applications

- Consumer: STB, DVD, TV, VCR, car radio, LCD monitors
- Networking: XDSL, modems, DC-DC modules
- Computer: printers, audio/graphic cards, optical storage, hard disk drive
- Industrial: changers, car battery, DC-DC converters

Figure 1. Test application circuit



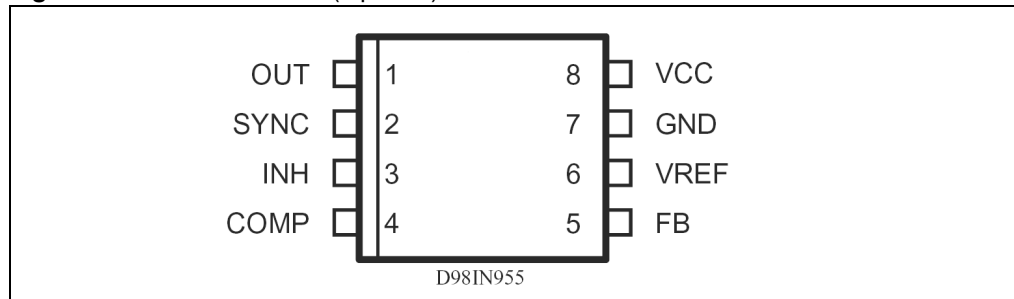
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1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Type	Description
1	OUT	Regulator output.
2	SYNC	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disable the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
6	VREF	3.3V V_{REF} No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V ₈	Input voltage	40	V
V ₁	Output DC voltage Output peak voltage at t = 0.1μs	-1 to 40 -5 to 40	V V
I ₁	Maximum output current	int. limit.	
V ₄ , V ₅	Analog pins	4	V
V ₃	INH	-0.3V to V _{CC}	
V ₂	SYNC	-0.3 to 4	V
P _{TOT}	Power dissipation at T _A ≤ 60°C	0.75	W
T _J	Operating junction temperature range	-40 to 150	°C
T _{STG}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO8	Unit
R _{thJA}	Maximum thermal resistance junction-ambient	120 ⁽¹⁾	°C/W

1. Package mounted on board

3 Electrical characteristics

Table 4. Electrical characteristics

 ($T_J = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
V_{CC}	Operating input voltage range	$V_o = 1.235\text{V}$; $I_o = 2\text{A}$	(1)	4.4		36	V
$R_{DS(on)}$	Mosfet on Resistance		(1)		0.250	0.5	Ω
I_l	Maximum limiting current	$V_{CC} = 4.4\text{V}$ to 36V		1.5	1.87	2.25	A
f_s	Switching frequency		(1)	212	250	280	KHz
				225	250	275	KHz
	Duty cycle			0		100	%
Dynamic characteristics (see test circuit).							
V_5	Voltage feedback	$4.4\text{V} < V_{CC} < 36\text{V}$, $20\text{mA} < I_o < 2\text{A}$		1.220	1.235	1.25	V
			(1)	1.198	1.235	1.272	V
h	Efficiency	$V_o = 5\text{V}$, $V_{CC} = 12\text{V}$			90		%
DC characteristics							
I_{qop}	Total operating quiescent current		(1)		3	5	mA
I_q	Quiescent current	Duty cycle = 0; $V_{FB} = 1.5\text{V}$				2.5	mA
I_{qst-by}	Total stand-by quiescent current	$V_{inh} > 2.2\text{V}$	(1)		50	100	μA
		$V_{CC} = 36\text{V}$; $V_{inh} > 2.2\text{V}$	(1)		80	150	μA
Inhibit							
	INH threshold voltage	Device ON				0.8	V
		Device OFF		2.2			V
Error amplifier							
V_{OH}	High level output voltage	$V_{FB} = 1\text{V}$		3.5			V
V_{OL}	Low level output voltage	$V_{FB} = 1.5\text{V}$				0.4	V
I_o source	Source output current	$V_{COMP} = 1.9\text{V}$; $V_{FB} = 1\text{V}$		200	300		μA

Table 4. Electrical characteristics (continued)
 ($T_J = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	
$I_{o\text{ sink}}$	Sink output current	$V_{\text{COMP}} = 1.9\text{V};$ $V_{\text{FB}} = 1.5\text{V}$	1	1.5		mA	
I_b	Source bias current			2.5	4	μA	
	DC open loop gain	$R_L = \infty$	50	65		dB	
gm	Transconductance	$I_{\text{comp}} = -0.1\text{mA}$ to 0.1mA $V_{\text{COMP}} = 1.9\text{V}$		2.3		mS	
Sync function							
	High input voltage	$V_{CC} = 4.4\text{V}$ to 36V	2.5		V_{REF}	V	
	Low input voltage	$V_{CC} = 4.4\text{V}$ to 36V			0.74	V	
	Slave sink current	$V_{\text{sync}} = 0.74\text{V}$ ⁽²⁾ $V_{\text{sync}} = 2.33\text{V}$	0.11 0.21		0.25 0.45	mA mA	
	Master output amplitude	$I_{\text{source}} = 3\text{mA}$	2.75	3		V	
	Output pulse width	no load, $V_{\text{sync}} = 1.65\text{V}$	0.20	0.35		μs	
Reference section							
	Reference voltage		3.234	3.3	3.366	V	
		$I_{\text{REF}} = 0$ to 5mA $V_{CC} = 4.4\text{V}$ to 36V	(1)	3.2	3.3	3.399	V
	Line regulation	$I_{\text{REF}} = 0\text{mA}$ $V_{CC} = 4.4\text{V}$ to 36V		5	10	mV	
	Load regulation	$I_{\text{REF}} = 0$ to 5mA		8	15	mV	
	Short circuit current		10	18	30	mA	

1. Specification Referred to T_J from -40 to 125°C . Specification over the -40 to $+125$ T_J Temperature range are assured by design, characterization and statistical correlation.

2. Guaranteed by design.

4 Typical characteristics

Figure 3. Junction temperature vs output current

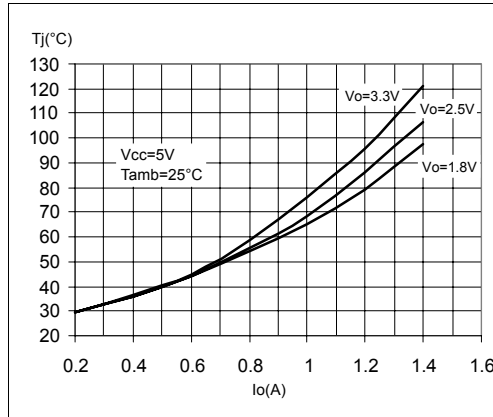


Figure 4. Load regulator

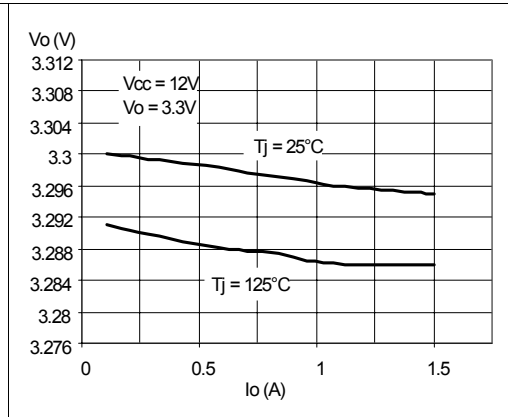


Figure 5. Junction temperature vs output current

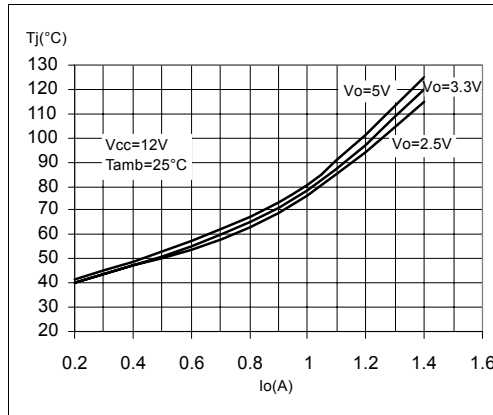


Figure 6. Line regulator

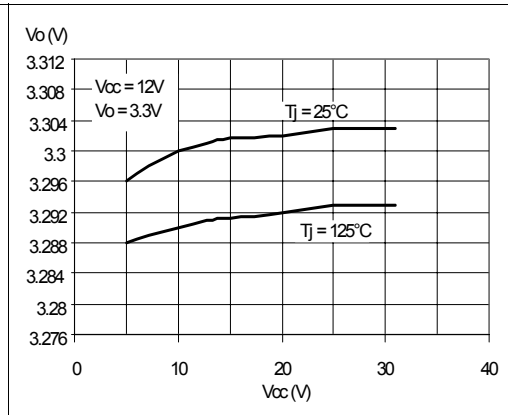


Figure 7. Junction temperature vs output current

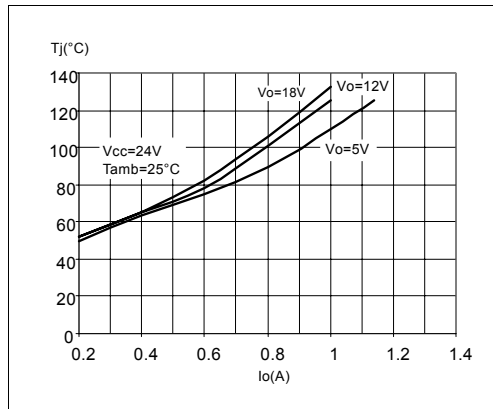


Figure 8. Output voltage vs junction temperature

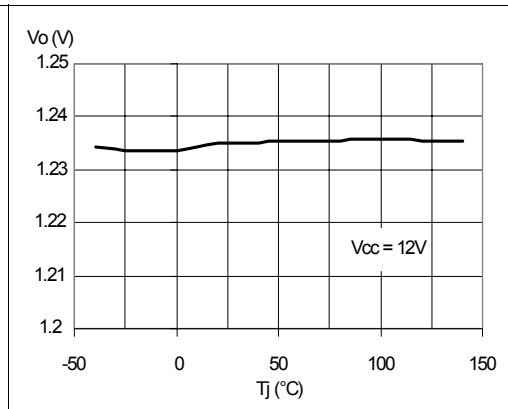


Figure 9. Quiescent current vs junction temperature

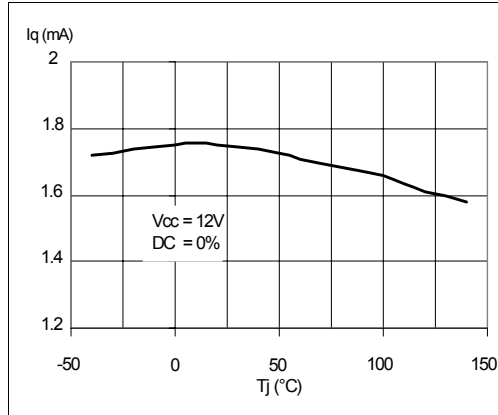


Figure 10. Switching frequency vs junction temperature

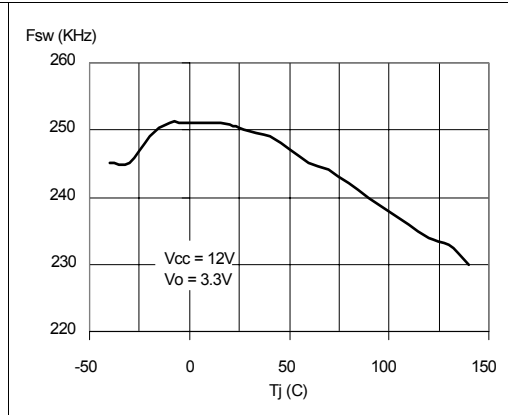


Figure 11. Shutdown current vs junction temperature

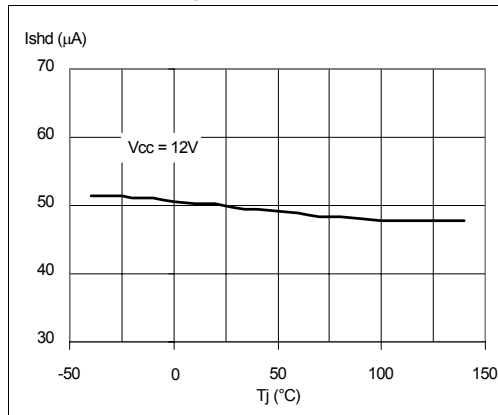


Figure 12. Efficiency vs output current

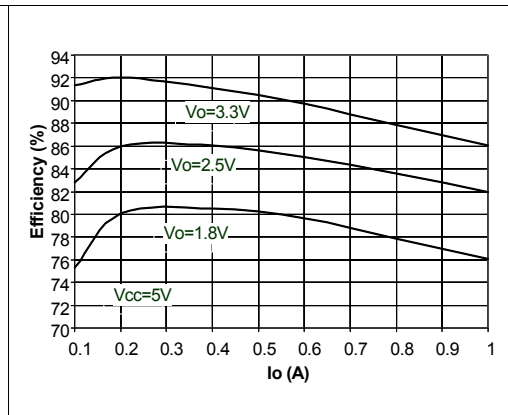
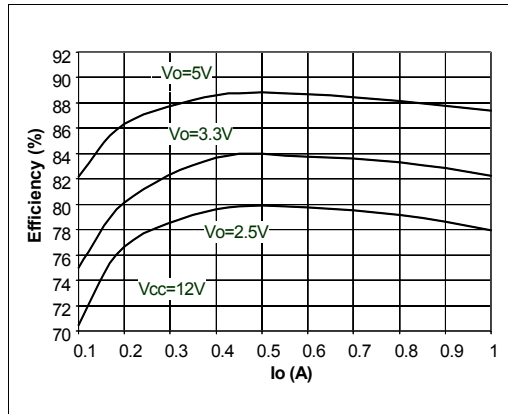


Figure 13. Efficiency vs output current



5 Application circuit

Figure 14. Demo board application circuit

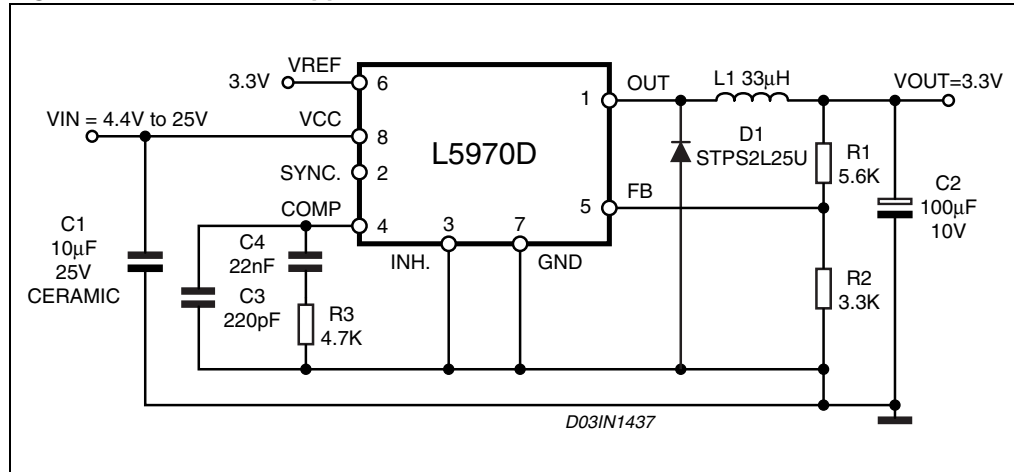


Table 5. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32DR61E106KA12L	10µF, 25V	MURATA
C2	POSCAP 10TPB100M	100µF, 10V	Sanyo
C3	C1206C221J5GAC	220pF, 5%, 50V	KEMET
C4	C1206C223K5RAC	22nF, 10%, 50V	KEMET
R1		5.6K, 1%, 0.1W 0603	Neohm
R2		3.3K, 1%, 0.1W 0603	Neohm
R3		4.7K, 1%, 0.1W 0603	Neohm
D1	STPS2L25U	2A, 25V	STMicroelectronics
L1	DO3316P-333	33µH, 2A	COILCRAFT

Figure 15. PCB layout (component side)

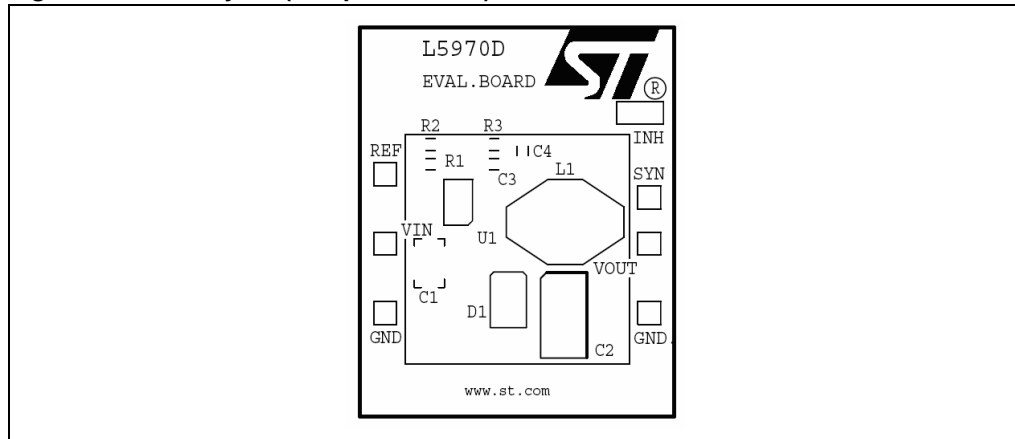


Figure 16. PCB layout (bottom side)

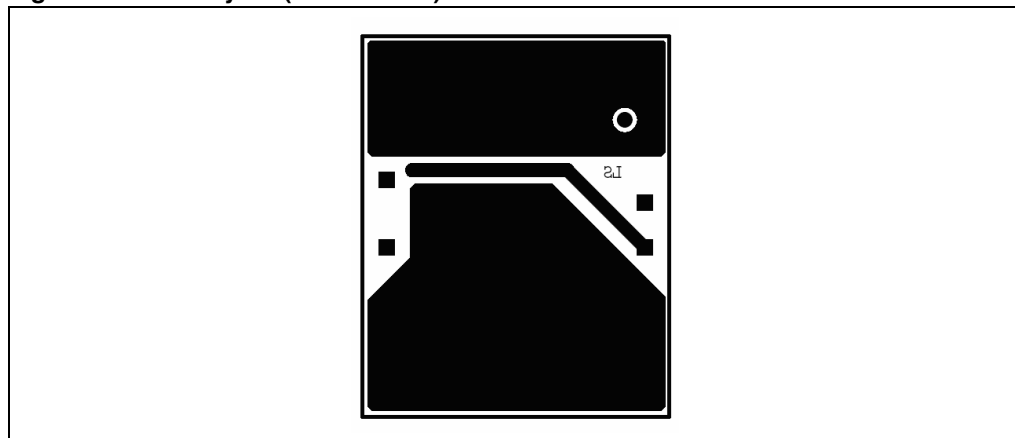
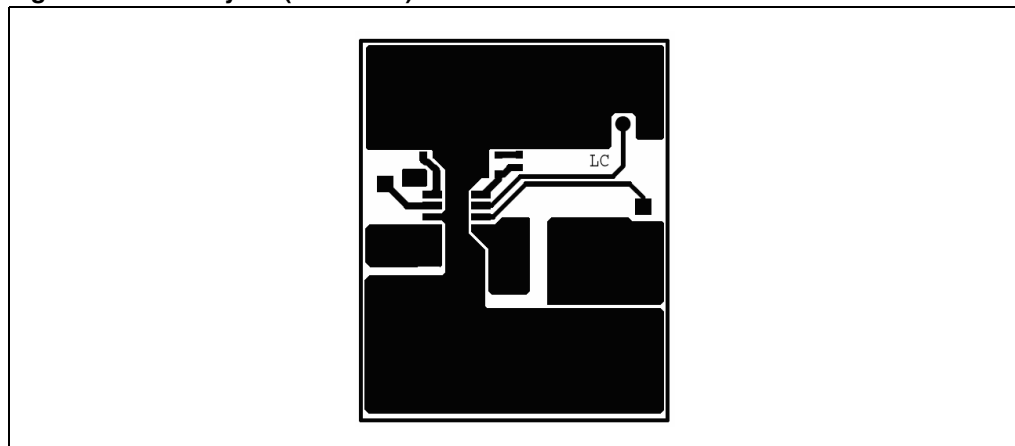


Figure 17. PCB layout (front side)



6 Application ideas

Figure 18. Dual output voltage with auxiliary winding

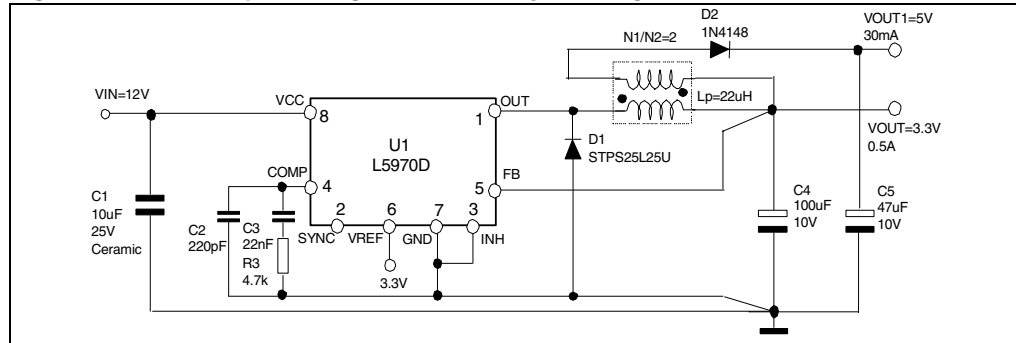


Figure 19. Buck-boost regulator

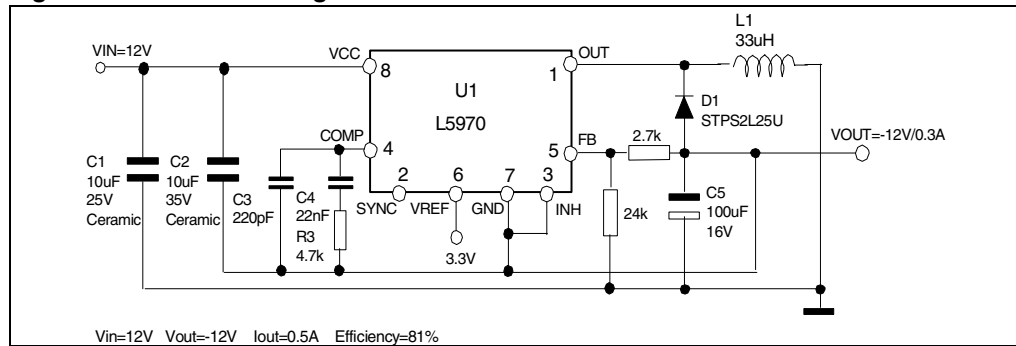


Figure 20. Positive Buck-Boost regulator

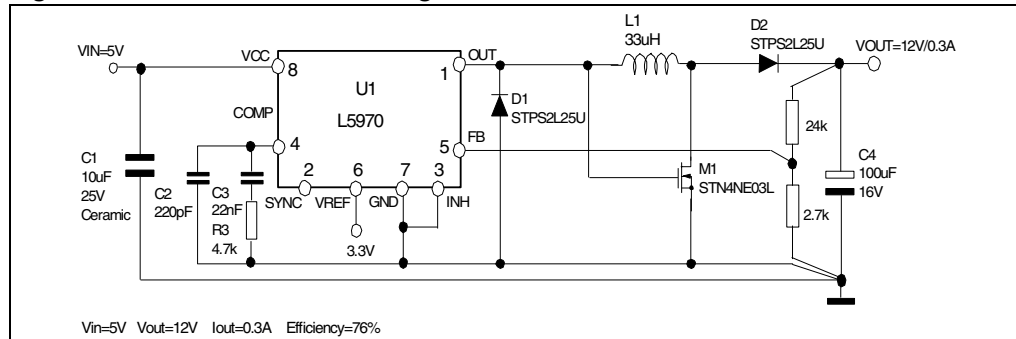
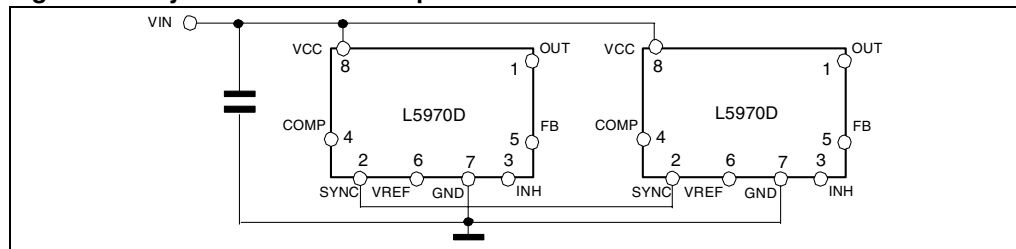


Figure 21. Synchronization example



7 Package mechanical data

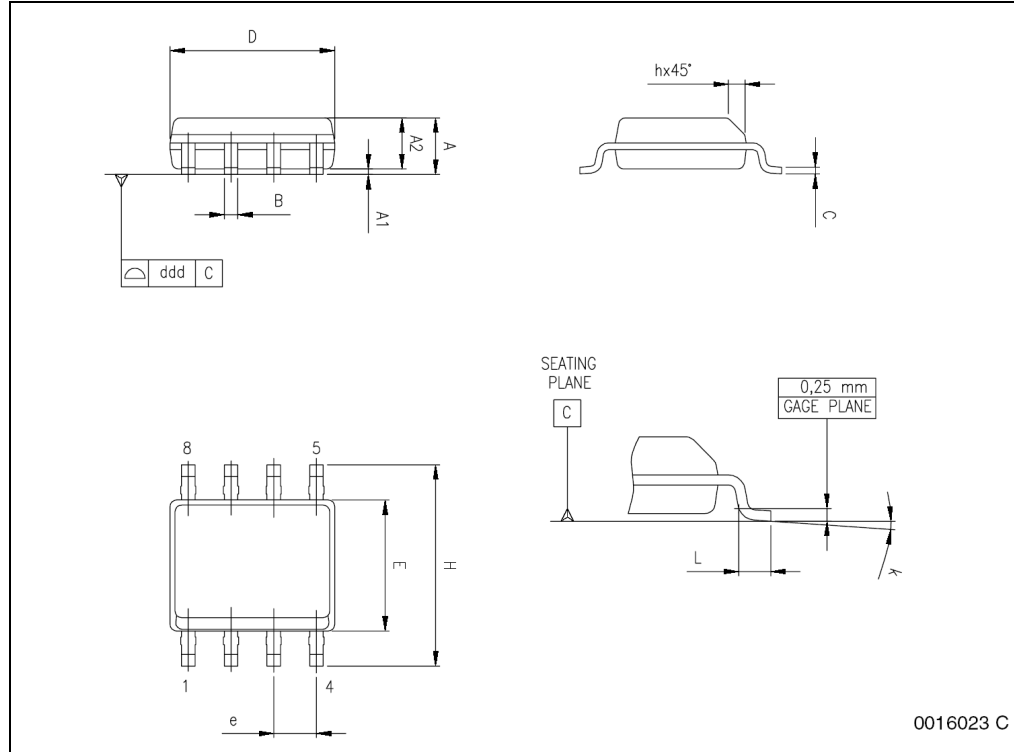
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D ⁽¹⁾	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 22. Package dimensions



8 Order codes

Table 7. Order codes

Part number	Package	Packaging
L5970D	SO8	Tube
L5970D013TR	SO8	Tape and reel

9 Revision history

Table 8. Revision history

Date	Revision	Changes
26-Jan-2007	14	Updated Table 5 on page 9
16-Mar-2007	15	Mechanical data typo
16-Oct-2007	16	Updated Section 5: Application circuit on page 9

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