WIDE INPUT AND OUTPUT, SYNCHRONOUS BUCK REGULATOR

FEATURES

- Input Voltage Range: 3V to 28V
- Output Voltage Range: 0.5V to 12V
- Constant On-Time control
- Excellent Efficiency at very low output current levels
- Gate drive charge pump option to maximize efficiency at higher output current levels
- Compensation Loop not Required
- Programmable switching frequency, soft start, and over current protection
- Power Good Output
- Precision Voltage Reference (0.5V, +/-1%)
- Enable Input with Voltage Monitoring Capability
- Pre-bias Start Up
- Under/Over Voltage Fault Protection
- 16pin 3x3 MLPQ lead free package
- RoHS compliant

DESCRIPTION

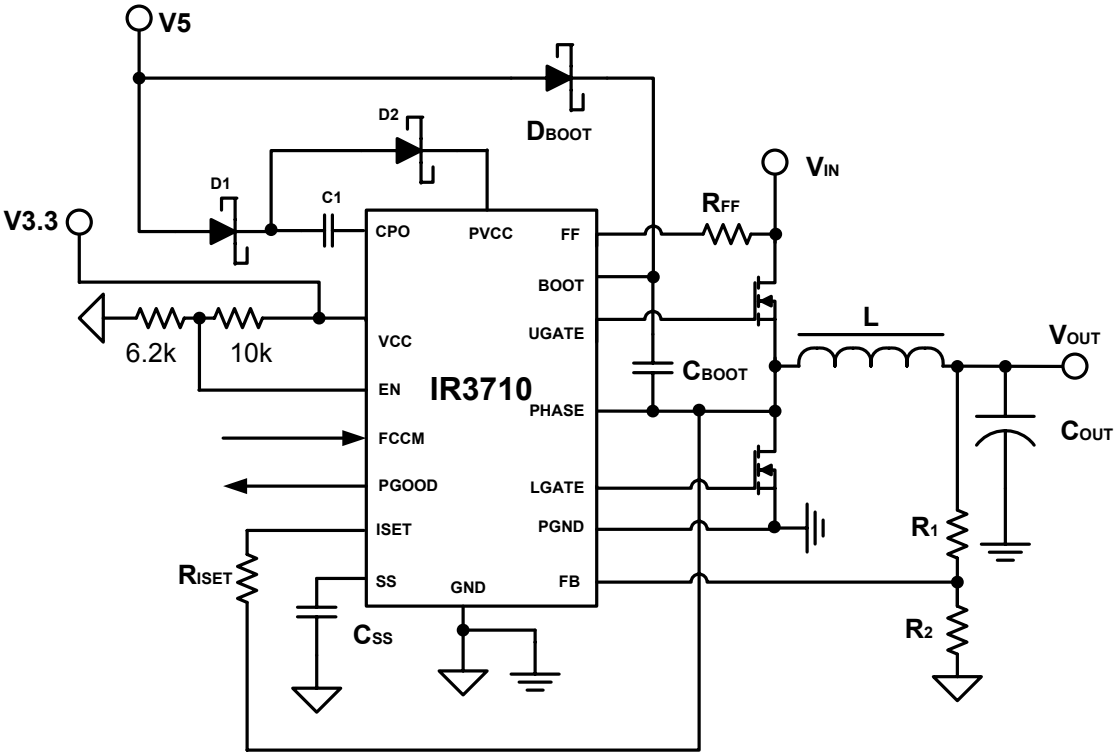
The IR3710 is a single-phase sync-buck PWM controller optimized for efficiency in high performance portable electronics. The switching modulator uses constant on-time control. Constant on-time with diode emulation provides the highest light-load efficiency required for all.

Programmable switching frequency, soft start, and over current protection allows for a very flexible solution suitable for many different applications. The combination of the gate drive charge pump option and constant on time control allow efficiency optimization in the whole output current range, making this device an ideal choice for battery powered applications.

Additional features include pre-bias startup, very precise 0.5V reference, over/under voltage shut down, power good output, and enable input with voltage monitoring capability.

APPLICATION CIRCUIT

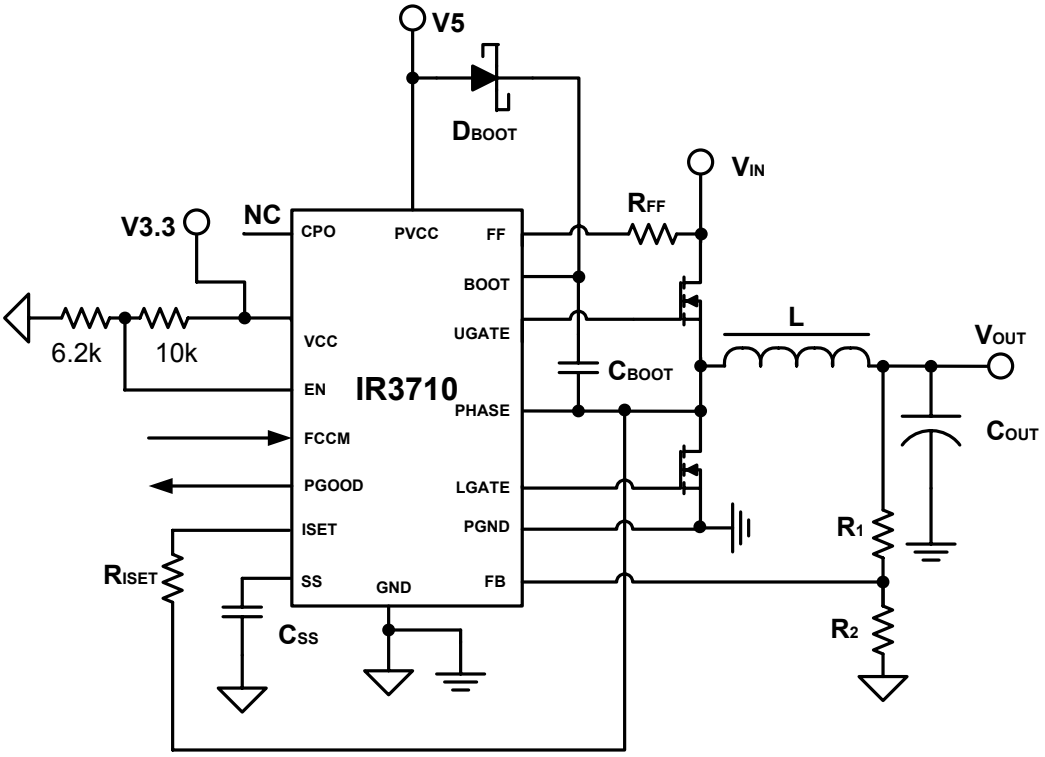
Enhanced Gate Drive Application Circuit:



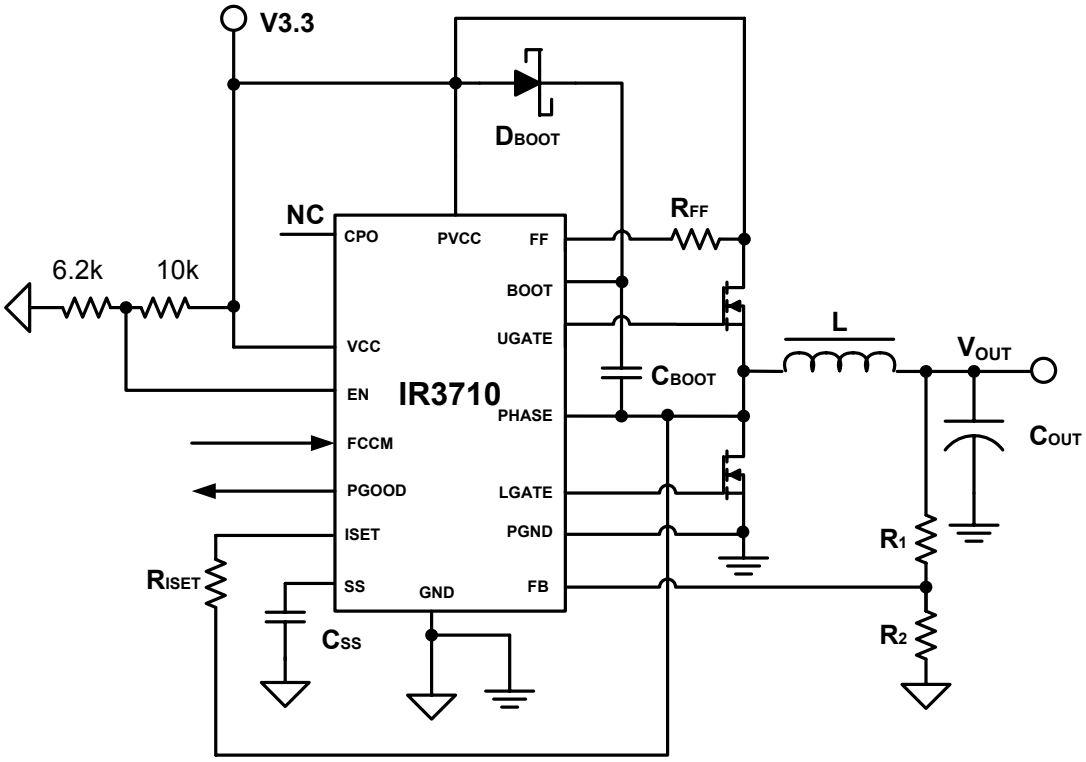
ORDERING INFORMATION

Package Description	Pin Count	Parts Per Reel
IR3710MTRPbF	16	4000

Fix Gate Voltage Application Circuit:



3.3V Input Voltage Application Circuit:



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Referenced to GND)
BOOT Voltage: .....40 V
PHASE Voltage:....-5V(100ns),-0.3V(DC) to 32.5 V
FF, ISET:.....32 V
BOOT minus PHASE Voltage:.....7.5 V
PVCC: .....7.5 V
VCC:.....3.9 V
PGOOD:.....3.9 V
PGND to GND:.....-0.3V to 0.3V
All other pins .....3.9 V

Operating Junction Temperature ..-10°C to +150°C
Storage Temperature Range ..... -65°C to 150°C
ESD Rating .....Class 1C
MSL Rating .....Level 2

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Definition	Min	Max	Units
V_{IN}	Input Voltage	3	28*	V
BOOT to PHASE	Supply Voltage		7.0	V
V_{OUT}	Output Voltage	0.5	12	V
Fs	Switching Frequency		1000	kHz

* Note: PHASE pin must not exceed 32.5V.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply: VCC = 3.3V, PVCC = 7.0V, $0^oC \le T_J \le 125^oC$

PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
BIAS SUPPLIES						
VCC Turn-on Threshold					3	V
VCC Turn-off Threshold			2.65			V
VCC Threshold Hysterisis				60		mV
PVCC Turn-on Threshold					3.05	V
PVCC Turn-off Threshold			2.65			V
PVCC Threshold Hysterisis				60		mV
VCC Shutdown Current		EN=LOW		25		µA
VCC Operating Current		EN=HIGH, No gate loading		1.2		mA
PVCC Shutdown Current		EN=LOW; PVCC = 5V		20		µA
FF Shutdown Current		EN=LOW		2		µA
CONTROL LOOP						
Reference Accuracy, V_{REF}		V_{FB} = 0.5V	0.495	0.5	0.505	V
On-Time Accuracy		R_{FF} = 180K, V_{IN} = 12.6V	270	300	330	ns
Zero Current Threshold		Measure at V_{PHASE}	-4.5		4.5	mV
Soft-Start Current		FCCM = EN = HIGH	8	10	12	µA

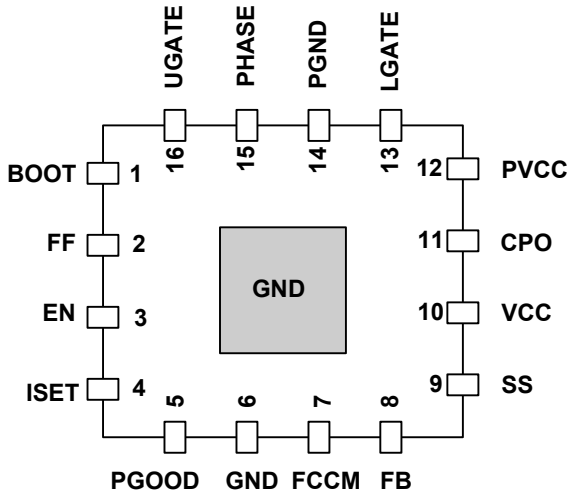
PARAMETER	NOTE	TEST CONDITION	MIN	TYP	MAX	UNIT
FAULT PROTECTION						
ISET pin output current			18	20	22	µA
Under Voltage Threshold		Falling V_{FB} & monitor PGOOD	0.37	0.4	0.43	V
Under Voltage Hysteresis		Rising V_{FB}		7.5		mV
Over Voltage Threshold		Rising V_{FB} & monitor PGOOD		0.6		V
PGOOD Delay Threshold (V_{SS})				0.6		V
GATE DRIVE						
UGATE Source Resistance	1	I_{GATE} = 0.1A		1.5	3	Ω
UGATE Sink Resistance	1	I_{GATE} = 0.1A		1	2	Ω
UGATE Rise and Fall Time		3nF load; 1V & 4V thresholds		10		ns
LGATE Source Resistance	1	I_{GATE} = 0.1A		1.5	3	Ω
LGATE Sink Resistance	1	I_{GATE} = 0.1A		0.4	1	Ω
LGATE Rise Time		6.8nF load; 1V to 4V		15		ns
LGATE Fall Time		6.8nF load; 4V to 1V		10		ns
Dead time		Measure time from V_{LGATE} = 1V to V_{UGATE} = 1V	5		50	ns
Minimum LGATE Interval				400		ns
CHARGE PUMP OUTPUT						
Source Resistance		I_{CPO} =15mA		3.3	5	Ω
Sink Resistance		I_{CPO} =15mA		1	2.1	Ω
Charge Pump Disable Threshold, $V_{CP\ TH}$		FCCM = HIGH	6.8	7.2		V
LOGIC INPUT AND OUTPUT						
EN Rising Threshold			1.14	1.22	1.3	V
EN Hysterisis			40	100	160	mV
EN Input Current					1	µA
FCCM Rising Threshold				1	1.2	V
FCCM Falling Threshold			0.5	0.7		V
FCCM Hysterisis				0.3		
FCCM Input Current					1	µA
PGOOD pull down resistance		I_{PGOOD} =2mA		50	100	Ω

NOTES:

1. Guaranteed by design, not tested in production

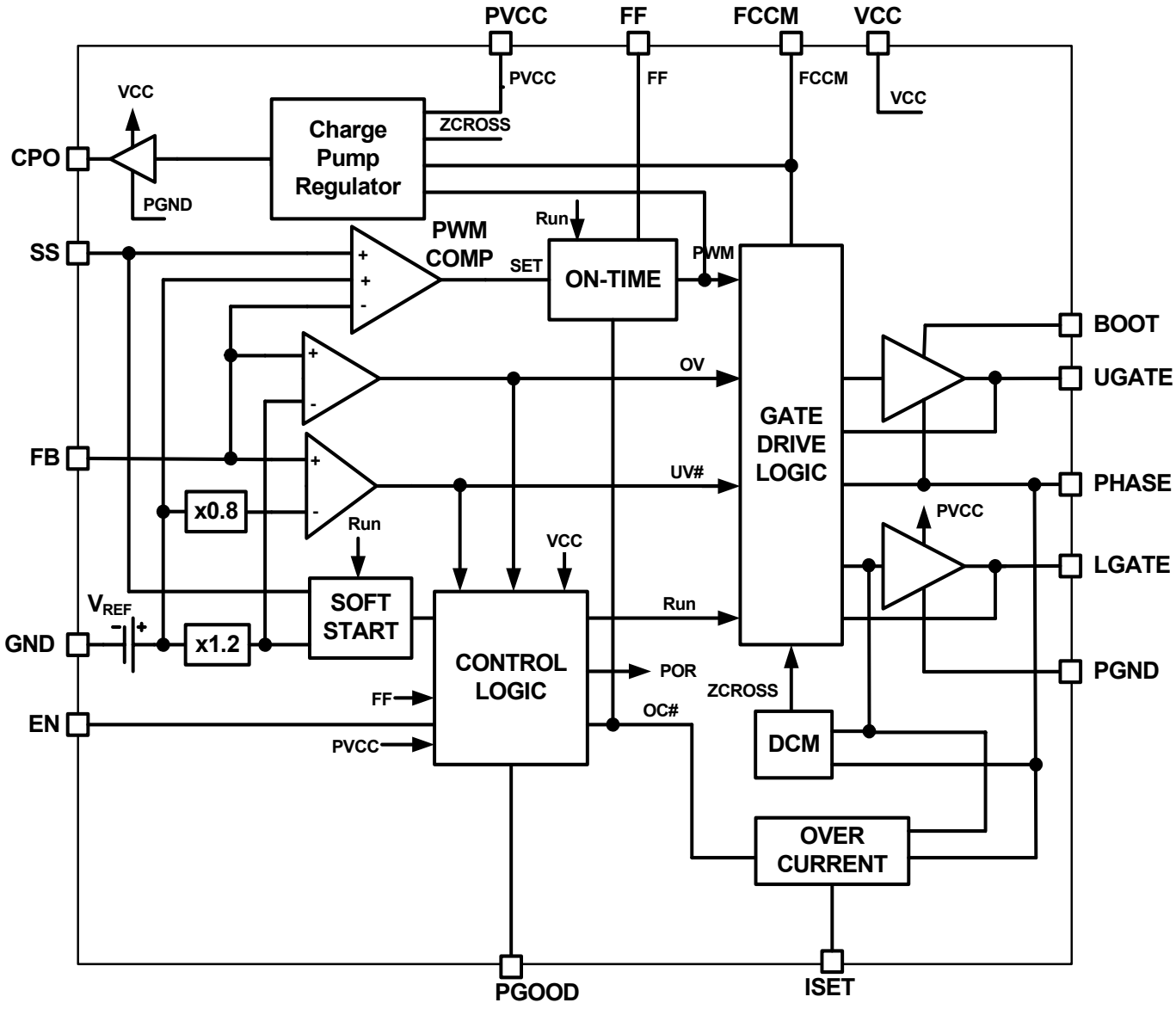
IC PIN ORDER AND DESCRIPTION

NAME	NUMBER	I/O LEVEL	DESCRIPTION
BOOT	1	V_{IN} +PVCC	Bootstrapped gate drive supply – connect a capacitor to PHASE
FF	2	V_{IN}	Input voltage feed forward – sets on-time with a resistor to V_{IN}
EN	3	3.3V	Enable input; EN = LOW inhibits GATE pulses
ISET	4	32V	Current limit setting with a resistor to PH pin
PGOOD	5	3.3V	Power good – pull up to 3.3V
GND	6	Reference	Bias return and signal reference
FCCM	7	3.3V	Force continuous conduction mode when pulled up to VCC
FB	8	3.3V	Feedback input
SS	9	3.3V	Set soft start slew-rate with a capacitor to GND
VCC	10	3.3V	IC bias supply
CPO	11	3.3V	Charge Pump Output
PVCC	12	7.4V	Gate drive supply
LGATE	13	PVCC	Lower gate drive for synchronous MOSFET
PGND	14	Reference	Power return – connect to source of synchronous MOSFET
PHASE	15	V_{IN}	Phase node (or switching node) of MOSFET half bridge
UGATE	16	V_{IN} + V5	Upper gate drive for control MOSFET



θ_{JA} = 49 °C/W
θ_{JC} = 4 °C/W

BLOCK DIAGRAM



TYPICAL OPERATING DATA

(Circuit of Figure 18, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, Unless otherwise noted.)

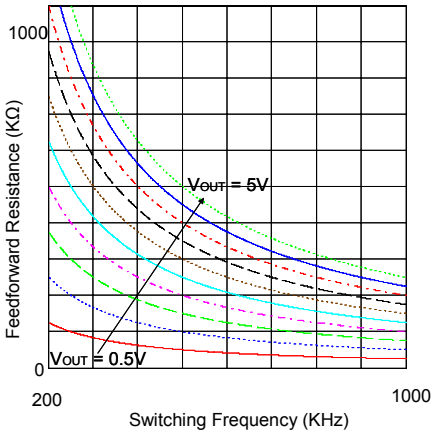


Figure 1. Feedforward Resistance vs Switching Freq: 0.5V V_{OUT} step, FCCM = HIGH.

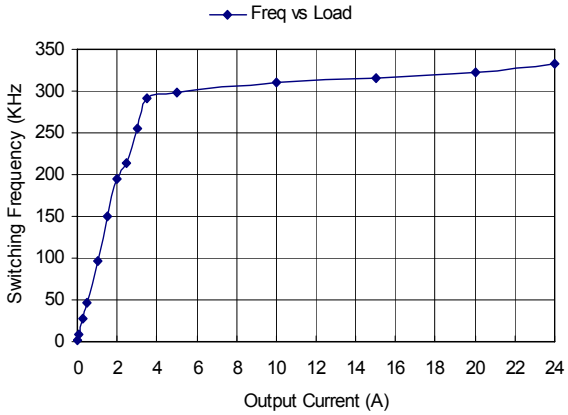


Figure 2. Switching Frequency vs Output Current

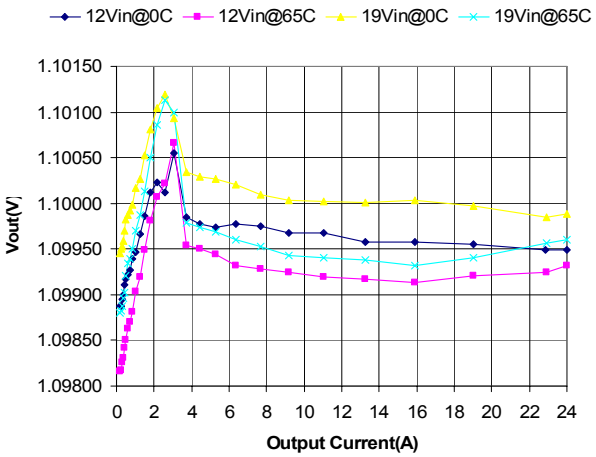


Figure 3. Output Voltage Regulation versus Input Voltage and Ambient Temperature

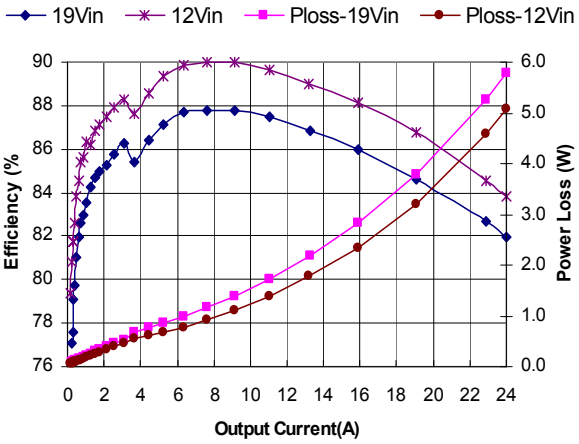


Figure 4. System Efficiency

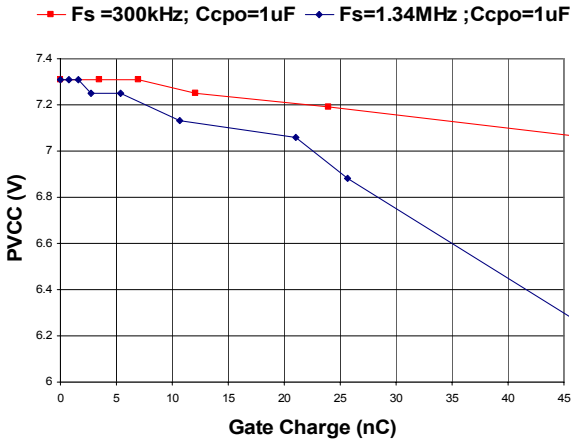


Figure 5. Charge Pump Regulation

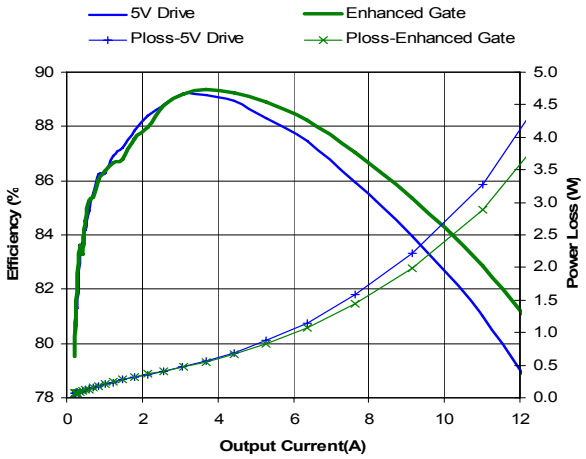
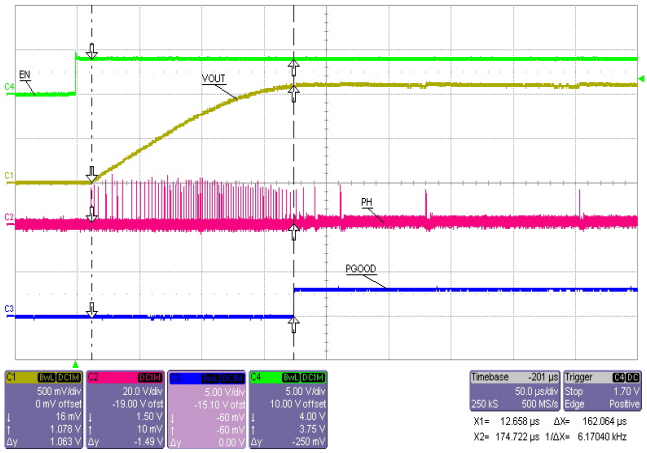


Figure 6. Charge Pump Efficiency Comparison: 1.25Vout, 12.6Vin, 300kHz, IRF8721/8721, 0.82uH (4.2mOhm DCR)

TYPICAL OPERATING WAVEFORM

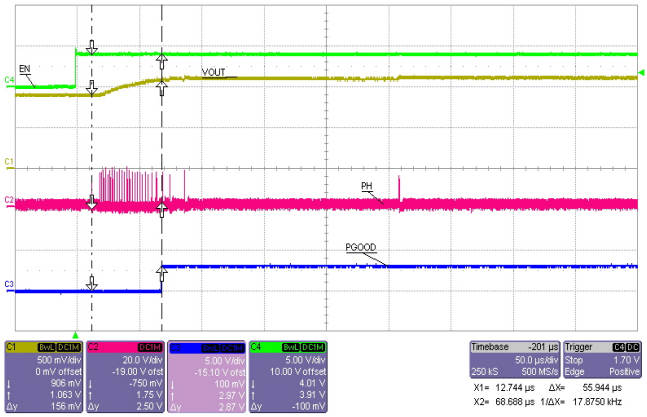
(Circuit of Figure 18, VCC = 3.3V, V5 = 5V, V_{IN} = 12.6V, Unless otherwise noted.)



CH1:Vout(0.5V/div), CH2: PHASE (20V/div)

CH3: PGOOD(5V/div), CH4:EN(5V/div) ; 50uS/div

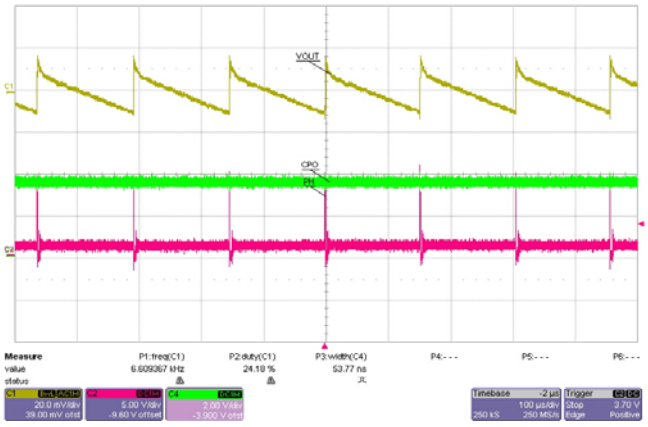
Figure 7. Start up with FCCM = Low @ 30mA



CH1:Vout(0.5V/div), CH2: PHASE (20V/div)

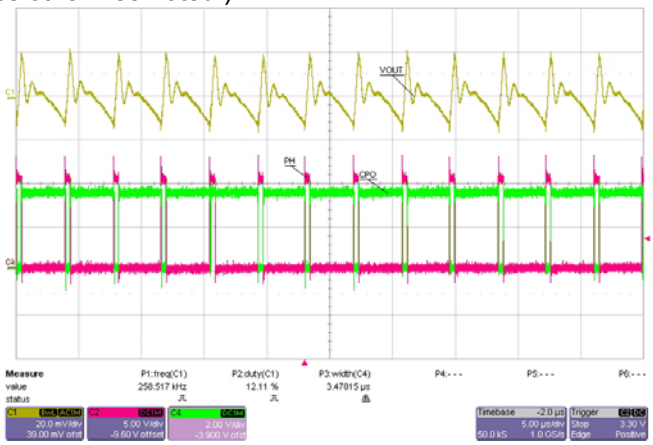
CH3: PGOOD(5V/div), CH4:EN(5V/div) ; 50uS/div

Figure 8. Start up with Prebias Vout, FCCM = Low @ 30mA



CH1:Vout(20mV/div), CH2: PHASE (5V/div), CH4: CPO(2V/div) ; 100uS/div

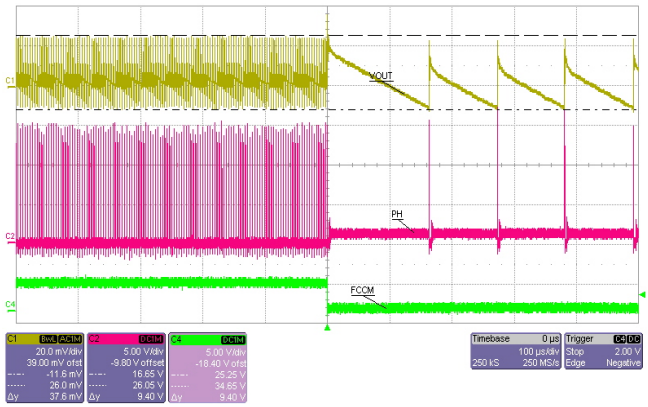
Figure 9. Charge Pump Off in DCM

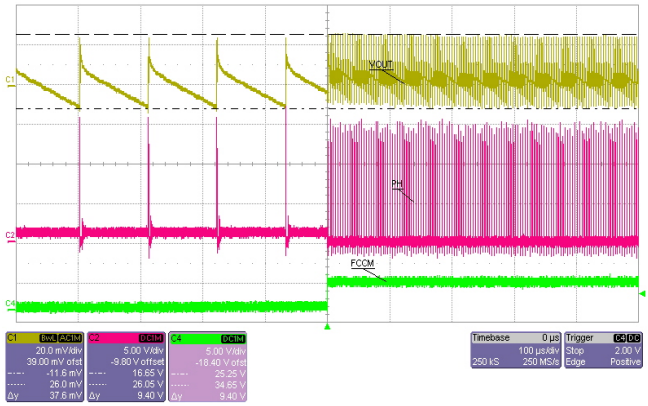


CH1:Vout(20mV/div), CH2: PHASE (5V/div)

CH4: CPO(2V/div) ; 5uS/div

Figure 10. Charge Pump ON

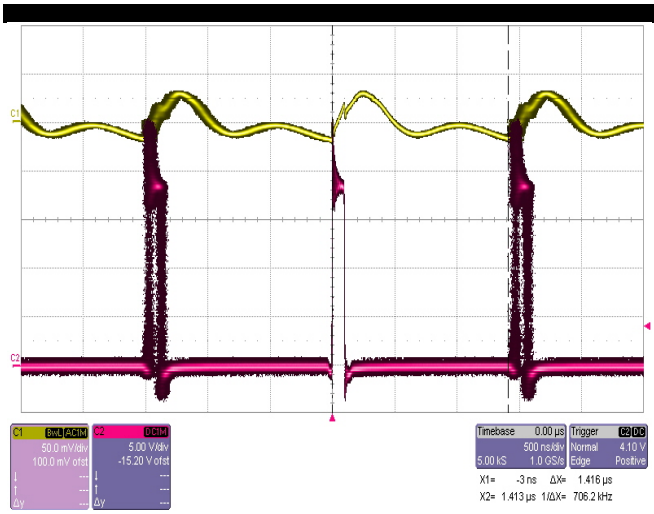




CH1:Vout(20mV/div), CH2: PHASE (5V/div)

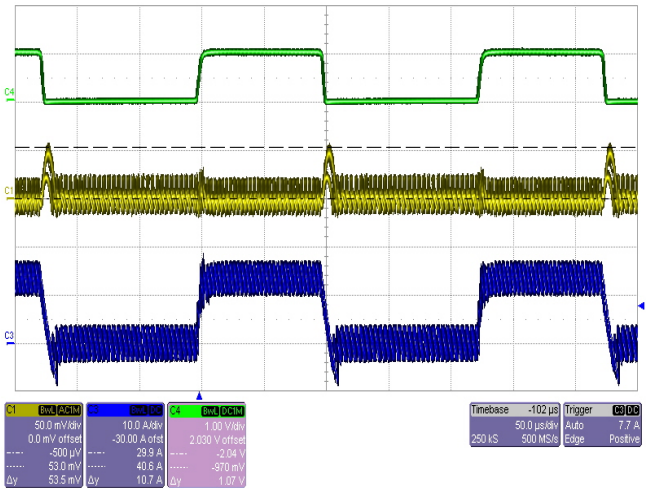
CH4: FCCM(5V/div) ; 100uS/div

Figure 11. DCM/FCCM Transition



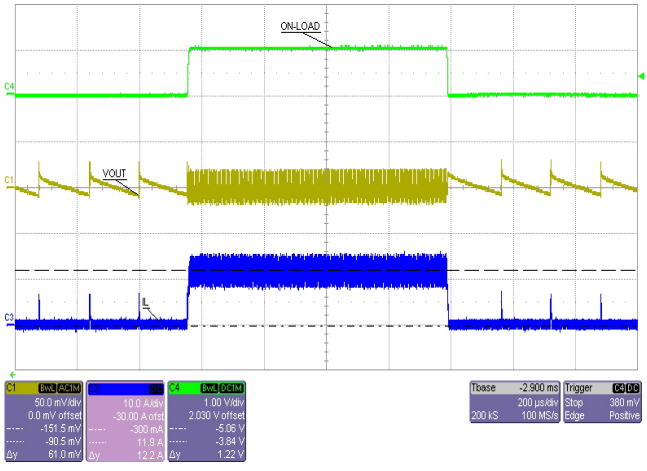
CH1:Vout(50mV/div), CH2: PHASE (5V/div);50uS/div

Figure 12. Frequency Variation less than 10% at 20A Load



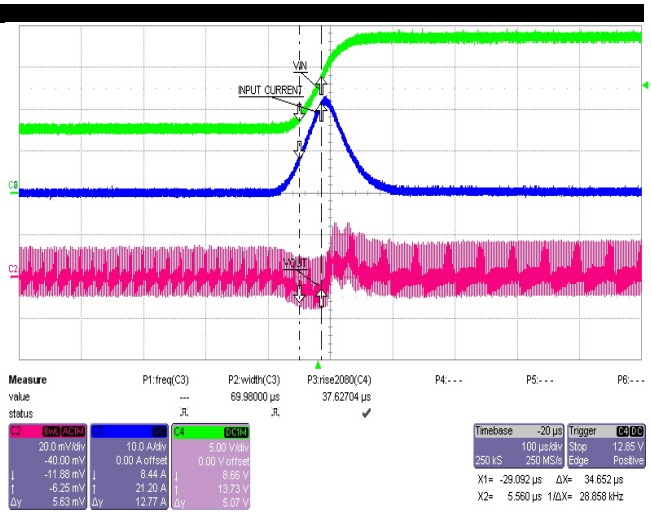
CH1:Vout(50mV/div), CH3: Inductor Current (10A/div), CH4: On-Board Load: 0A-14A ;50uS/div

Figure 13. Load Step Transient in CCM @ Vin = 19V



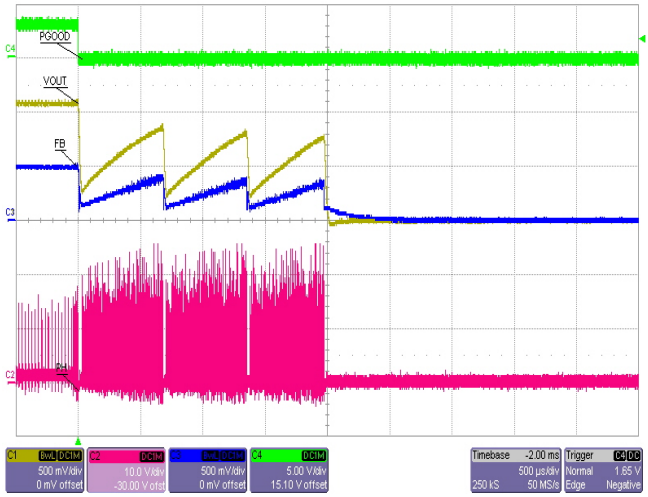
CH1:Vout(50mV/div), CH3: Inductor Current (10A/div), CH4: On-Board Load: 0.1A-12A; 50uS/div

Figure 14. Load Step Transient in DCM @ Vin = 19V



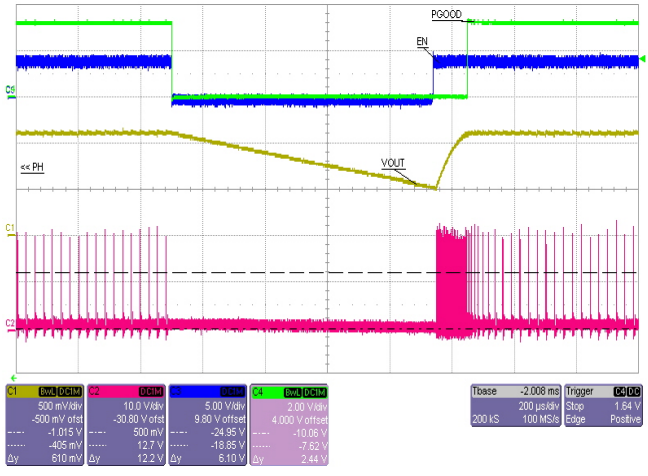
CH2:Vout(20mV/div), CH3: Input Current (10A/div), CH4: Input Voltage (5V/div) 8V to 19V; 100uS/div

Figure 15. Input Voltage Step at 2A Load with 0.1V/uS



CH1:Vout(0.5V/div), CH2: PHASE (10V/div), CH3: FB (0.5V/div), CH4: PGOOD (5V/div); 500uS/div

Figure 16. Over Current Protection at 30A



CH1:Vout(0.5V/div), CH2: PHASE (10V/div), CH3: EN (5V/div), CH4: PGOOD (2V/div); 200uS/div

Figure 17. Shutdown by EN in DCM @500mA

TYPICAL OPERATING CIRCUIT

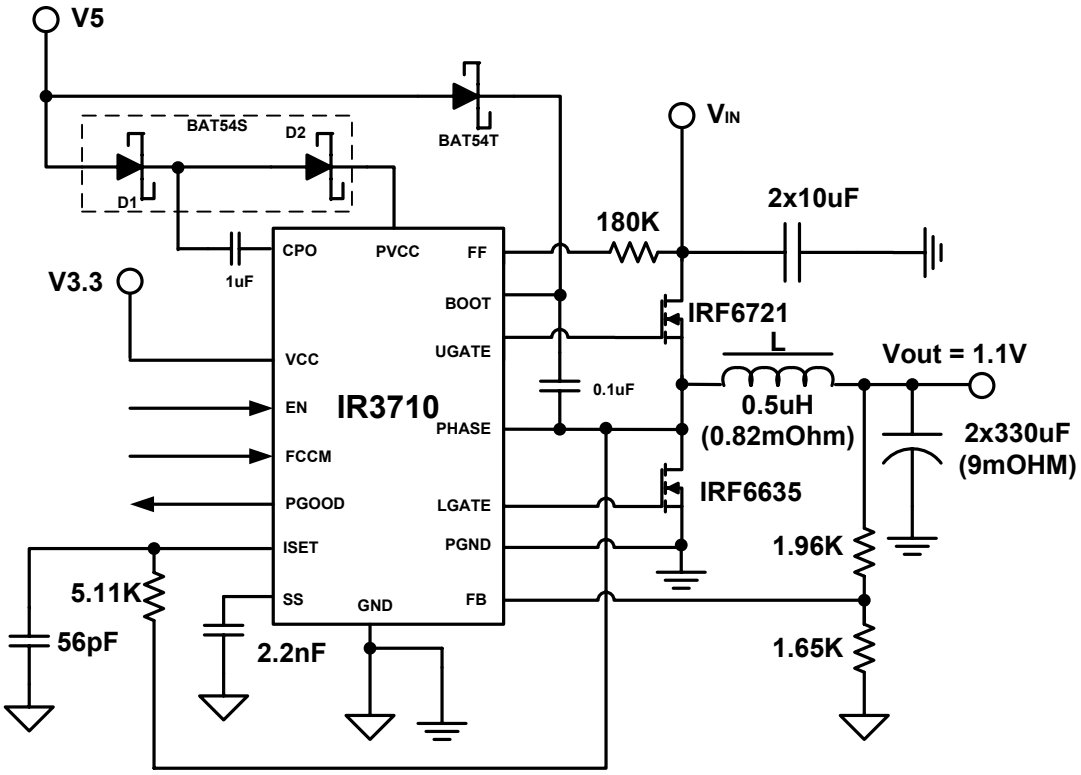


Figure 18. Typical Application Circuit for 24A Load

FUNCTIONAL DESCRIPTION

Refer to Block Diagram

ON-TIME GENERATOR

The PWM comparator initiates a SET signal (PWM pulse) when the FB pin falls below lower of the reference (VREF) or soft start (SS) voltage.

The PWM on-time duration is programmed with an external resistor (R_{FF}) from the input supply (V_{IN}) to the FF pin. The simplified equation for R_{FF} is shown in the equation 1. The FF pin is held to an internal reference after EN goes HIGH. A copy of the current in R_{FF} charges a timing capacitor, which set the on-time duration, as shown in equation 2.

$$R_{FF} = \frac{V_{OUT}}{1V \cdot 20\,pF \cdot F_{SW}} \quad (1)$$

$$T_{ON} = \frac{R_{FF} \cdot 1V \cdot 20\,pF}{V_{IN}} \quad (2)$$

SOFT START

An internal 10uA current source charges external capacitor on the SS pin to set the output voltage slew rate during the soft start interval. The output voltage reaches regulation when the FB pin is above the under voltage threshold and the UV# = HIGH. Once the voltage on the SS pin is above the PGOOD delay threshold, the combination of the SSDelay and UV# signals release the PGOOD pin. With EN = LOW, the capacitor voltage and SS pin is held to the FB pin voltage.

OVER CURRENT MONITOR

IR3710 monitors the output current every switching cycle. The voltage across the synchronous MOSFET, V_{PHASE} is monitored for over current and zero crossing. The minimum LGATE interval allows time to sample V_{PHASE}.

The over current trip point is programmed with a resistor from ISET to PHASE pins, as shown in equation 3. When over current is detected, output gates are tri-state and SS voltage is pulled to 0V. A new soft start cycle begins right after. If there is three (3) consecutive OC events, IR3710 will disable switching. Toggling VCC or EN will allow next start up.

$$R_{SET} = \frac{R_{DSON} \cdot I_{OC}}{20\,\mu A} \quad (3)$$

GATE DRIVE LOGIC

The gate drive logic features adaptive dead time, diode emulation, and a minimum lower gate interval. An adaptive dead time prevents the simultaneous conduction of the upper and lower MOSFETs. The lower gate voltage must be below approximately 1V after PWM goes HIGH before the upper MOSFET can be gated on. Also the upper gate voltage, the difference voltage between UGATE and PHASE, must be below approximately 1V after PWM goes LOW and before the lower MOSFET can be gated on.

Diode emulation is enabled after PGOOD = HIGH when FCCM is LOW. The control MOSFET is gated on after the adaptive delay for PWM = HIGH and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW. The lower MOSFET is driven 'off' when the signal Z_{CROSS} indicates that the inductor current reverses as detected by the PHASE voltage crossing the zero current threshold. The synchronous MOSFET stays 'off' until the next PWM falling edge.

When FCCM = HIGH, forced continuous current condition is selected. The control MOSFET is gated on after the adaptive delay for PWM = HIGH and the synchronous MOSFET is gated on after the adaptive delay for PWM = LOW.

The synchronous MOSFET gate is driven on for a minimum duration. This minimum duration allows time to recharge the bootstrap capacitor and allows the current monitor to sample the phase voltage.

CONTROL LOGIC

The control logic monitors input power sources for supply voltage conditions, sequences the converter through the soft-start and protective modes, and indicates output voltage status on the PGOOD pin. VCC and PVCC pins are continuously monitored. IR3710 is disabled if either of these voltages drops below falling thresholds.

IR3710 will initiate a soft start when the VCC and PVCC are in the normal range and the EN pin = HIGH. In the event of a sustained overload, a counter keep track of 4 consecutive soft-start cycles and disables IR3710.

If the overload is momentary and output voltage is within regulation before 4 consecutive soft-start cycles, PGOOD transitions HIGH to reset the counter.

OVER VOLTAGE PROTECTION

IR3710 monitors the voltage at FB node. If the FB voltage is above the threshold of over voltage, the gates are turn off and pulls PGOOD signal low. Toggling VCC or EN will allow next start up.

CHARGE PUMP

The purpose of the charge pump is to improve the system efficiency. A combination of VCC, V5 and three(3) external components are used to boost PVCC up to $V_{CP\ TH}$. PVCC drives the synchronous MOSFET and reduces the R_{DSON} when compared to a regular 5V rail driver. The lower R_{DSON} reduces the conduction power loss as discussed in the ***Power Loss*** section.

The charge pump is continuously enabled for FCCM = HIGH. The charge pump circuit is disabled when FCCM = LOW and the output loading is less than half of inductor current ripple. In this case, PVCC is two (2) diode voltage away from V5 rail. Therefore, the power loss for driver is reduced. The charge pump circuit stops switching the CPO pin for PVCC above $V_{CP\ TH}$.

It is not recommended to use PVCC for supply power to boot capacitor when use charge pump circuit. This can be exceeding the maximum rating of BOOT to PHASE pins and damages to the IC.

POWER UP SEQUENCE

With EN pin HIGH, IR3710 initiates a soft start when the VCC and PVCC are in the above ULVO threshold and V_{IN} is in normal range. The order of VCC, PVCC and V_{IN} is not require.

COMPONENT SELECTION

Selection of components for the converter is an iterative process which involves meeting the specifications and trade-offs between the performance and cost. The following sections will guide one through the process.

Power Loss

The main sources contributing to the power loss of a converter are switching loss of the upper MOSFETs, conduction loss of the lower MOSFETs, AC and DC losses in the inductor, and driving loss which is a large factor at light load condition.

In small duty cycle converter system, switching loss is main power loss of upper MOSFETs because its on-time is relatively small. To find the switching power loss, Figure 19 shows the typical turn-on waveform of the upper MOSFETs. Turn-off is quantitatively similar with x-axis reversed. The switching loss can be estimate as the cross sectional area in the figure. Equation 4 and 5 show the relationship of MOSFET's switching charge and loss.

$$W_{ON} = \frac{V_{IN} \cdot I_{PK}}{2}(t3 - t1) \quad (4)$$

$$P_{SW} = W_{ON} \cdot F_S = \frac{V_{IN} \cdot I_{PK}}{2} \cdot \frac{Q_{GS2} + Q_{GD}}{I_{GDr}} \cdot F_S \quad (5)$$

Fs is the switching frequency. I_{GDr} is gate driver current. To find the driver current, Figure 20 shows the simplified circuit of driver and MOSFET. I_{Gdr} can be found by using Ohm's law as shown in the equation 6 with an assumption that V_{Qgd} is the gate voltage during t_2 and t_3. Therefore, the turn on switching power loss of a cycle can be easily be found as shown in equation 7.

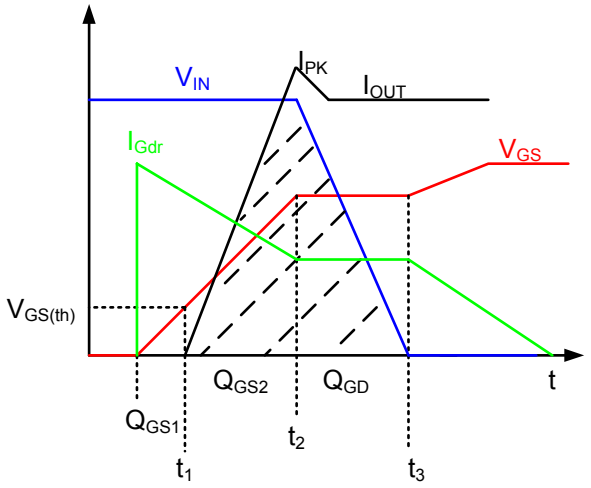


Figure 19. Typical Turn-On Waveform.

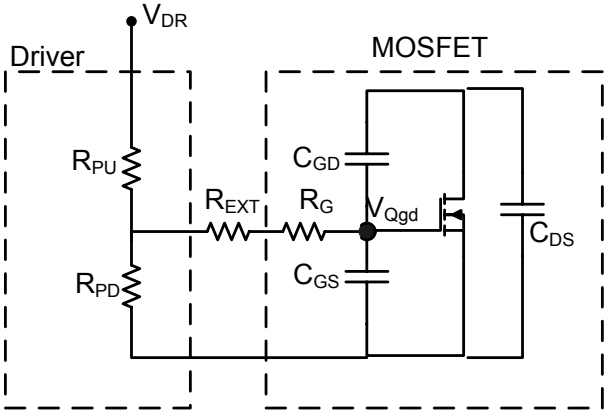


Figure 20. Simplify Driver and MOSFET Circuit.

$$I_{GDr(on\text{-}time)} = \frac{V_{DR} - V_{Qgd}}{R_{PU} + R_{EXT} + R_G} \quad (6a)$$

$$I_{GDr(off\text{-}time)} = \frac{V_{Qgd}}{R_{PD} + R_{EXT} + R_G} \quad (6b)$$

$$P_{SW} = \frac{V_{IN} \cdot I_{PK}}{2} \cdot \frac{Q_{GS2} + Q_{GD}}{I_{GDr(on\text{-}time)}} \cdot F_S \quad (7)$$

The reverse recovery power loss of the lower MOSFETs is also a factor of the upper MOSFET's

switching power loss because the output current flow through the lower MOSFET's body diode during the dead time stores some minority charges. When the upper MOSFETs turn on, it has to carry this extra current to remove the minority charges. The reverse recovery power loss can be found in equation 8.

$$P_{Qrr} = Q_{rr} \cdot V_{IN} \cdot F_S \quad (8)$$

By combining the P_{SW} and P_{Qrr}, the total switching power loss of the upper MOSFETs is much greater than its conduction loss. International Rectifier MOSFET datasheets has separated the gate charge of Q_{GS1} and Q_{GS2} so that the designer can calculate the switching power loss. Therefore, selection of the upper MOSFETs should consider those factors. Otherwise, the converter losses degrade the system efficiency and may exceed the thermal constraints.

The main power loss of lower MOSFETs is the conduction loss because its on-time is in the range of 90% of the switching period. The switching power loss of lower MOSFETs can be negligible because their body diode voltage drops are in the range of 1V. Equation 9 shows the conduction power loss calculation. T_S is inversely proportional to fs, and T_{OFF} is the on-time of the lower MOSFETs. $R_{DS(on)}$ increases approximately 30% with temperature.

$$P_{COND} = I_{RMS\_COND}^2 \cdot R_{DSON} \cdot \frac{T_{OFF}}{T_S} \quad (9)$$

$$\text{Where : } I_{RMS\_COND} = I_{OUT} \cdot \sqrt{1-D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{I_{OUT}}\right)^2}$$

The driver power loss is a small factor when heavily loaded but it can be significant contributor of degradation to the converter efficiency in light load. Equation 10 shows the driver power loss relating to the total gate charge of upper and lower MOSFETs and switching frequency.

$$P_{COND} = \frac{1}{T_S} \int_0^{T_S} V_{DR} \cdot I_{GDr} \cdot dt = V_{DR} \cdot Q_{GTotal} \cdot F_S \quad (10)$$

The low frequency and core losses are main factors of the total power loss of an inductor. Low frequency loss of an inductor is caused by the resistance of copper winding. The copper loss of the winding is shown in equation 11. The core loss of an inductor depends on the B-H loop characteristic, volume and frequency. This data can be obtained from the inductor manufactures.

$$P_{DCR} = I_{RMS}^2 \cdot DCR \quad (11)$$

$$\text{Where : } I_{RMS} = I_{OUT} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{I_{OUT}}\right)^2}$$

Inductor Selection

Inductor selection involves meeting the steady state output ripple requirement, minimizing the switching loss of upper MOSFETs, transient response and minimizing the output capacitance. The output voltage includes a DC voltage and a small AC ripple component due to the low pass filter which has incomplete attenuation of the switching harmonics. Neglecting the inductance in series with output capacitor, the magnitude of the AC voltage ripple is determined by the total inductor ripple current flow through the total equivalent series resistance (ESR) of the output capacitor bank.

$$\Delta I = \frac{V_{OUT}}{L} \cdot (1 - D) \cdot T_S = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot L \cdot F_S} \quad (12)$$

One can use equation 12 to find the inductance. The main advantage of small inductance is increased inductor current slew rate during a load transient, which leads to small output capacitance requirement as discussed in the ***Output Capacitor Selection*** section. The draw back of using smaller inductances is increased switching power loss in upper MOSFETs, which reduces the system efficiency and increases the thermal dissipation as discussed in the ***Power Loss*** section.

Input Capacitor Selection

The main function of the input capacitor bank is to provide the input ripple current and fast slew rate current during the load current step up. The input capacitor bank must have adequate to handle the total RMS current. Figure 21 shows a typical input current. Equation 13 shows the RMS input current. The RMS input current contains the DC load current and the inductor ripple current. As shown in equation 12, inductor ripple current is unrelated to the load current. The maximum RMS input current occurs at the maximum output current. The maximum power dissipate in the input capacitor equals the square of the maximum RMS input current times the input capacitor's total ESR.

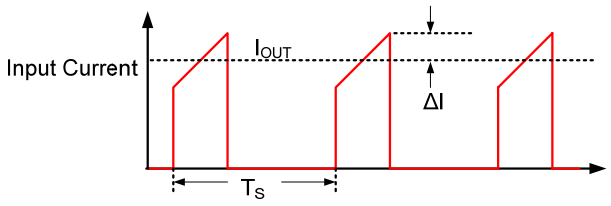


Figure 21. Typical Input Current Waveform.

$$I_{IN\_RMS} = \sqrt{\frac{1}{T_S} \cdot \int_0^{T_S} f^2(t) \cdot dt} = I_{OUT} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{I_{OUT}}\right)^2} \quad (13)$$

The voltage rating of the input capacitor needs to be greater than the maximum input voltage because of the high frequency ringing at the phase node. The typical percentage is 25%.

Output Capacitor Selection

Select the output capacitor involves meeting the overshoot requirement during the load removal, transient response when the system is demanding the current and meeting the output ripple voltage requirement. The output capacitor has the higher cost in the converter and increases the overall system cost. The output capacitor decoupling in the converter typically includes the low frequency capacitor, such as Specialty Polymer Aluminum, and mid frequency ceramic capacitors.

The first purpose of output capacitors is to provide the different energy when the load demands the current until the inductor current reaches the load's current as shown in figure 22. Equation 14 shows the charge requirement for certain load. The advantage of IR3710 at the load step is to reduce the delay, Tdmax, down to logic delay (in nanosecond) compare to fix frequency control method in microsecond or (1-D)*Ts. If the load increases right after the PWM signal low, the longest delay of Tdmax will be equal to the minimum lower gate on as shown in *Electrical Specification* table. IR3710 also reduces the total inductor time, which takes to reach output current, by increasing the switching frequency up to 2.5MHz. The result reduces the recovery time.

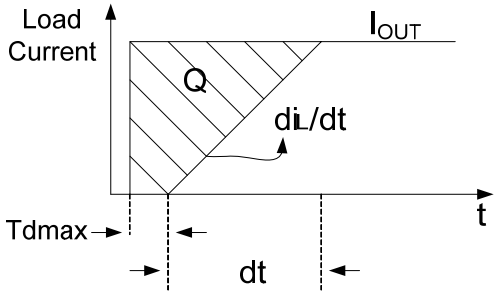


Figure 22. Charge Requirement during Load Step

$$Q = C \cdot V = I_{OUT} \cdot T_{dmax} + 0.5 \cdot I_{OUT} \cdot dt \quad (14a)$$

$$C_{OUT1} = \frac{1}{V_{DROP}} \left[\Delta I_{OUT} \cdot \frac{(1-D)}{F_S} + \frac{1}{2} \cdot \frac{L \cdot \Delta I_{OUT}^2}{(V_{IN} - V_{OUT})} \right] \quad (14b)$$

The output voltage drops, $V_{DROP,}$ initially depending on the characteristic of the output capacitor. V_{DROP} is the sum of equivalent series inductance (ESL) of output capacitor times the rate of change output current and ESR times the change of output current. V_{ESR} is usually much greater than V_{ESL}. IR3710 requires a total ESR such that the ripple voltage at the FB pin is 7mV.

The second purpose of the output capacitor is to minimize the overshoot of the output voltage when the load decreases as shown in Figure 23. By using the law of energy before and after the load removal, equation 15 shows the output capacitance requirement for a load step.

$$C_{OUT2} = \frac{L \cdot I_{STEP}^2}{V_{OS}^2 - V_{OUT}^2} \quad (15)$$

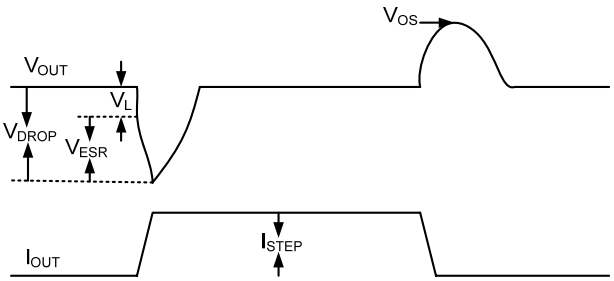


Figure 23. Typical Output Voltage Response Vaveform.

Boot Capacitor Selection

The boot capacitor starts the cycle fully charged to a voltage of $V_B(0)$. An equivalent gate drive capacitance is calculated by consulting the high side MOSFET data sheet and taking the ratio of total gate charge at the V5 voltage, $Q_G(V5)$, to the V5 voltage. $Q_G(V5)/V5$ is the equivalent gate drive capacitance C_g which will be used in the following calculations. The voltage of the capacitor pair C_B and C_g after C_g becomes charged at C_B's expense will be $V_B(0)$-ΔV. Choose a sufficiently small ΔV such that $V_B(0)$-ΔV exceeds the maximum gate threshold voltage to turn on the high side MOSFET. Since total charge Q_T is conserved, we can write the following equations.

$$V_B(0) \cdot C_B = Q_T = V(t_{on}) \cdot (C_B + C_g) \quad (16)$$

$$C_B = C_g \cdot \left(\frac{V_B(0)}{\Delta V} - 1 \right)$$

Choose a boot capacitor value larger than the calculated C_B. The voltage rating of this part needs to be larger than $V_B(0)$ plus the desired derating voltage. The voltage between BOOT and PHASE pins must not exceed the maximum rating of IR3710. Its ESR and ESL needs to be low in order to allow it to deliver the large current and di/dt's which drive MOSFETs most efficiently. In support of these requirements a ceramic capacitor should be chosen.

DESIGN EXAMPLE

Design Criteria:
Input Voltage, V_{IN}, = 6V to 21V
Output Voltage, V_{OUT} = 1.1V
Switching Frequency, F_S = 300KHz
Inductor Ripple Current, ΔI = 5A
Maximum Output Current, I_{OUT} = 20A
Over Current Trip, I_{OC} = 30A
Overshoot Allowance, V_{OS} = V_{OUT} + 150mV
Undershoot Allowance, V_{DROP} = 150mV

Find R_{FF} :

$$\mathbf{RFF} = \frac{\mathbf{1.1}V}{\mathbf{1}V \cdot \mathbf{20}\,pF \cdot \mathbf{300K}Hz} = \mathbf{183\,K}\Omega$$

Pick 182KΩ for 1% standard resistor

Find R_{SET} :

$$\mathbf{RSET} = \frac{\mathbf{1.3} \cdot \mathbf{3m}\Omega \cdot \mathbf{30}A}{\mathbf{20}\mu A} = \mathbf{5.85K}\Omega$$

1.3 factor is base on R_{DSON} of lower MOSFET increase over the temperature. Therefore, pick 5.9K for 1% standard resistor.

Find resistor divider for V_{OUT} = 1.1V:

$$\mathbf{VFB} = \frac{\mathbf{R2}}{\mathbf{R2} + \mathbf{R1}} \cdot \mathbf{VOUT} = \mathbf{0.5}V$$

R_2 = 8.45KΩ, R_1 = 10KΩ for 1% standard resistor

Choose the soft start capacitor:

Once the soft start time has chosen such as 100uS to reach to the reference voltage, a 2.2nF for C_{SS} is used to meet 100uS.

Choose inductor to meet design specification:

$$\mathbf{L} = \frac{\mathbf{VOUT} \cdot (\mathbf{VIN} - \mathbf{VOUT})}{\mathbf{VIN} \cdot \mathbf{\Delta I} \cdot \mathbf{Fs}} = \frac{\mathbf{1.1}V \cdot (\mathbf{21}V - \mathbf{1.1}V)}{\mathbf{21}V \cdot \mathbf{5}A \cdot \mathbf{300K}Hz} = \mathbf{0.7u}\,H$$

Choose the inductor with lowest DCR and AC power loss as possible to increase the overall system efficiency. For instance, choose FDUE1250-R56M from TOKO manufacture. The inductance of this part is 0.56uH and has 0.82mΩ DCR. The core loss for this inductor is 0.41W and 0.41W for DCR. Ripple current needs to recalculate with a chosen inductor.

$$\mathbf{\Delta I} = \frac{\mathbf{1.1}V \cdot (\mathbf{21}V - \mathbf{1.1}V)}{\mathbf{21}V \cdot \mathbf{0.56u}H \cdot \mathbf{300K}\,Hz} = \mathbf{6.2}A$$

Choose input capacitor:

$$\mathbf{I_{IN\_RMS}} = \mathbf{20}A \cdot \sqrt{\frac{\mathbf{1.1}V}{\mathbf{21}V}} \cdot \sqrt{\mathbf{1} + \frac{\mathbf{1}}{\mathbf{3}} \cdot \left(\frac{\mathbf{6.2}A}{\mathbf{20}A}\right)^{\mathbf{2}}} = \mathbf{4.7}A$$

A 10uF (ECJ3YB1E106M) from Panasonic manufacture has 6Arms at 300KHz. Due to the chemistry of multilayer ceramic capacitors, the capacitance varies over temperature and operating voltage both of AC and DC. Two (2) of 10uF are recommended. In practical solution, one (1) of 1uF is required along with 2x10uF. The purposes of 1uF are to suppress the switching noise and deliver a high frequency current.

Choose output capacitor:

To meet the undershoot specification, select a set of output capacitor which has an equivalent of 7.5mΩ (150mV/20A). To meet the overshoot specification, equation 15 will be use to calculate the minimum output capacitance. As a result, 516uF will be needed. Combine those two requirements, one can choose a set of output capacitor bank from manufactures such as SP-Cap (Specialty Polymer Capacitor) from Panasonic or POSCAP from Sanyo. Two (2) of 270uF (EEFUD0D271XR) from Panasonic are recommended. This capacitor has 12mΩ ESR which leaves margin for voltage drop of ESL during load step up. The typical ESL for this capacitor is around 2nH.

LAYOUT RECOMMENDATION

Bypass Capacitor:
One 1uF high quality ceramic capacitor is recommended to be placed as near VCC pin as possible. Other end of capacitor can be via or directly connect to GND plane. Use a GND plane not a thin trace to GND pin because this thin trace has higher impedance compare to GND plane. A 1uF is recommended for both V5 and PVCC and repeat the layout procedure above for those signals.
Charge Pump:
It is recommended to place D1, D2 and C2 as close to the CPO and PVCC pins as possible. If those components can not placed on the same layer as IR3710, a minimum of two (2) vias need for the connection of C2 and CPO pin and the connection of D2 and PVCC.
Boot Circuit:
C_{BOOT} needs to place near BOOT and PHASE pins to reduce the impedance during the turn on of the upper MOSFET. D_{BOOT} does not need to be close to C_{BOOT} because the average current to charge C_{BOOT} is small during the on time of lower MOSFET.

Gate Impedance:
We recommended placing LGATE signal path on top next to the source of low side MOSFET path and place UGATE signal path on top of PHASE signal path.
If the connection of PGND pin to the source of low side MOSFET is through an internal layer, it is recommended connecting through at least 2 vias by build a small island of next to PGND pin.
Power Stage:
Figure 24 shows the flowing current path for on and off period. The on time path has low average DC current with high AC current. Therefore, it is recommended to place input ceramic capacitor, upper and lower MOSFET in a tight loop as shown in Figure 24. The purpose tight loop of input ceramic capacitor is to suppress the high frequency (10MHz range) switching noise to reduce Electromagnetic Interference (EMI). If this path has high inductance, the circuit will cause voltage spike and ringing, increase the switching loss. The off time path has low AC and high average DC current. Therefore, it is recommended to layout with tight loop and fat trace at two end of inductor. The higher resistance of this loop increases the power loss. The typical resistance value of 1 ounce copper thickness has one-half mili-Ω per square.

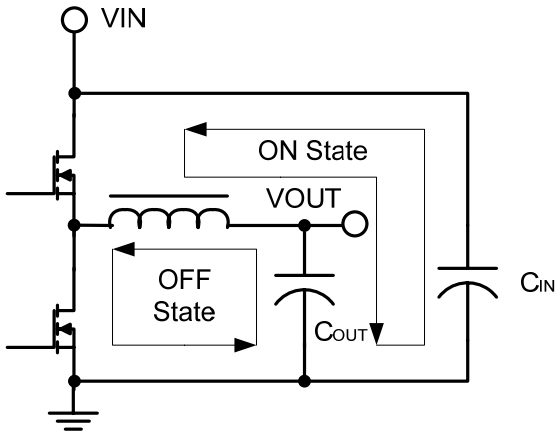


Figure 24. Current Path of Power Stage

PCB PAD AND COMPONENT PLACEMENT

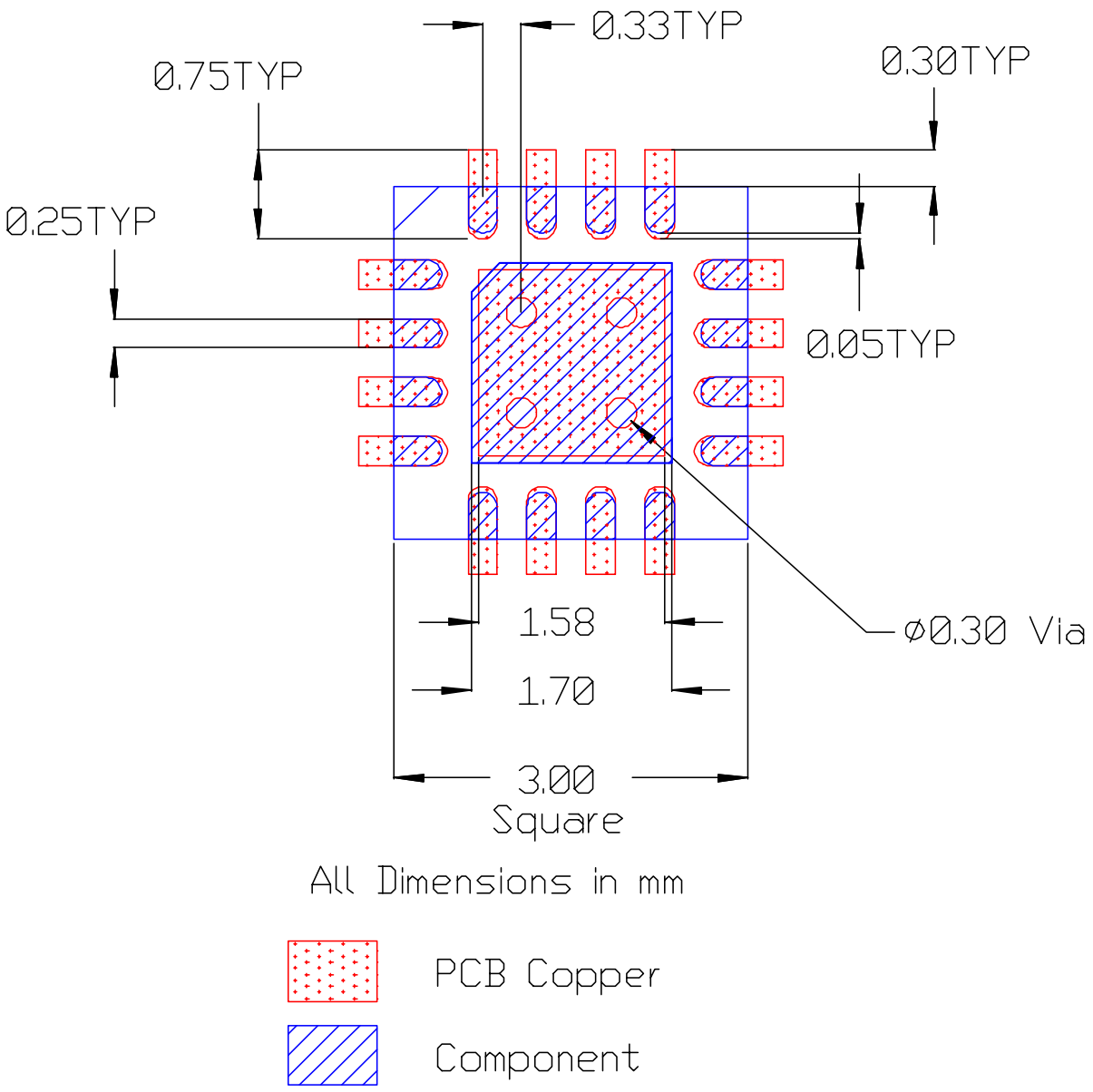


Figure 25. Ssuggested pad and component placement.

SOLDER RESIST

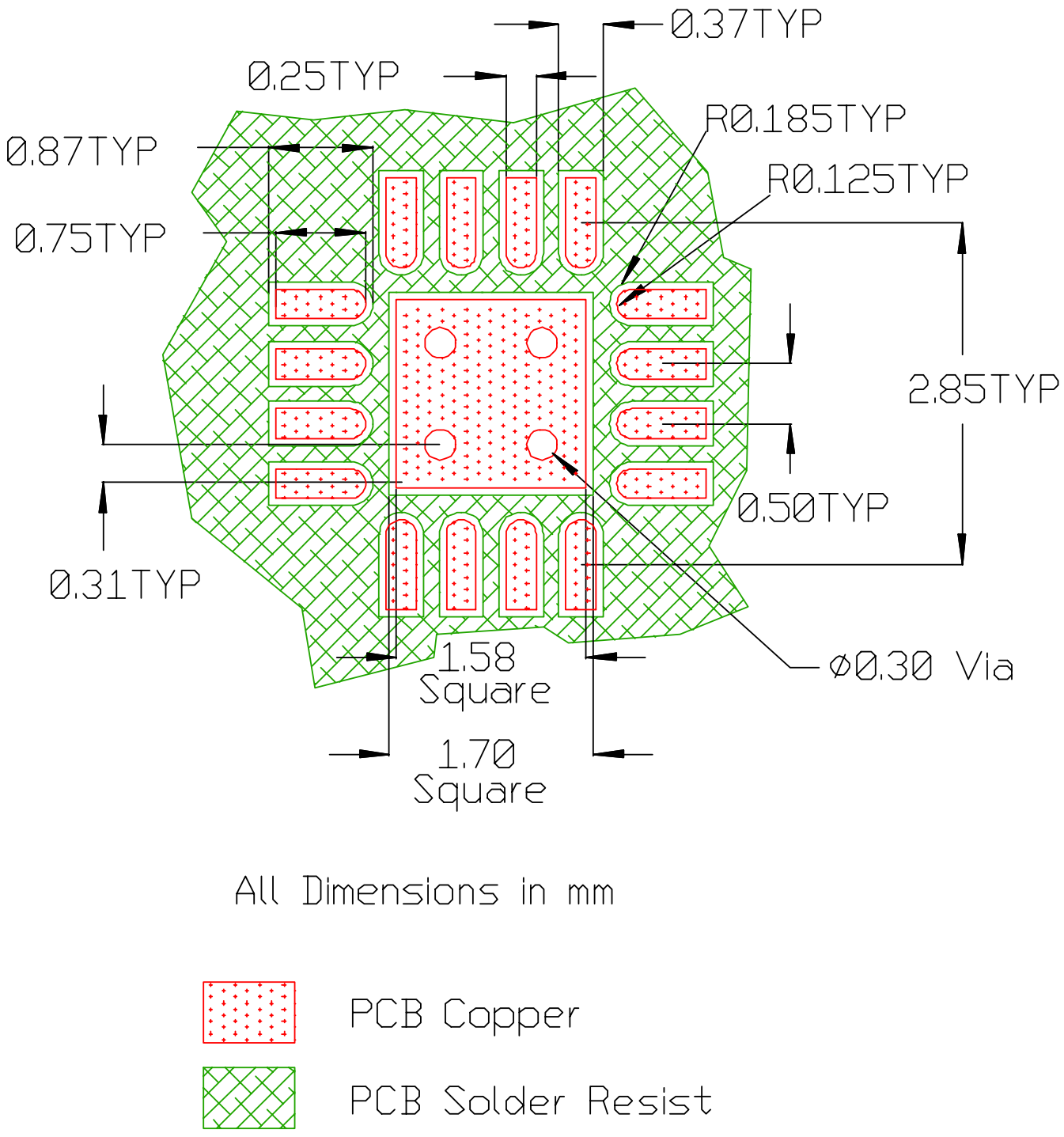


Figure 26. Suggested solder resist placement.

STENCIL DESIGN

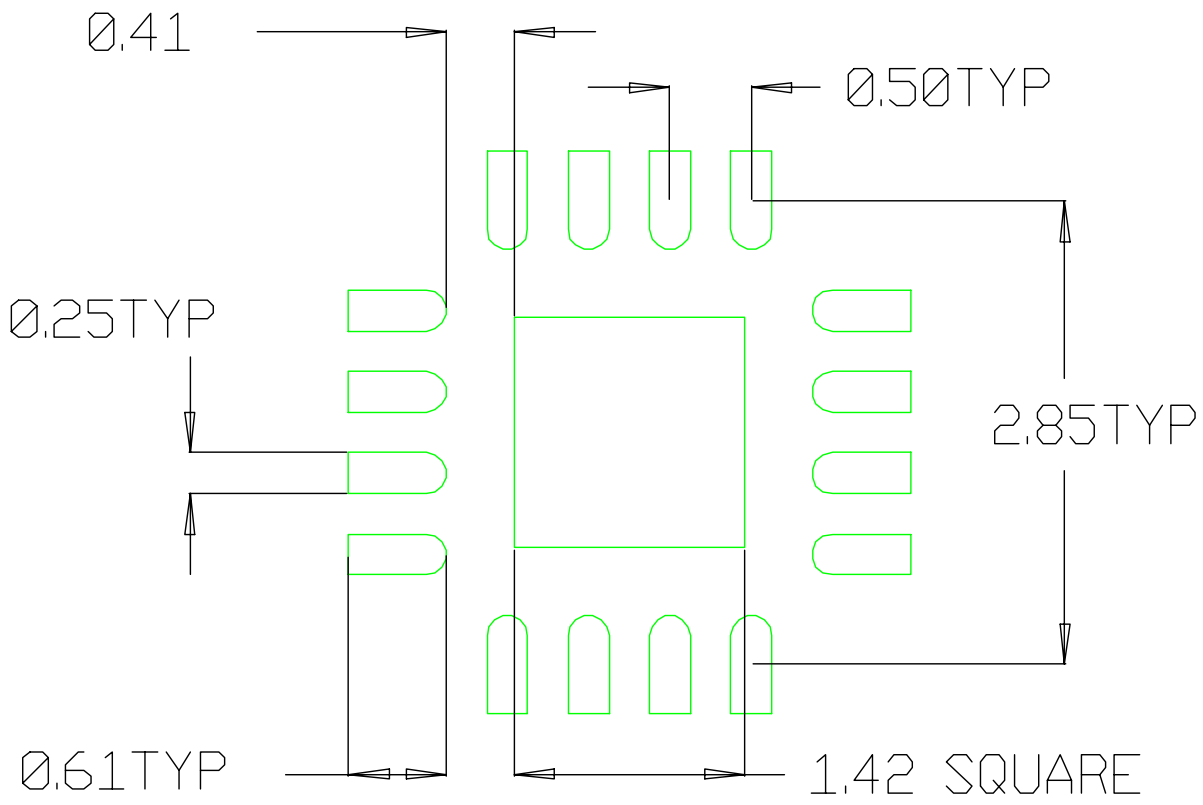
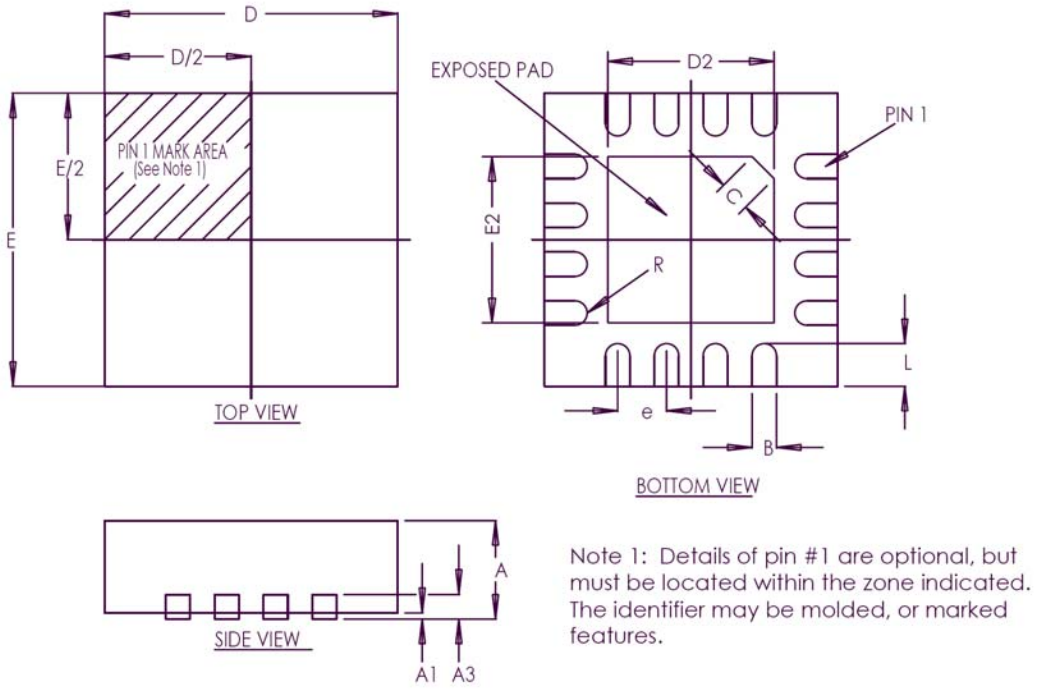


Figure 27. Suggested stencil design.

PACKAGE INFORMATION



SYMBOL	16-PIN 3x3 (unit: MM)		
DESIGN	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D		3.00 BSC	
D2	1.6	1.70	1.8
E		3.00 BSC	
E2	1.6	1.70	1.8
e		0.50 TYP	
L	0.30	0.40	0.50
R	0.125	---	---
C		0.35 TYP	

Figure 28. Package Outline Drawing

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
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