AP2007

Synchronous PWM Controller

■ Features

- Single 4.5V to 20V Supply Application
- 0.8V ± 2.0% Voltage Reference
- Virtual Frequency Control™
- Fast Transient Response
- Synchronous Operation for High Efficiency (93%)
- Short Circuit Protect
- Small Size with Minimum External Components
- Soft Start and Enable Functions
- Under Voltage Lockout Function
- SOP-8L **Pb-Free** Package

■ Applications

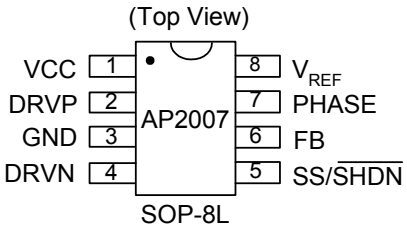
- Microprocessor Core Supply
- Low Cost Synchronous Applications
- Voltage Regulator Modules (VRM)
- Networking Power Supplies
- Sequenced Power Supplies
- Telecommunication Power Supplies.

■ General Description

The AP2007 is a low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The AP2007 is ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems or in distributed power applications where efficiency is important. High-side drive circuitry, and preset shoot-thru control, allows the use of inexpensive 1P+1N-channel power switches.
AP2007's features include temperature compensated voltage reference, Virtual Frequency Control™ method to reduce external component count, an internal 200KHz virtual frequency oscillator, under-voltage lockout protection, soft-start, shutdown function and current sense comparator circuitry.

Virtual Frequency Control is a trademark of PWRTEK, LLC.

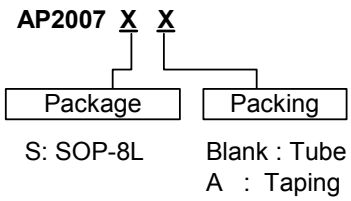
■ Pin Assignments



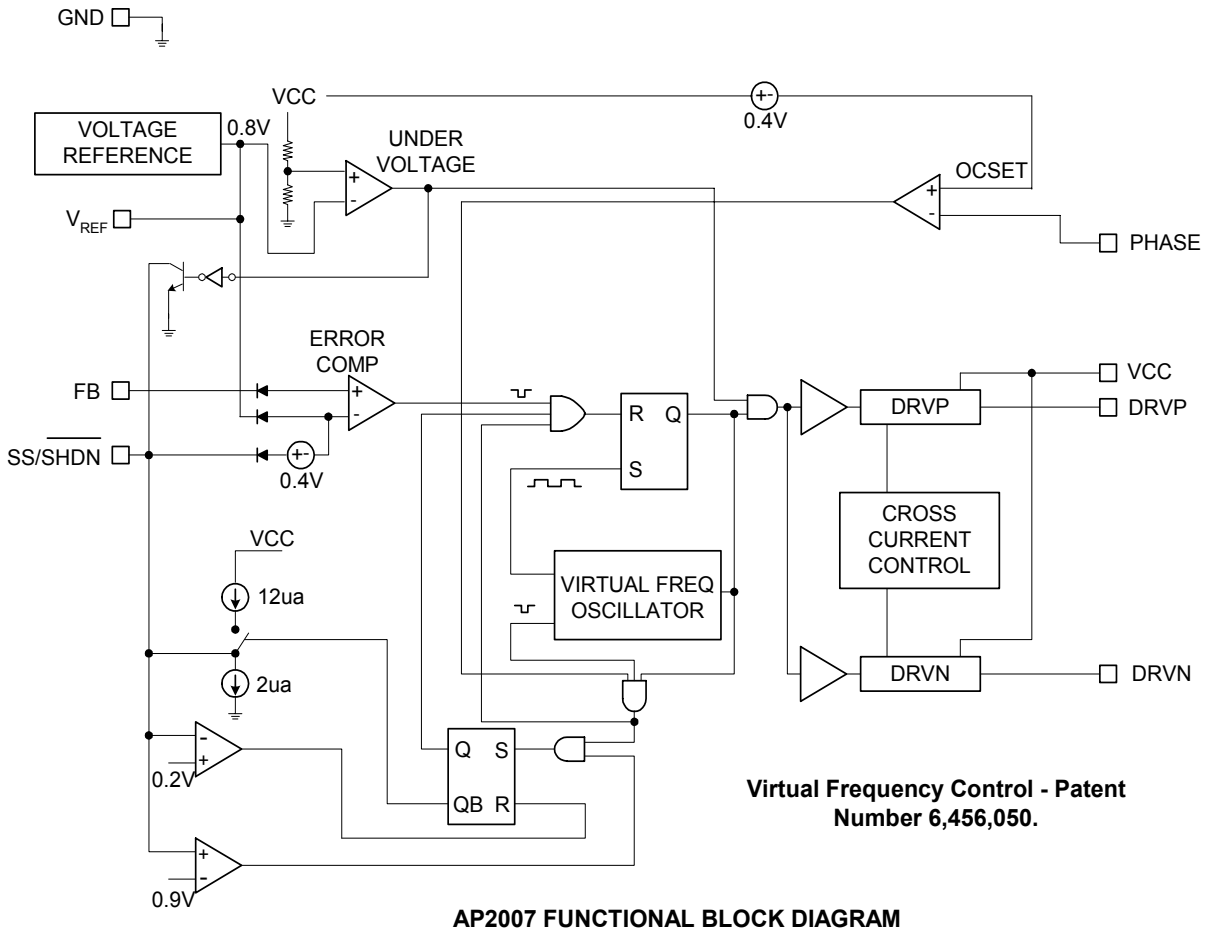
■ Pin Descriptions

Name	Description
VCC	Chip supply voltage
V_{REF}	Reference voltage
PHASE	Input from the phase node between the MOSFETs
DRVP	High side driver output (P MOSFET)
GND	Ground
DRVN	Low side driver output (N MOSFET)
FB	Feedback input
SS/$\overline{SHDN}$	Soft start, a capacitor to ground sets the slow start time / Shutdown function

■ Ordering Information



■ Block Diagram



Virtual Frequency Control - Patent Number 6,456,050.

AP2007 FUNCTIONAL BLOCK DIAGRAM

■ Absolute Maximum Ratings

Symbol	Parameter	Range.	Unit
V_{IN}	VCC to GND	-1 to 22	V
V_{PHASE}	PHASE to GND	-1 to 22	V
V_{DRVP}	DRVP to GND	-1 to 22	V
V_{DRVN}	DRVN to GND	-1 to 22	V
θ_{JC}	Thermal Resistance Junction to Case	90	°C/W
θ_{JA}	Thermal Resistance Junction to Ambient	250	°C/W
T_{OP}	Operating Temperature Range	-40 to +85	°C
T_{ST}	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering) 10 Sec.	300	°C

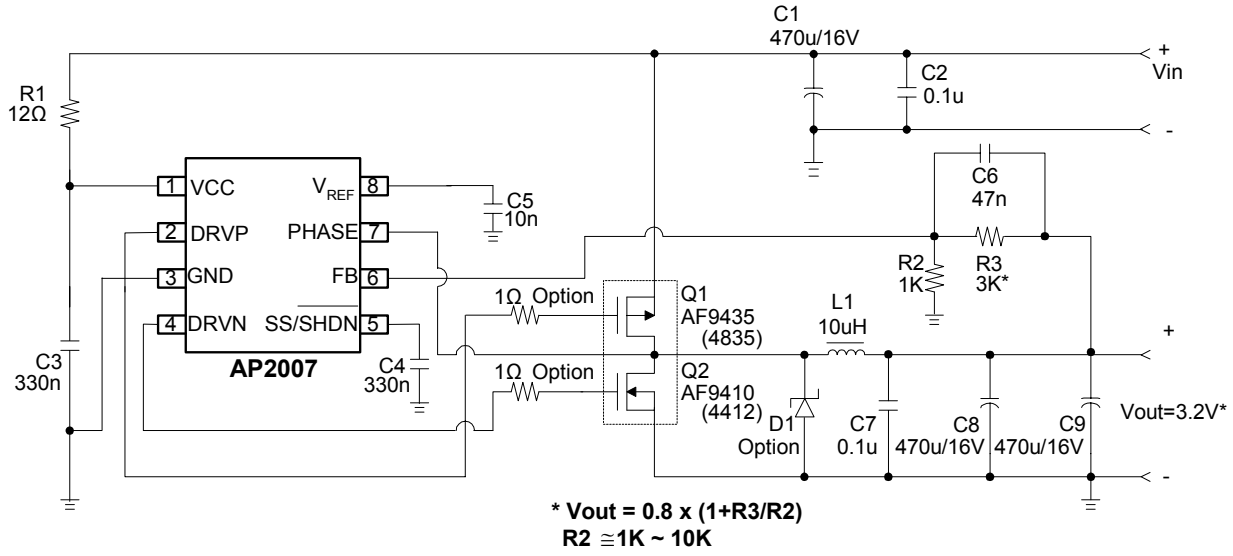
■ Electrical Characteristics

Unless specified: V_{CC} =12V; GND = 0V;V_O = 5V; T_J = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	Supply Voltage (Recommended)		4.5	-	20	V
I_{CC}	Supply Current	DRVP & DRVN are floating	-	9.5	-	mA
ΔV_{LINE}	Line Regulation	V_O = 2.5V	-	0.5		%
Error Comparator						
A_{OL}	Gain (A_{OL})		-	70	-	dB
I_B	Input Bias		-	0.2	1	uA
Oscillator						
F_{OSC}	Oscillator Frequency		-	200	-	KHz
DC_{MAX}	Oscillator Max Duty Cycle		80	85	-	%
Mofset Drivers						
I_{DRVP}	DRVP Source/Sink	$V_{CC} - V_{DRVP}$ =3V $V_{DRVP} - V_{GND}$ = 2V	0.5	1	-	A
I_{DRVN}	DRVN Source/Sink	$V_{CC} - V_{DRVN}$ = 3V $V_{DRVL} - V_{GND}$ = 2V	0.5	1	-	A
V_{DRVL}	DRVP/N Low Level Voltage		-	-	1.2	V
V_{DRVH}	DRVP/N High Level Voltage		V_{CC}-1.2	-	-	V
Protection						
T_{DEAD}	Dead Time	DRVP & DRVN are floating	-	150	-	nS
Vocset	Over Current Setting Voltage			0.4		V
$V_{DRVP/N}$	DRVP/DRVN System Error Voltage (Note3)	V_{SS}=Low, V_{CC}＜3.8, over current happen	V_{CC}-1.2	-	-	V
Reference						
V_{REF}	Reference Voltage	0°C to 70°C	0.784	0.8	0.816	V
	Accuracy		-2	-	+ 2	%
Soft Start						
I_{SSC}	Charge Current	V_{SS} = 1.5V	8.0	10	12	uA
I_{SSD}	Discharge Current	V_{SS} = 1.5V	1.3	2	2.7	uA
Under voltage lockout (UVLO)						
V_{UT}	Upper Threshold Voltage (V_{CC})		-	4.0	-	V
V_{LWT}	Lower Threshold Voltage (V_{CC})		-	3.8	-	V
V_{HT}	Hysteresis (V_{CC})		-	200	-	mV

Note 1. Specification refers to Typical Application Circuit.
Note 2. This device is ESD sensitive. Use of standard ESD handling precautions is required.
Note 3. Abnormal condition; Ex: over-current, under-voltage lockout, soft-start disappear.

■ Typical Application Circuit



*** Vout = 0.8 x (1+R3/R2)**
R2 ≅1K ~ 10K

■ Virtual Frequency Control

Virtual Frequency Control™ combines the advantages of constant frequency and constant off-time control in a single mode of operation. This allows fix frequency, precision switching voltage regulator control with fast transient response and the smallest solution size. Switch duty cycle can be adjusted from 0% to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. Figure 1 depicts a simplified operation of the Virtual Frequency Control technique: The VFC oscillator generates a pulse of a known duration (VFC_Pulse). The regulator loop responds by returning a complementary feedback pulse (FB_Pulse). The FB_Pulse duration is a result of external conditions such as inductor size, the voltage across the inductor and the duration of the VFC_Pulse. A VFC control loop is then formed whereby the duration of the VFC_Pulse is modified as a result of the FB_Pulse duration. The VFC loop arrives at a state of equilibrium, where the operating frequency remains inherently constant.

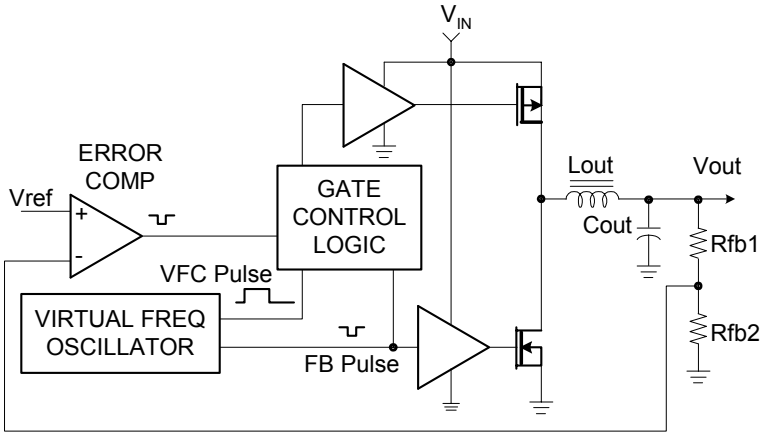


Figure 1: Virtual Frequency Control Loop-Synchronous single supply application.

■ Virtual Frequency Control (Continued)

Virtual frequency control is a technique that provides stable, constant frequency of operation for pulse controlled architectures such as constant off-time/on-time. This is all done internal to the IC with minimal number of components and without the need for connections to external terminals such as input and/or output. No external compensation is required, thus providing a low cost, high performance fix frequency solution for switching voltage regulators.

Virtual Frequency Control is a trademark of PWRTEK, LLC.

■ Function Description

Synchronous Buck Converter

Primary V_{CORE} power is provided by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including soft-start, shutdown, and cycle-by-cycle current limit.

Referring to the functional block diagram FIG 1, the output voltage of the synchronous converter is set and controlled by the output of the error comparator. The external resistive divider reference voltage, is derived from an internal trimmed-bandgap voltage reference. The inverting input of the error comparator receives its voltage from the FB pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the virtual oscillation frequency to 200KHz. The virtual frequency oscillator sets the PWM latch. This pulls DRVN low, turning off the low-side N_MOSFET and DRVP is pulled low, turning on the high-side P-MOSFET (once the cross-current control allows it). The triangular voltage ramp at the FB pin is then compared against the reference voltage at the inverting input of the error comparator. When the FB voltage increases above the reference voltage, the comparator output goes high. This pulls DRVP high, turning off the high-side P-MOSFET, and DRVN is pulled high, turning on the low-side N-MOSFET (once the cross-current control allows it). The Virtual Frequency Oscillator then generates a programmed off time to allow the FB voltage to return to the valley voltage of the triangular ramp. At the end of the off time the PWM latch is set and the cycle repeats again.

Under Voltage Lockout

The under voltage lockout circuit of the AP2007 assures that the high-side P-MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 3.8V. Normal operation resumes once V_{CC} rises above 4.0V.

$R_{DS(ON)}$ Current Limiting

The current limit threshold (0.4V) is set by connecting an internal resistor from the V_{CC} supply to OCSET. Vocset is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an over-current condition occurs and the soft start cycle is initiated. The synchronous switch

turns on and $\overline{SS/SHDN}$ starts to sink 2uA. When $\overline{SS/SHDN}$ reaches 0.2V, it then starts to source 10uA and a new cycle begins. When the soft start voltage is below 0.9V the cycle is controlled with pulse by pulse current limiting.

Soft Start

Initially, $\overline{SS/SHDN}$ pin sources 10uA of current to charge an external capacitor. The inverting input of the error comparator is clamped to a voltage proportional to the voltage on $\overline{SS/SHDN}$. This limits the on-time of the high-side P-MOSFET, thus leading to a controlled ramp-up of the output voltages.

■ Function Description (Continued)

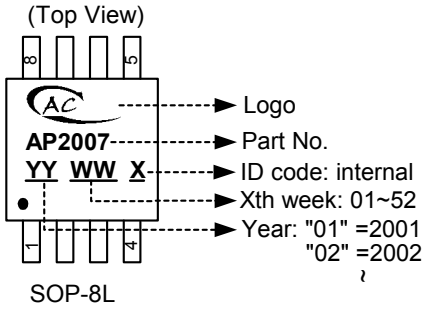
Hiccup Mode

During power up, the SS/$\overline{\text{SHDN}}$ pin is internally pulled low until V_{CC} reaches the under-voltage lockout level of 4V. Once V_{CC} has reached 4V, the SS/$\overline{\text{SHDN}}$ pin is released and begins to source 10uA of current to the external soft-start capacitor. As the soft-start voltage rises, the inverting input of the error comparator is clamped to this voltage. When the error signal reaches the level of the internal 0.8V reference, the output voltage is to have reached its programmed voltage. If an over-current condition has not occurred the soft-start voltage will continue to rise and level off at about 2.5V.

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the SS/$\overline{\text{SHDN}}$ pin begins to sink 2uA. The soft-start voltage will begin to decrease as the 2uA of current discharge the external capacitor. When the soft-start voltage reaches 0.2V, the SS/$\overline{\text{SHDN}}$ pin will begin to source 10uA and begin to charge the external capacitor causing the soft-start voltage to rise again. If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the SS/$\overline{\text{SHDN}}$ pin will again begin to sink 2uA. This cycle will continue indefinitely until the over-current condition is removed.

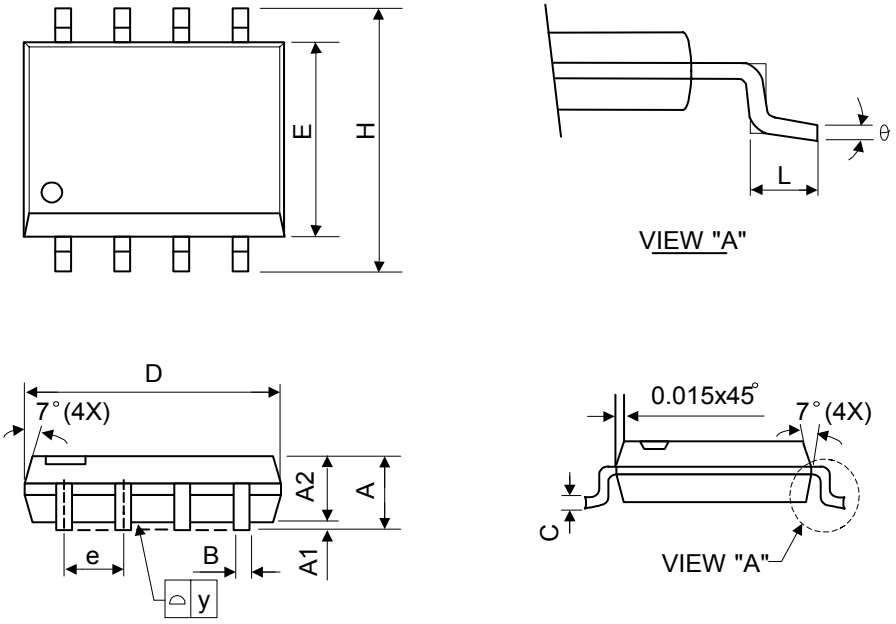
In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to GND.

■ Marking Information



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{O}	-	8^{O}	0^{O}	-	8^{O}